		APPLICATION FOR ESCC QUALIFICATION APPROVAL				Page 1 Appl. No. 393
Component Title: Integrated Circuits, Silicon, Monolithic, Radiation-Hardened 32-bit ARM Cortex-M7 Microcontroller (SAMRH707)		Executive Member: CNES		Date: 12/05/2025		
Components (including series and families) submitted for Qualification Approval						1
ESCC COMPONENT. NO.	VARIANTS	RANGE OF COMPONENTS	BASED ON	TEST VEHICLE / S	COMPONENT SIMILAR	
9512/008	01	Integrated Circuits, Silicon Monolithic, Radiation-Hardened 32-bit ARM Cortex-M7 Microcontroller	SAMRH707 - ATMx150RHA technology	SAMRH707 CQFP-164	NA	
Component Manufacturer MICROCHIP TECHNOLOGY NANTES		Location of Manufacturing Plant LA CHANTRERIE – ROUTE DE GACHET BP70602 44306 NANTES CEDEX		ESCC Specification used for Qualification Generic: ESCC9000 Issue: 11 Detail/s: 9512/008 Issue: 1		
Qualification Report Reference and date: QP-SAMRH707 Rev C Date: 01/02/2025			PID used for manufacturing Qualification Lot Ref No: PID0041 Issue: 0 Date: 03/04/2025			
PID changes since start of qualification None <input checked="" type="checkbox"/> Minor* <input type="checkbox"/> Major* <input type="checkbox"/> (* Details not published, provided in confidential annex 2.)			Current PID Verified by CNES Name of Executive Representative Ref No: SAMRH707 PID 0041 Issue: 0 Date: 03/04/2025			
Current Manufacturing facilities surveyed by: CNES (D. Dangla) ESA (S. Hernandez)						9
(Name of Executive Responsible) _____ (Date) _____						
Report Reference DTN QE EC-2024.0014739 - CR-ESCC QML survey MCHP-16102024.pdf						
Satisfactory: Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Explain						
Quality and Reliability Data Evaluation testing performed Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Report Ref. No.: _____ Date: _____ Equivalent Data: Single Phase Qualification applies Certification:			Failure analysis, DPA, NCCS available Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> (supply data) Ref Nos. and purpose: Construction analysis reports done by MCHP/SERMA: SERMA 24-2560-100_240716.pdf (July 16th, 2024)			

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	Component Title: Radiation Tolerant Arm Cortex-M7 Microcontroller (SAMRH707)		Appl. No.
Executive Member: CNES	Date: 12/05/2025		393

The undersigned hereby certifies on behalf of the ESCC Executive, that the above information is correct; that the appropriate documentation has been evaluated; that full compliance to all ESCC requirements is evidence except as stated in box 13; that the reports and data are available at the ESCC Executive and therefore applies for ESCC qualification status to be given to the component(s) listed herein.

Date: 12/05/2025

Fontaine Lya

Signature numérique de Fontaine Lya

L. FONTAINE

Date : 2025.05.12 15:11:30 +02'00'

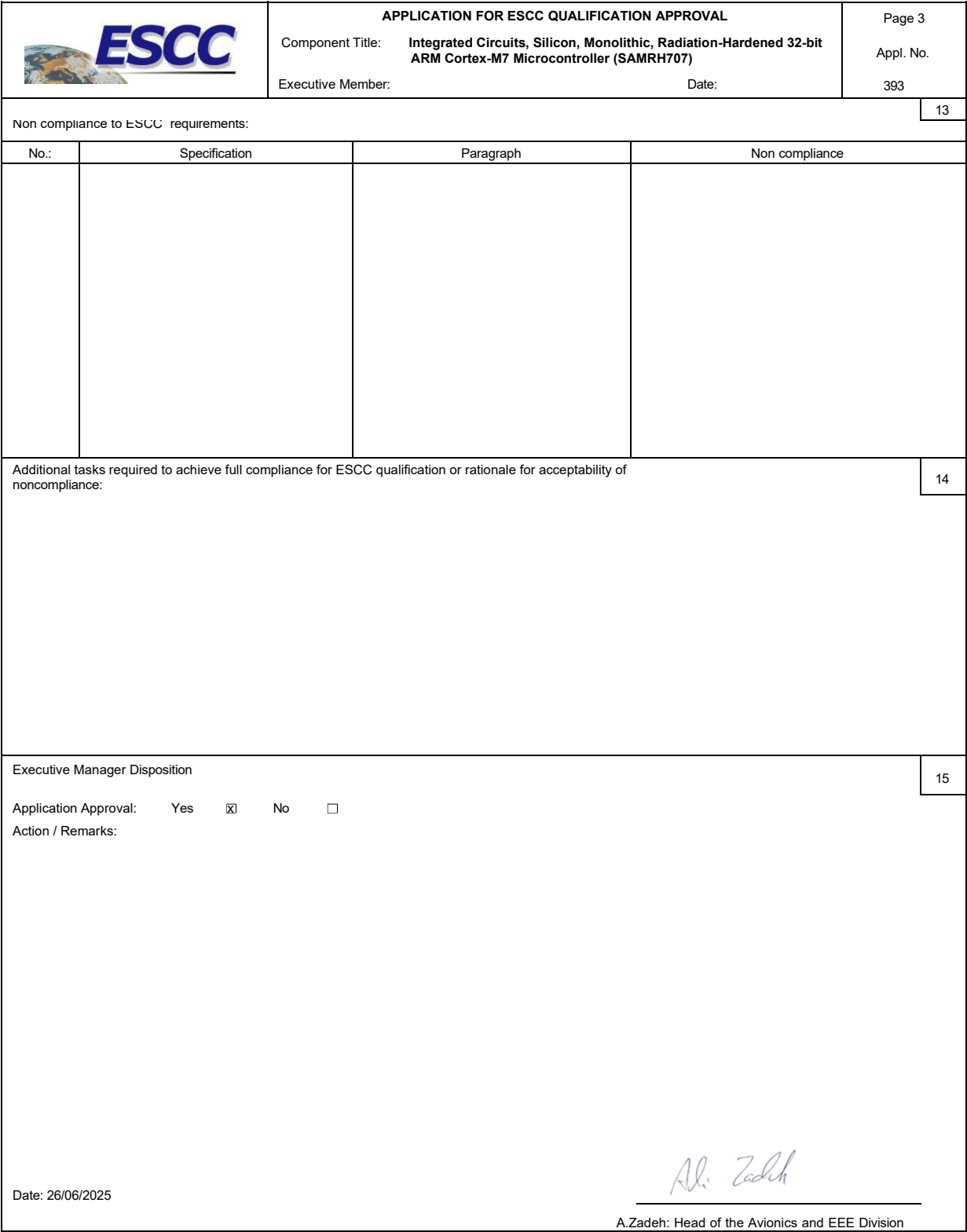
(Signature of the Executive Coordinator)


Continuation of Boxes above: (Only non-confidential comments)

Qualification Package SAMRH707 - QP_SAMRH707.pdf (Rev C)

SAMRH707 ESCC QPL - submission 2025-02 rev1.pptx
RAD-SAMRH707.pdf
2022-EC-1037_TID ELDRS report SAMRH707_rev2.0.pdf

Construction analysis reports done by MCHP/SERMA:
SERMA 24-2560-100_240716.pdf (July 16th, 2024)



	APPLICATION FOR ESCC QUALIFICATION APPROVAL Component Title: Integrated Circuits, Silicon, Monolithic, Radiation-Hardened 32-bit ARM Cortex-M7 Microcontroller (SAMRH707) Executive Member: _____ Date: _____	Page 4 Appl. No. 393
ANNEX 1: LIST OF TESTS DONE TO SUPPORT QUALIFICATION		16
Tests conducted in compliance with: - ESCC 9000 generic specification; Chart F4 (for ESCC/QPL parts); - Or PID-TFD _____ (for ESCC/QML parts) Tests vehicle identification/description:		
SAMRH707 CQFP-164	The SAMRH707 is a high-performance microcontroller based on the 32-bit Arm Cortex-M7 RISC processor with Floating Point Unit (FPU). The device operates at a maximum speed of 50 MHz and features 128 Kbytes of Flash, 16 Kbytes of dual-cache memory, more than 320 Kbytes of embedded SRAM (128 Kbytes of DTCM memory, 64 Kbytes of ITCM memory, and 128 Kbytes of multiport SRAM), 128 Kbytes of ROM with bootloader firmware pre-installed and external memory interfaces for EEPROM, Flash, and SRAM. All memories include embedded Error Correction Code (ECC) protection. The peripheral set includes two CAN-FDs, up to four FLEXCOMs (USART/UART/SPI/I2C), SpaceWire and Mil-Std-1553 links, as well as high-performance SHA, TRNG, CRCCU, ICM, and PCC. It also includes a 12-bit ADC (16 channels) and a DAC (three channels, with two single-ended, and one differential).	
Detail Specification reference: 9512/008 issue 1 Draft A		



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Qualification results – Environmental/Mechanical subgroup

The SAMRH707 is part of the package family “Flat-Substrate CQFP”:

(SubGroup 1 - Assy/Pack reliability tests - Not required – Included in the ATMX150RHA qualified domain)

	SAMRH707 (JAGUAR)	MMT assy line - qualified domain
Flat-substrate Package	R-CQ164-B	Up to CQFP352
Seam welded Lid	23.7 * 23.7 mm ²	Up to 31.2*31.2 mm ²
Die size	190 mm ²	Up to 219 mm ²
Die attach	JM7000	JM7000
Bonding	Ultrasonic wedge, AlSi 25 µm	Ultrasonic wedge, AlSi 25 and 32 µm



Environmental/Mechanical subgroup, required by ESCC every 2-years, is done every 26-weeks per package family.

In addition to monitoring, a specific SubGrp1/GrD has been performed on these assembly lots.

Chart F4	Test	Tick when done	Conditions	Assembly lot datecode	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Environmental/Mechanical Subgroup	Thermal Shock	<input checked="" type="checkbox"/>	MIL-STD-883. Test Method 1011B	A5XJ7A264M DC2350	15	0	15 shocks
	Temperature Cycling	<input checked="" type="checkbox"/>	MIL-STD-883. Test Method 1010C		(15)	0	100 cycles
	Moisture Resistance	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1004		(15)	0	
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	3 Temperature Electrical Test		(15)	0	Device specification
	Seal (Fine and Gross Leak)	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1014		(15)	0	
	Visual Inspection	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2009	A5XJFA264P DC2404	(15)	0	
	Mechanical Shock	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2002B		15	0	5 pulses
	Vibration	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2007A		(15)	0	12 sweeps
	Constant Acceleration	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2001E	A5XJGA264Q DC2407	(15)	0	Y1
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	3 Temperature Electrical Test		(15)	0	Device specification
	Seal (Fine and Gross Leak)	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1014		(15)	0	
	Visual Inspection	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2009		(15)	0	

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Endurance subgroup

Note:

Life-Test is done on each wafer lot.

For initial qualification, Life-Test has been extended up to 4000 hours/125°C/Vccmax.

No seal test has been performed after Life-Test.

Chart F4	Test	Tick when done	Conditions	Diffusion Lot Assembly lot Date code	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Endurance Subgroup	Operating Life-Test	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1005	DM92M.1 A5XJ7A264M DC2350	45	0	4000 hrs/Vccmax/125°C
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	Intermediate and End-Point Electrical Measurements in the Detail Specification	DM9Q6.1 A5XJFA264P DC2404 DM9Q7.1 A5XJGA264Q DC2407	(45)	0	

Assembly/Packaging capability is verified on each assembly lot.

- Solderability test, required by ESCC, is done on each assembly lot.

- Terminal strength test, required by ESCC every 2-years, is done every 26-weeks per package family.

Chart F4	Test	Tick when done	Conditions	Lot / Date Code	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Assembly Capability Subgroup	Marking Permanency	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2015	A5XJ7A264M DC2350	3#	0	
	Bond Pull tests	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2011		4#	0	22 wires
	Substrate attach strength	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2027		3#	0	
	Internal Visual Inspection	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 2010A	A5XJFA264P DC2404	2#	0	
	Solderability test	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 2003	A5XJGA264Q DC2407	3#	0	22 leads
	Terminal strength test	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 2004 B2		3#	0	45 leads
	Internal gas analysis	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 1018		3#	0	

Chart F4	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Additional Tests	HBM ESD	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 3015	DKTMSA289N DC2229 A5XHGA2AFV DC2238 A5XHJA2AG8 DC2240	3#	0	Ok up to 250V Class 1A
	CDM ESD	<input checked="" type="checkbox"/>	ANSI/ESDA/JEDEC JS-002	DKTMSA289N DC2229 A5XHGA2AFV DC2238 A5XHJA2AG8 DC2240	3#	0	Ok up to 750V Class C2b
	Electrical latch-up	<input checked="" type="checkbox"/>	JESD78	DKTMSA289N DC2229 A5XHGA2AFV DC2238 A5XHJA2AG8 DC2240	6#	0	2 parts tested/lot Current injection 100mA, Overvoltage 1.5*Vccmax, Class I: 25°C ambient
				A5XJA264N DC2350	6#	0	Current injection 100mA, Overvoltage 1.5*Vccmax, Class II: 125°C ambient
	TID	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 1019	Wafer Lot DM92M.1 DM9Q6.1 DM9Q7.1	27#	0	TID no NVM Ok 150 krad(Si) (22 ON and 5 OFF parts)
					27#	0	TID with NVM Ok 30 krad(Si) (22 ON and 5 OFF parts)
	SEL	<input checked="" type="checkbox"/>	JESD57, ESCC25100	Wafer Lot	4#	0	SEL LET threshold > 78 MeV.cm ² /mg.
				DM92M.1	3#	0	Note: For SEU, refer to "RAD-SAMRH707.pdf" rad test report

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Executive Member:

Date:

NOTES ON THE COMPLETION OF THE APPLICATION FORM FOR ESCC QUALIFICATION APPROVAL**ENTRIES****Form Heading**

shall indicate:— the title of the component as given in its detail specification or the name of the series or family; — the entering date; — the serial number and the suffix of the form.

Box 1

shall provide details given in table; in particular there shall be listed - the variants or range of variants; the range of components by using the ESCC code for values tolerances, etc.; the designation given in detail specification as 'based on'; ---under Test Vehicle enter either a cross or the specific characteristic capable to identify the component tested; — under component similar enter a cross.

Box 2 and 3

Manufacturer's name and location of plant where the components were manufactured and tested.

Box 4

Generic and detail specifications used during qualification program.

Box 5

Reference to test report(s) submitted in support of application.

Box 6

Enter details to identify the PID that was applicable at the time the qualification lot was manufactured.

Box 7

If the PID was evolved after qualification lot manufacture, adequate details of such evolution shall be provided together with reasons for changes. Major changes shall be clearly marked.

Box 8

The box serves to identify the current PID and the Executive Representative that has verified it together with the date of this occurrence.

Box 9

This box can be completed only after a physical visit to the plant to confirm that the practices, procedures, materials, etc. used in manufacturing the components are as described in the PID. This survey shall be carried out in accordance with the requirements of ESCC Basic Specification No. 20200 and its findings shall be recorded.

Box 10

Details entered shall be sufficient to evidence that an evaluation program according to ESCC Basic Specification No. 22600 has been performed and that the results thereof are summarized in the survey and test reports. If the evaluation program has not been carried out according to established ESCC documents, the applicant Executive Representative shall provide alternative data and declare its assessed degree of satisfactory compliance with the ESCC basic requirements. Reference shall be made to the reports on Destructive Physical Analysis (DPA), Failure Analysis and Non conformance (NCCS) issued during the Evaluation and/or Qualification Phase.

Box 11

Enter the name of the Executive Coordinator and the signature.

Box 12

To be used when there is a need to expand any of the boxes from 1 through 10. Identify box affected and reference the Box 12 in the relevant Box. Box 12 can be broken into 12a, 12b, etc. if several Boxes have to be expanded.

Box 13

Fill table as requested.

Box 14

Fill in any additional tasks required to achieve full compliance.

Box 15

All Executive recommendations on the application itself, special conditions or restrictions, modifications of the QPL or ESCC QML entry, letters to the manufacturer, etc. shall be entered clearly in Box 15, signed by the ESA Representative.

Box 16

Fill in Table as requested.

Box 17

Confidential details of PID changes shall be provided.

Box 18

State noncompliance with reference to specification(s) and paragraph(s). To simplify reference in Box 18 each nonconformance shall be sequentially numbered. If relevant state 'None'

Box 19

Any additional action deemed necessary by the Executive Representative to bring the submitted data to a standard likely to be accepted by the ESCC Executive should be listed herein or the reason(s) to accept the nonconformance.

Box 20

Additional Comments