REQUIREMENTS FOR THE TECHNOLOGY FLOW QUALIFICATION OF DISCRETE SEMICONDUCTOR COMPONENTS

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DCR No.	CHANGE DESCRIPTION

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1 PURPOSE

This specification provides additional information and requirements for the Qualification Approval of Discrete Semiconductor Technology Flows and Components, and their inclusion on the ESCC Qualified Manufacturer's List (QML). It outlines the additional specific requirements for the definition of Technology Flow and its boundaries, the establishment of a Quality Management Programme, the preparation of a Process Capability and Reliability Assessment Programme, an Evaluation Test Programme and Qualification Test Programme, and the performance of an On-site Validation Audit.

This specification shall be read in conjunction with ESCC Basic Specification No. 25400.

This specification does not directly define detailed requirements for a component Manufacturer but instead defines the points which the Manufacturer must address in his Quality Management Programme.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the Technology Flow certification.

- ESCC Basic Specification No. 20200, Component Manufacturer Evaluation
- ESCC Basic Specification No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- ESCC Basic Specification No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice
- ESCC Basic Specification No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application
- ESCC Basic Specification No. 22700, Requirements and Guidelines for The Process Identification Document (PID)
- ESCC Basic Specification No. 25400, Requirements for the Technology Flow Qualification of Electronic Components for Space Application.
- ESCC Generic Specification No. 5000, Discrete Semiconductor Components, Hermetically Sealed and Die.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

4 INTRODUCTION

ESCC Technology Flow qualification is the status granted to a Manufacturer's specified Technology Flow after successful completion of an evaluation, certification and qualification programme as defined in ESCC Basic Specification No. 25400, the relevant parts of ESCC Generic Specification No. 5000 and this specification. It is also the status granted to any component type which is both:

- Manufactured using, and within the boundaries defined for, a qualified Technology Flow.
- Defined by, and meets the requirements of, ESCC Generic Specification No. 5000 and the relevant ESCC Detail Specification.

5 DEFINITION OF TECHNOLOGY FLOW BOUNDARIES

5.1 GENERAL

The Manufacturer shall define the Technology Flow for which certification and qualification is sought, as required by ESCC Basic Specification No. 25400.

This Technology Flow definition shall also form the basis of a Process Identification Document (PID) to be produced by the Manufacturer which shall fulfil all of the requirements of ESCC Basic Specification No. 22700 in terms of content and configuration control. This definition must demonstrate that the Technology Flow and its corresponding boundaries represent a structured, properly controlled and monitored design methodology and manufacturing process for discrete semiconductors technologies.

To meet these requirements, the definition should, as a minimum, address the areas listed in the following paragraphs at least to the extent detailed therein. The definition should cover all elements of the Technology Flow where a change could affect product performance and would therefore need to be reviewed by the Technology Review Board (TRB) before being introduced. Additional information should be supplied whenever necessitated by the particular nature of the technology under approval.

Within the definition of the Technology Flow, five areas are of particular concern:

- The component design and procedures which are closely related to the manufacturing process (see Para. 5.2)
- The design system and procedures used to implement the component design methodology (see Para. 5.3)
- The component manufacture and assembly including materials and piece-parts (including the component package), technologies, and processes applied (see Para. 5.4)
- Inspection and test requirements (see Para. 5.5)
- Traceability (see Para. 5.6)

These areas are addressed in the subsequent paragraphs.

NOTE: When considered necessary and appropriate by the Manufacturer, any information considered as proprietary may be made available to the ESCC Executive on a limited access basis for review only within the Manufacturer's facility.

5.2 COMPONENT DESIGN

The component design is governed by a set of technology specific rules and parameters, commonly called 'Design Rules'. These rules define the construction and composition of all structures foreseen for the design and manufacture of the component in a specific technology.

The description of the design requires the definition of at least the following:

(a) A summary of the physical design rules including a reference(s) for the applicable procedure(s), documents(s) and issue(s).

(b) A summary of the electrical design rules including a reference(s) for the applicable procedure(s), documents(s) and issue(s).

(c) A summary of any other requirements relevant to the design not covered in the previous points including, as applicable, a reference(s) for the applicable procedure(s), documents(s) and issue(s).

5.3 DESIGN SYSTEM

The design methodology is defined by the design system and all other procedures applied in the design of a component. The design system comprises all software, basic design data and the hardware platform.

Technology Flow Qualification of a design system requires as a minimum:

- The implementation of a configuration control system guaranteeing the traceability of all software and data forming part of the system.
- The application of a quality assurance system addressing at least documentation procedures, acceptance testing prior to system release and the organisation of error reporting and corrective action procedures.

Both systems shall be fully documented, and their application must be evident.

At least the following items shall be covered in the PID:

(a) The design flow-chart including a general description of the design system plus block diagrams representing:
- The software structure of the system.
- The design flow, distinguishing between interactive and automatic actions.
- The data flow within the system, with emphasis on the dynamics of the accumulated design data.

(b) A description of the hardware platform (e.g. workstations, memory requirements, LAN, host computers, etc.).

(c) Software and associated data shall be described in terms of:
- The origin and version of the programme.
- A comprehensive description of its functional scope.
- The programming language and the amount of code.
- The memory requirements.
- Definition of data formats and description languages.
- Definition of programme interfaces.
- A description of the human interface with permitted or required interactivity, and output format.
- All software serving simulation type purposes require a detailed description of the underlying models and their parametric capability.

(d) A description of the configuration control system.

(e) A description of the quality assurance system.

5.4 MANUFACTURE AND ASSEMBLY

The Technology Flow definition shall as a minimum cover the following areas with regards to the manufacture of components within the boundaries of the Technology Flow.

5.4.1 Materials and Piece-Parts

The Manufacturer shall summarise the procedures for provision of all materials and piece-parts (including semiconductor wafers and dice, and the component package) used for the manufacture of components. The summaries should include, but not be limited to, the following areas:

- The selection and approval of the materials and piece-parts, and vendors used, where applicable.
- A list of materials and piece-parts used, and the associated procurement specifications, as applicable.
- A list of incoming inspection procedures and other documents used to ensure the consistent quality of materials and piece-parts used.
- Procedures for traceability, and control of limited shelf-life items.

5.4.2 Technologies

The Manufacturer shall summarise the basic technologies used for the manufacture and assembly of components. The summaries should include, but not be limited to, the following areas:

- Materials and piece-parts preparation processes.
- Lot definition.
- Assembly process sequence.
- Finishing including marking.

5.4.3 Processes

The Manufacturer shall summarise the processes for the manufacture and assembly of components. They shall also give reference to the documents specifying the processes. The summaries, which shall include a statement on the equipment used, should include, but not be limited to, the following areas:

- Lot formation.
- Physical location of the manufacturing facility.
- Clean room conditions.
- Rework procedures.
- Handling and storage conditions.

5.5 INSPECTION AND TEST

The Manufacturer shall summarise the inspection and test facility characteristics for the manufacture and assembly of components. The test facility characteristics to be covered by the summaries should include, but not be limited to, the following areas:

- Implementation procedures for external visual or other test methods.
- Testing flow.
- Physical location of the test facility.
- Sample plans (quantity and acceptance numbers).
- Test procedures.
- Lot formation.

The Manufacturer shall summarise the inspection and test methods giving references to the documents specifying the methods. The summaries should include, but not be limited to, the following areas:

- Incoming inspection testing
- In-process controls/inspections & acceptance criteria
- Statistical process control (SPC) implementation
- Production control testing
- Customer Source Inspections
- Screening tests and associated electrical tests.
- Qualification testing.
- Periodic testing and Lot Validation Testing.

5.6 TRACEABILITY

The Manufacturer shall summarise his traceability system that allows for traceability from the device serial number to a specific wafer lot and production lot. Equivalent traceability must also exist for any test structures which are used. The summaries should include, but not be limited to, the following areas:

- The use of purchase orders and specifications.
- The use of route sheets and travellers.
- The traceability of materials, test vehicles, and components.

6 QUALITY MANAGEMENT PROGRAMME

As specified in ESCC Basic Specification No. 25400.

7 PARAMETRIC MONITORS AND TECHNOLOGY CHARACTERISATION VEHICLES

7.1 PARAMETRIC MONITORS

The Manufacturer should have parametric monitor test structures to be used for measuring electrical characteristics of each wafer type in a specified technology. The parametric monitor test structures can be incorporated into the grid, within a device die, as a dedicated drop-in die or any combination thereof. Location of the parametric monitor test structures should be optimally positioned to allow for the determination of uniformity across the wafer.

The Manufacturer should establish and document reject limits and procedures for parametric measurements including which parameters will be routinely monitored and which will be included in the SPC programme. Documentation of the parametric monitor should also include parametric monitor test structure design and test procedure, including electrical measurements at temperature, if any and the relationship between the measured limits and those determined in the Manufacturer's design and process rules. Alternative measurement techniques, such as in-line monitors are acceptable if properly documented.

7.2 TECHNOLOGY CHARACTERISATION VEHICLE (TCV) PROGRAMME

A TCV programme should be implemented by the Manufacturer for the technology or process being considered for certification. The programme should contain, as a minimum, those test structures needed to characterise a technology's susceptibility to all known, intrinsic reliability failure mechanisms.

The TCV test structures do not have to be a single die or location, but can appear on the parametric monitor or the device itself. The TCV programme should, however, indicate where the structures are located and how they are tested and analysed.

All of the TCV test structures shall be packaged using the same materials and assembly procedures as standard components in the technology. The packaging requirements for the TCV may be waived by the ESCC Executive if the Manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated ageing results. In any case, the TCV should be packaged in a suitable package to allow for the evaluation of the die technology without adversely affecting the outcome of the test.

Generally, TCV test structures shall be provided to verify all relevant material, process and device parameters.

8 PROCESS CAPABILITY AND RELIABILITY ASSESSMENT PLAN AND EVALUATION TEST PLAN

8.1 GENERAL

As part of evaluation, the Manufacturer shall build devices and/or special test structures, perform tests and analyses and run software benchmarks. These actions shall be designed to demonstrate, together with any existing information, the capabilities of the total manufacturing process with regard to quality, reliability and producibility, and its suitability for producing space level components. The necessary activities shall be described in either a process capability and reliability assessment plan and/or an evaluation test plan which should cover all design, manufacture, assembly, test and control processes which comprise the total manufacturing process.

As a minimum the plans must generate sufficient information to allow for a process capability demonstration covering:

(a) Design.

(b) Manufacture including:

- SPC and in-process monitoring programmes inducing parametric monitors and the TCV programme.
- Wafer acceptance.

(c) Assembly and packaging.

(d) Radiation hardness assurance (RHA), if applicable.

8.2 DESIGN

In the plan(s), the Manufacturer should address the methodology for the following areas of design, (this is also applicable if a third-party design centre is used). The design procedure and tools should be controlled in such a manner that the ensuing component design performs only within limits that have been shown to be reliable for the technology being used, within the constraints of established design rules.

(a) Component design
It shall be demonstrated that the design process results in components that are functional, predictable and accurate over the worst-case temperature and electrical extremes. It shall be demonstrated that the procedures used for design are capable of identifying all known design errors.

(b) Performance verification
Testing shall be performed on test vehicles representative of the full range of components covered by the Technology Flow to verify the performance of the component design is in line with the defined thermal and electrical design goals.

8.3 MANUFACTURE

8.3.1 Wafer Fabrication

The wafer fabrication facility should be controlled such that error free wafers are produced from the design database. This should include monitoring, controlling and reducing defect density.

The Manufacturer should identify a specific technology for the wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. The wafer fabrication process should then be controlled with the following:

(a) In-line statistical control.

(b) A parametric monitor structure for measuring electrical parameters.

(c) A TCV structure to study intrinsic reliability mechanisms.

8.3.2 SPC and In-Process Monitoring Programme

The Manufacturer should have an in-process monitoring system, including parametric monitors where appropriate, to control key processing steps to ensure device yield, reliability and radiation hardness assurance, if applicable.

The critical operations to be monitored should be determined by the Manufacturer based on his experience and knowledge of his processes. The resulting data should be analysed by appropriate SPC methods to determine control effectiveness.

8.3.3 TCV Testing

As part of evaluation, as a minimum, the quantity of TCV test structures for each wear-out mechanism, as specified in the Process Capability and Reliability Assessment Programme or the Evaluation Test Programme, should be subjected to accelerated ageing tests.

The TCV test structures should be randomly chosen from, and evenly distributed over, three homogeneous, non-consecutive wafer lots in the technology to be certified, and from the fabrication facility to be certified. These wafers must have passed wafer or wafer lot acceptance requirements, including all appropriate testing of parametric monitors.

The accelerated ageing experiments should provide an estimate of the mean time to failure (MTTF) and a distribution of the failure times under worst case operating conditions consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures, a worst-case operating lifetime or a worst-case failure rate can be predicted. Test structures should be from completed wafers which have been passivated/glassivated.

A summary of the accelerated ageing data and analysis should be prepared in a suitable form for review by the ESCC Executive. The initial evaluation MTTF, failure distribution and acceleration factors should be retained and used as benchmarks for the technology with which subsequent TCV results will be compared.

8.3.4 Wafer Acceptance Plan

The Manufacturer shall have a wafer acceptance plan based on electrical and radiation (if applicable) measurement of parametric monitors. This plan should utilise the parametric monitors and should include visual criteria, if applicable. In addition, the plan should address the concerns detailed in ESCC Basic Specification No. 21400 or equivalent test methods; alternative procedures utilising parametric monitors and in-line monitors can be proposed by the Manufacturer. The plan can be either a wafer-by-wafer acceptance plan or a wafer lot acceptance plan.

8.4 ASSEMBLY AND PACKAGING

The Manufacturer should demonstrate the capability of the assembly and package processes by performing a qualification exercise on an actual product package.

8.4.1 Assembly Processes

The Manufacturer should list the assembly processes (die attachment, wire/ribbon bonding, sealing and marking) that are expected to be listed in the ESCC QML and used in ESCC QML component assembly and should then qualify these processes by the testing of fully assembled packages in accordance with appropriate tests for the assembly/packaging technology used.

The assembly process related tests given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 5000, can be used by Manufacturers as a baseline guide to suitable qualification tests. Sample sizes should be defined by the TRB.

8.4.2 Package Technology Styles

The Manufacturer should document how packages used in the manufacture of ESCC QML products are qualified. In particular, the Manufacturer should document his criteria for deciding which packages can be treated as similar and show how these are grouped together for qualification and change control purposes. Package technology style qualification test methodologies, vehicles and results should be available. Key package characteristics for which testing must be addressed on each ESCC QML package technology style are:

- Dimensions.
- Resistance to moisture.
- Susceptibility to corrosion.
- Lead integrity.
- Thermal resistance.

The package technology related tests given in ESCC Basic Specification No. 22600 and the appropriate ancillary Basic Specification and ESCC Generic Specification No. 5000, can be used by Manufacturers as a baseline guide to suitable testing. Sample sizes should be defined by the TRB.

8.5 RADIATION HARDNESS ASSURANCE (RHA)

For components covered by the Technology Flow known to be susceptible to degradation in space radiation environments, encompassing Total Ionizing Dose, Displacement Damage, and Single Event Effects, as applicable, the Manufacturer should address RHA characterisation and verification. The Manufacturer should establish procedures to be followed to ensure that the components meet a specified RHA level (as specified by the Manufacturer). It is the responsibility of the Manufacturer's TRB to evaluate the test requirements, details and methods to be used.

9 ON-SITE VALIDATION AUDIT

9.1 GENERAL

The on-site audit by the ESCC Executive shall be performed in accordance with the requirements of ESCC Basic Specifications No. 20200 and No. 25400 and will cover, as a minimum, the following applicable areas of the Manufacturer's facility:

- Management.
- Quality assurance.
- Design.
- Manufacture.
- Assembly and package.
- Electrical test.

The on-site validation will be performed only after a satisfactory review of the Manufacturer's QM plan and self-validation results.

9.2 TECHNOLOGY VALIDATION

A satisfactory review of the following areas during validation by the ESCC Executive, where applicable, is seen as critical for ESCC QML certification and should cover:

- Design centre procedures.
- Design review procedures.
- Hardware software configuration and configuration management.
- Testability procedures.
- Archival system.
- TCV and parametric monitor tests and data.
- Fabrication rework procedures.
- Design rule documentation.
- Clean room procedures.
- Wafer traceability.
- Wafer and boule evaluation procedures.
- Assembly rework procedures.
- Die attach procedures.
- Wire/ribbon bonding.
- Device traceability and travellers.
- Lot formation (wafer, device and inspection).
- Assembly area environmental control.
- Internal water vapour control programme.
- Electrostatic discharge control and testing.
- Visual inspection.
- Human contamination prevention procedures.
- Equipment calibration and maintenance.
- Training policy and procedures.
- Electrical test procedures.
- Screening procedures.
- Periodic testing procedures.
- Third party design centre procedures.
- Die encapsulation/moulding.
- Qualification test plan.

10 QUALIFICATION TEST PLAN

10.1 QUALIFICATION TEST VEHICLES

The qualification test programme should define the relevant number of qualification test vehicles (TV) to cover the certified Technology Flow which the Manufacturer will produce on the certified manufacturing line. The qualification test vehicles should be of such complexity as to be representative of the ESCC QML components to be supplied by the Manufacturer. Each vehicle should operate and perform in compliance with the device specification and should be suitable for space use and which will not induce additional failures.

10.2 QUALIFICATION TEST PLAN

The qualification test plan should detail the test flow, test limits, test data to be measured, recorded and analysed, test sampling techniques and traceability records. As a baseline, the test flow should be based on the qualification testing specified in ESCC Generic Specification No. 5000 and the electrical measurements should be those given in the appropriate Detail Specification. The qualification test plan must be agreed and approved between the Manufacturer and the ESCC Executive.

10.3 QUALIFICATION TEST REPORT

The Manufacturer should present to the ESCC Executive an analysis of the qualifying data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TV data monitoring is adequate and can be correlated to the process. The ESCC Executive should be notified of any improvements/changes to the certified ESCC QML Technology Flow as a result of evaluation of the qualification test results.

The following data, if applicable, should be addressed and retained by the Manufacturer to support the results:

- Parametric monitor test data.
- Results of each subgroup test conducted, both initial and any resubmission.
- Number of devices tested and rejected.
- Failure mode and mechanism for each rejected device.
- Read and record variables data on all specified electrical parameter measurements.
- Where delta limits are specified, variable data, identified to the component serial number, should be provided for initial and final measurements.
- physical dimensions are checked, the actual dimensions of three randomly selected components should be recorded, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices has been approved.
- For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the components if no failures occur.
- For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.
- For RHA testing (if applicable), pre- and post-test end-point electrical parameters and test conditions.
- For internal water vapour content readings, report of all gases found.

10.4 QUALIFICATION TEST FAILURES

If any particular testing results are not successful, the Manufacturer should perform failure analysis and take any necessary corrective action after consultation with the ESCC Executive. The Manufacturer should notify the ESCC Executive of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

11 PROCUREMENT

Procurement of components manufactured within the boundaries of the qualified Technology Flow shall be in accordance with the requirements of ESCC Generic Specification No. 5000.