5.2.3 ST Microelectronics, France: ASIC platform C65Space

5.2.3.1 Contact Information

Address	ESCC Chief Inspector
STMicroelectronics (Tours) SAS 3 rue de Suisse 35200 Rennes France	Ms Emmanuelle Guerinel Tel. +33 2 99 26 4800 emmanuelle.guerinel@st.com
	ASICs QA Project Manager
	M. Jean-Noël LETRILLARD Tel. +33 2 99 26 4800 ext : 4937 jean-noel.letrillard@st.com

5.2.3.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
381A	Aug 2022	Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/086

STMicroelectronics Process Identification Documents:

- 8097046: GENERIC PID Ref. ST.01.2008

- DM00508779: PID FOR ASICs C65S WB and FC

- DM00508782: PID ASICs C65Space WB and FC Die Layout

5.2.3.3 List of Qualified Components

Component Number	Detail Specification	Generic part number	Circuit function	FPGA Matrix	Package
930401001A	9304/010	NX1H35AS-CQ352	3M System gate field programmable gate array	NX1H35AS	CQFP-352

5.2.3.4 Technology Flow Abstract

GENERAL FEATURES

The CMOS 65nm SPACE is a silicon technology node, 8 metal layers. It provides a logic capacity with additional DSPs, a 400 Mbs SpaceWire physical interface and also a DDR 2/3 physical interface. Benefiting from an advanced underlying technology, the NG-Medium provides high performances in terms of frequency and consumption. It is also reprogrammable without any limits.

- Power supply:
  - Core: 1.2V±10%.
  - IOS: 1.5V±10% or 1.8V±10% or 2.5V±10% or 3.3V±10%.
- Performance:
  - 250MHz Logic.
  - 333MHz DSP.
  - 800Mbps I/O.
- Temperature :
  - -55°C to +125°C.

BASIC INFORMATION

Main features

- 65 nm ST-SPACE process technology.
- 4-Input Look-up tables.
- Lut expender to support up to 16 bits boolean functions.
- High performance carry chains.
- Advanced interconnect network to support random logic and coarse grain block functions.
- DSP Blocks for complex arithmetic operations.
- User memories with variable width and depth.
- Configuration modes: JTAG, Parallel 8 bits, Parallel 16 bits, Serial dump bus, Space Wire
- Integrated Space Wire interface available for user applications.
- Dedicated lowskew distribution network for clock, reset and load enable signals.
- On-chip thermal monitoring capability.

Input/Output features

- Multiple I/O powering support from 1.5V to 3.3V
- Cold sparing support.
- Programmable output drive to support multiple industry standards.
- Embedded logic to support DDR2 and DDR3.
- 800 Mbps I/O support.
- LVDS compatible mode.
- All pins support 2000V of ESD-HBM.
- Embedded logic to support Space Wire Data Strobe encoding.
- Programmable delay lines on all pins.
- Programmable resistive termination.

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9202/086 and individual custom ESCC ASIC Sheets:

Part number	Part Type	Package	Temperature range
920208601A####	C65SPACE	CQFP-352	-55°C to +125°C

5.2.3.5 Technology Flow Definition

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of packaged products using ST C65Space silicon technology node and ST assembly line technology capabilities in CQFP352 package family.

7. Design

The following features are based on ST ESCC evaluated libraries from C65SPACE Design Environment:
- DSPs,
- DPRAMs & SPREGs memories,
- Input / Output in I/O Banks (except for the pas itself, which keeps original pad structure but receives Custom Design Add On featuring)
- Bitstream manager,
- PLLs (1201),
- Waveform generators,
- SapceWire Interface (including LVDS pads).

Other features designed by NanoXplore are full in compliant with ST C65Space design rules.

The NG-MEDIUM FPGA is based on NanoXplore patented interconnect architecture offering the highest logic density as well as high efficiency mapping. Application mapping is supported by NanoXplore tools based on proprietary algorithms tailored to the interconnect topology.

The device is composed of a central fabric embedding the programmable logic, RAM and DSP blocks, and peripheral I/O buffers. The fabric is covered with a grid of high level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/O buffers. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. The I/O buffers are arranged into multiple banks. Each bank has its own I/O buffer supply voltage.

8. Fabrication

The wafer manufacturing is performed in ST Crolles 300mm fab using the new C65SPACE technology silicon node developed in ST Crolles 300mm and successfully qualified by ST in September 2014.

The main characteristics of the silicon die are described below:

Mask Levels: 41.
Masks Levels of Metallization: 8 (7 Layers in Cu + 1 Layer Ta/TaN/AlCu).

Die size: 15.3*10.96 mm².
Die Pad Pitch: 70µm min.
Die Pad Opening: 44*108 µm².
Die Pads Numbers: 374 non-staggered.
Die Finish Front Side (passivation): PSG + Nitride.
Die Finish Back Side: Raw Silicon.
An additional step of OPM (Over Pad Metallization) deposition is performed at a third party subcontractor ChipBond (TW), under ST quality control.
OPM : TiW/Au (Au= 3.5µm±1µm)
OPM Pad size : 54*165 µm²

9. Assembly

Process

The assembly process of the C65 Space devices is set-up in the historical ST Space certified plant in Rennes, France using the main following process capabilities:

Die Attach Medium: “Cyanate Ester” JM7000
Wire Bonding technology: Ultrasonic Gold Ball-Bonding.
Wire: 0.8 mils (20µm) Gold 4N
Bonding Decks & Bonding wire number:

	CQFP352
Bonding decks N#	2
Bonding wires N#	448
Bond Wires on Deck #1	223
Bond Wires on Deck #2	225

Package

Ceramic Quad Flat Package with 352 leads (CQFP352) with Ceramic Tie Bar
Dimensions: 75*75*3.51 mm3.
Cavity Size: 17*12.66 mm²
Cavity Volume: 320 mm3.
Lid Material: Kovar with Plating Layers (Ni/Au)
Lid Size: 23.62*19.30 mm²
Lead finishing: Au Plated

10. Control and Test

The control & test of C65 Space devices are performed in both ST Grenoble plant, France for electrical testing and accelerated ageing (reliability screening) and Rennes, France for all other space related tests or at subcontracted third parties under Rennes Quality monitoring and control.

All these space related manufacturing operations are performed under the supervision and control of the ST ESCC Chief Inspector, located in our basic space plant, Rennes.

11. TCVs and SEC

TCV program has been carried out to address intrinsic failure mechanisms of the C65Space technology. NG-Medium encapsulated in CQFP352 are used as SECs to conduct all the requested evaluation and qualification tests.

12. Radiation Characteristics

The ST C65SPACE technology has been developed to fulfil the following characteristics:

- SEL immune up to LET > 60MeV.cm2/mg.
- TID tolerance = 300 krad(Si).

5.2.3.6 Manufacturing sites

DESIGN:
NanoXplore
1 avenue de la Cristallerie, 92310 Sèvres, France

WAFER FABRICATION:
ST Crolles 300 - 850 rue Jean Monnet 38926 Crolles, France

ASSEMBLY:
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

CONTROL AND TEST:
ST Grenoble - 12 rue Jules Horowitz, B.P. 217 38019 Grenoble, France
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

5.2.4 ST Microelectronics, France: ASIC platform FDSOI 28nm

5.2.4.1 Contact Information

Address	ESCC Chief Inspector
STMicroelectronics (Tours) SAS 3 rue de Suisse 35200 Rennes France	Ms Emmanuelle Guerinel Tel. +33 2 99 26 4800 emmanuelle.guerinel@st.com
	ASICs QA Project Manager
	M. Jean-Noël LETRILLARD Tel. +33 2 99 26 4800 ext : 4937 jean-noel.letrillard@st.com

5.2.4.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
394	Nov 2025	Integrated Circuits, Silicon, Monolithic, FDSOI 28nm ASIC Platform

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9304/012

STMicroelectronics Process Identification Documents:

- 8097046: GENERIC PID Ref. ST.01.2008

- DM00978658: PID for ASICs C28FDSOI Space FC

- DM00978698: PID for ASICs C28FDSOI Space FC Die Layout

5.2.4.3 List of Qualified Components

Component Number	Detail Specification	Generic part number	Circuit function	FPGA Matrix	Package
930401201P	9304/012	NX2H540TSC-FF1760	SoC field programmable gate array	NX2H540ATSC	FCTEBGA-1760

5.2.4.1 Technology Flow Abstract

GENERAL FEATURES

The NG-ULTRA NX2H540TSC is a Radiation Hardened By Design (RHBD) SoC FPGA in 28nm with quadcore ARM R52 running at 600MHz each, based on ST CMOS28FDSOI SPACE GEO Technology Platform from STMicroelectronics. It has a logic capacity of 537KLUT. The hardening techniques used in the NG-ULTRA, alongside the FD-SOI technology, provide radiation hardening performance.

NG-ULTRA NX2H540TSC contains two parts: A programmable logic matrix and Microprocessor subsystem.

First part is composed of a central fabric embedding the programmable logic, RAM and DP blocks. The fabric takes benefit from the highspeed connectivity such as High-Speed Serial Links (HSSLs) and DDR2/3 interfaces.
It is covered with a grid of high-level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/Os. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. I/Os are arranged into multiple banks. Each bank has its own I/O bu;er supply voltage.

Second part is the microprocessor subsystem which is based on a complete System on Chip.

Power Supply	Description	Maximum ratings (V)
Supply Voltages	VDDCORE VDD_AUX VDD_SWITCH	1 ±5% 1.8 ±10% 1.8 ±10%
Input/Output Voltage Range Complex I/O Bank: Simple I/O Bank:	VDDIO	 1.2; 1.5; 1.8; 1.8; 2.5; 3.3; ±10%

Table1: maximum ratings of VDDIo

BASIC INFORMATION

Main features

- Technology Node: ST CMOS28FDSOI SPACE GEO technology
- Processing System: Quad core ARM Cortex R52 based System-on-Chip (SoC)
- Programmable Logic:
  537KLUT (4-input Look-Up Tables)
  High-performance carry chains
  Advanced interconnect network enabling both logic and coarse-grain block functions
- Arithmetic Capabilities: Dedicated DSP blocks for complex computations
- User-configurable memories with variable width and depth
- Configuration interfaces:
  Master Serial SPI (Single, Sequential, Triple Modular Redundancy - TMR)
  SpaceWire Protocol Support
- Debug interfaces:
  JTAG

16-bit Parallel
UART
– Dedicated lowskew distribution network for clock, reset and load signals
– On-chip thermal monitoring for system reliability

Input/Output features

– Multiple I/O voltage supported from 1.2V to 3.3V
– Integrated Cold Sparing Capability
– Programmable output drive strength to support various industry standards.
– High-Speed Interfaces:
Embedded logic to support SpaceWire interface (data strobe encoding)
Embedded logic to support DDR2, DDR3 for the fabric + DDR4 via the SoC memory
Up to 1.6 Gbps I/O speed for SSTL, HSTL and POD standards
– LVDS compatible mode
– All I/O pins support 2000V ESD-HBM protection
– Programmable delay lines on complex I/O pins
– Programmable resistive termination on complex I/O pins
– Optional register single rate for direct I/O pins and single or double rate for complex I/O pins

COMPONENT TYPES

Device Types as per ESCC Detail Specification 9304/012 and individual custom ESCC ASIC Sheets:

Part number	Part Type	Package	Temperature range
930401201P	NX2H540ATS C-FF1760 (NG-ULTRA)	Fine pitch Flip-Chip Organic Ball Grid Array with 1760 balls (FF1760)	-40°C to +125°C

5.2.4.2 Technology Flow Definition

1. Design

NG-ULTRA is a SoC-FPGA divided into 2 parts:
• PS: It is composed of 4 ARM cores with multiple peripherals. The PS is responsible for booting, executing the ASW and transferring the bitstream to the PL part.
• PL: It is composed of a central fabric with analog elements on the ring. The PL is managed by a bitstream manager responsible for programming this matrix.

The NG-ULTRA PS features a quad-core ARM Cortex-R52, optimized for real-time and safety-critical systems. This architecture supports hardware-enforced isolation and fault tolerant execution, enabling secure partitioning of tasks and robust system behaviour under adverse conditions.

The following IPs are based on ST ESCC evaluated libraries from ST CMOS28FDSOI SPACE GEO Design Environment:

- Clock subsystem

- Reset subsystem
- Watchdog
- Bootrom
- Flash Controller
- AXI Controller
- Error Management
- QoS Monitor
- SoC Monitoring
- DMA
- eRAM
- RS DDR Controller
- Space Wire Boot AHB
- Network Interconnect
- UART
- DSP
- Register file
- Bitstream Manager
- iobank_complex
- iobank_direct
- iobank_hssl
- iobank_clockgen
- iobank_soc_ddr.

ST CMOS28FDSOI SPACE GEO Standard libraries :

analogmixed
C28SOI_AN_VTSENS_SPACE
C28SOI_PLL_PF_5000MHZ_SPACE
fuse
C28SOI_FU_SAFMEMHV_SPACE
digital standard cells
C28SOI_SC_12/8_CORE/CLK_LL/LR
C28SOI_SC_8_CORESPACE_LL
memory
C28SOI_MEM_ROM_SPACE
C28SOI_MEM_SRAM_DPHD_SPACE
C28SOI_MEM_SRAM_DPREG_SPACE
C28SOI_MEM_SRAM_SPHD_SPACE
C28SOI_MEM_SRAM_SPREG_SPACE
io
C28SOI_IO_SPACE

2. Fabrication

The wafer manufacturing is performed in ST Crolles 300mm fab using the ST CMOS28FDSOI SPACE GEO technology silicon node developed in ST Crolles 300mm and successfully qualified by ST in May 2019.

The main characteristics of the silicon die are described below:

Mask Levels: 42.
Masks Levels of Metallization: 11 (10 Layers in Cu + 1 Layer Ta/TaN/AlCu).
Die size: 21.888*20.348 mm2.
Die Pad Pitch: 180µm min.

Die Pad Opening: 87 µm.
Die Pads Numbers: 11236 non-staggered.
Die Finish Front Side (passivation): PSG + Nitride + PIX
Die Finish Back Side: Raw Silicon.

3. Assembly

Process

The assembly process of the ST CMOS28FDSOI SPACE GEO devices is set-up in the historical ST Space certified plant in Rennes, France using the main following process capabilities:

Substrate : FCTEBGA 45sq, 1760 land pads, SOP µBalls on FC Pads + OSP on bottom side
Flip chip soldering (lead free solder bump): flux dipping
SMD : Capacitor 0.1µF, 0603, 25v +/-10%, Pure Tin finishing, JAXA qualified
Underfill : epoxy liquid
Thermal Interface Material : thermal grease
Lid material : Copper Alloy, nickel finishing
Lid size : 44mm * 44mm
Lid attach : glue
Ball material : SnPb 63/37
Ball size : 0.64mm

4. Control and Test

The control & test of ST CMOS28FDSOI SPACE GEO devices are performed in both ST Grenoble plant, for electrical testing and accelerated ageing (reliability screening) and Rennes, for all other space related tests or at subcontracted third parties under Rennes Quality monitoring and control.
All these space related manufacturing operations are performed under the supervision and control of the ST ESCC Chief Inspector, located in ST basic space plant, Rennes.

5. TCVs and SEC

NG-ULTRA packaged in organic non hermetic FCTEBGA 45*45 is used as SEC to conduct all the requested evaluation and qualification tests.

6. Radiation Characteristics

Radiation Tolerance:
- Radiation-hardened design applied to configuration memories and registers for enhanced resilience
- Single Event Upset (SEU) immunity validated up to LET > 60 MeV.cm2/mg for configuration memory, DPRAM user memory and programmable logic registers.
- Total Ionizing Dose (TID) tolerance up to 50Krads (Si), ensuring long-term reliability in harsh environments
- Embedded Error Detection and Correction (EDAC) mechanisms safeguard user memory integrity

- Critical logic blocks are triplicated to enhance fault tolerance and reliability

5.2.4.3 Manufacturing sites

DESIGN:

NG-ULTRA
NanoXplore
1 avenue de la Cristallerie, 92310 Sèvres, France

WAFER FABRICATION:
ST Crolles 300 - 850 rue Jean Monnet 38926 Crolles, France

WAFER LOT BUMPING

AMKOR Korea - 150, Songdomirae-ro, Yeonsu-gu, Incheon 21991, Korea

WAFERLOT ELECTRICAL TESTING

ST GRENOBLE - 12 RUE JULES HOROWITZ, B.P. 217 38019 GRENOBLE, FRANCE

ASSEMBLY:
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

CONTROL AND TEST:

ST GRENOBLE - 12 RUE JULES HOROWITZ, B.P. 217 38019 GRENOBLE, FRANCE
ST RENNES – 3 RUE DE SUISSE 35200 RENNES, FRANCE. BASIC PLANT