



Description of MEMS 3D-System-in-Package Spacecraft Subsystems and Packaging Technology

Ångström Aerospace Corporation

R. Thorslund, P. Nilsson, M. Antelius, J. Davidsson, M. Hagström, E. Källén, E. Lamoureux, R. Lindegren, K. Lindqvist, V. Lindskog, A. Ljunggren, L. Stenmark, F. Bruhn



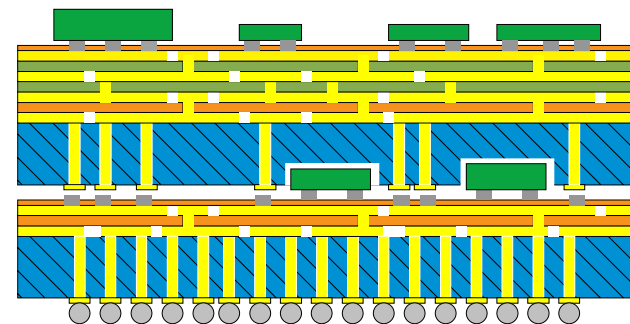
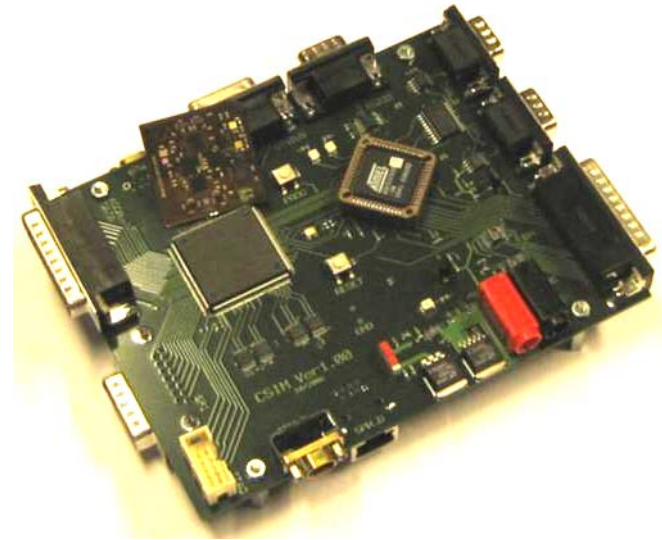
Outline

- 3D-System-in-Package (3D-SiP) module
- QA Procedures
- Manufacturing Examples
- 3D-SiP Remote Terminal Unit
- 3D-SiP Magnetic Attitude Controller
- 3D-SiP Solid State Mass Memory
- Flight Scheduled July 2008
- Acknowledgement



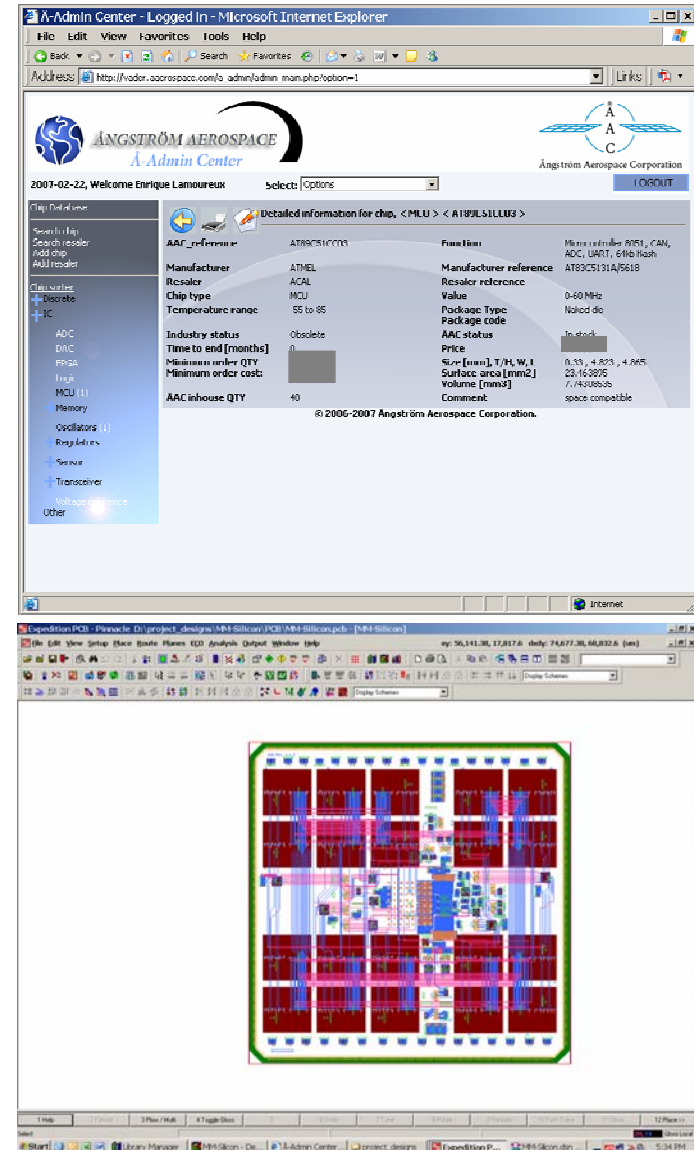
3D-SiP Module

- Extreme Size and Weight Reduction
- Heat Transfer
 - FR4 with 2 metal layers $k_{pe} \sim 21\text{W/mK}$,
 $k_{ne} \sim 0.3\text{W/mK}$
 - Silicon $k = 170\text{W/mK}$
- Thermal Expansion Match
- Short Signal Paths
- Fine Pitch Capabilities



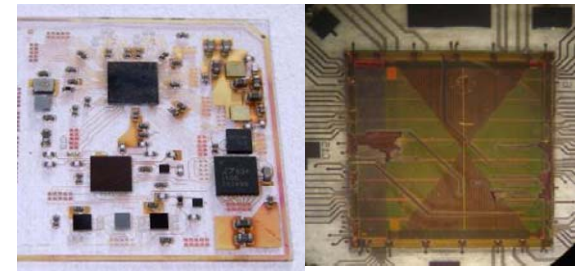
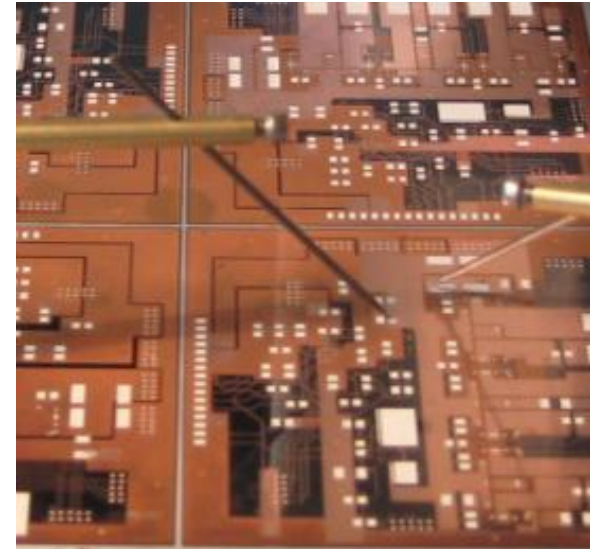
Standardized QA Procedures

- Component and Layout Database
 - Verified die map library
 - Standard layout library
- Standardized Test Procedures
- Process and Test Protocols
 - All process data recorded
 - QA test pattern
- Recipe Database
 - MEMS "cookbook"

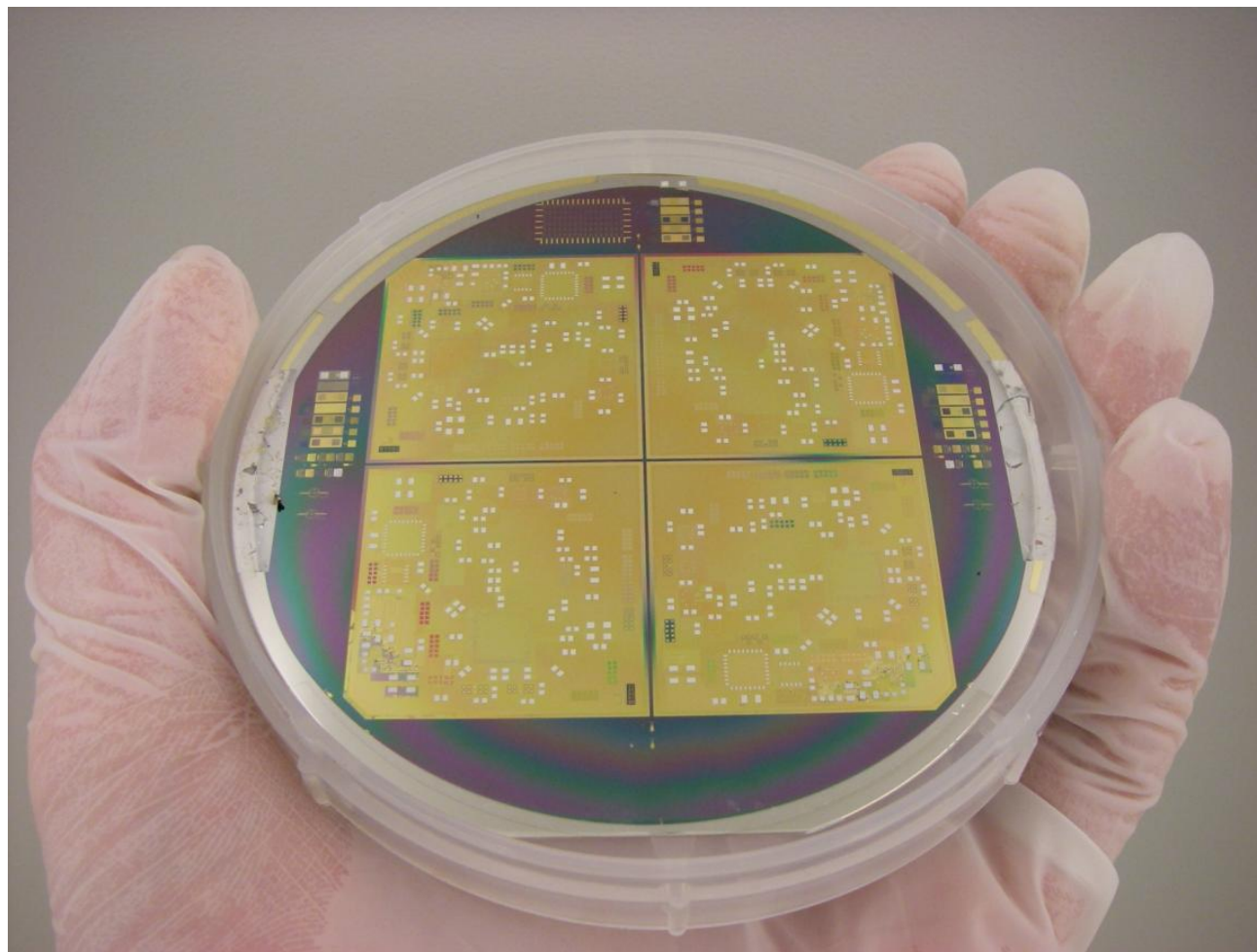


Standardized QA Procedures

- Continuous Probing During Manufacturing
 - Standardized testprotocoll
- Temperature Cycling
- IR Inspection
- X-ray Inspection
- Glas/Pyrex Wafers
 - Soldering verification
 - Pad layout verification

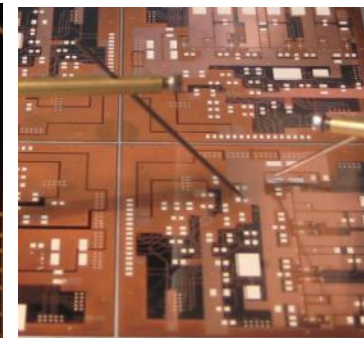
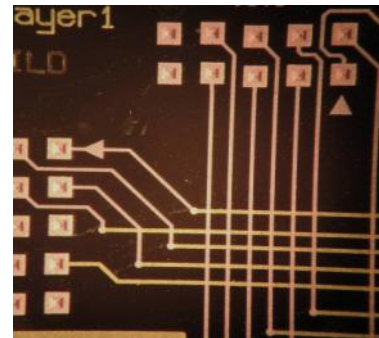
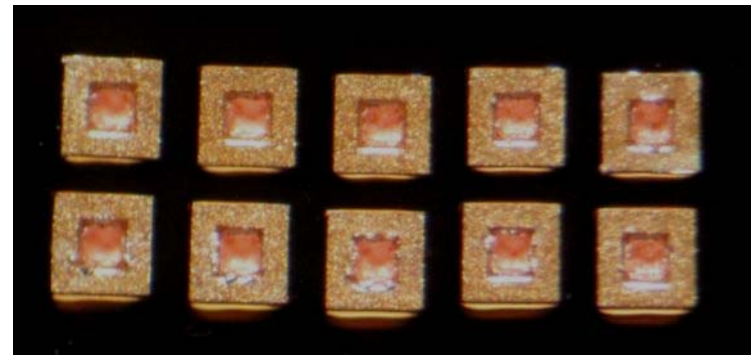
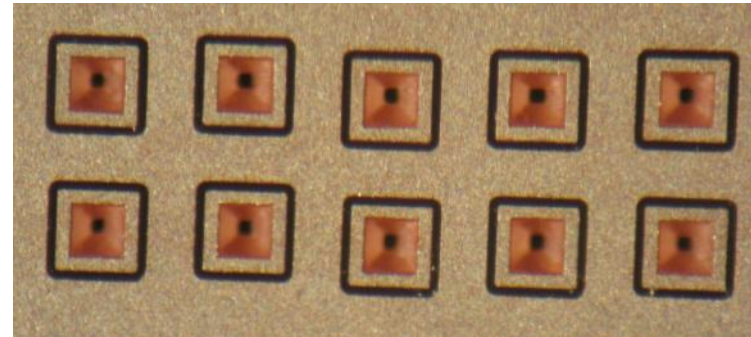


Manufacturing – 4” silicon wafers with Through Silicon Vias



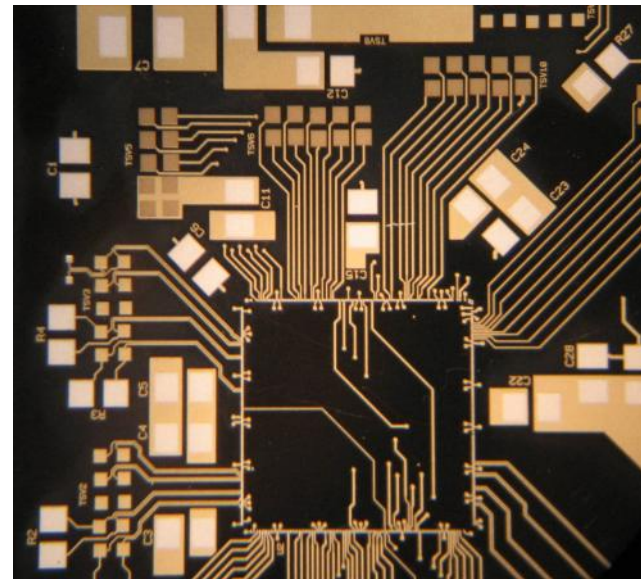
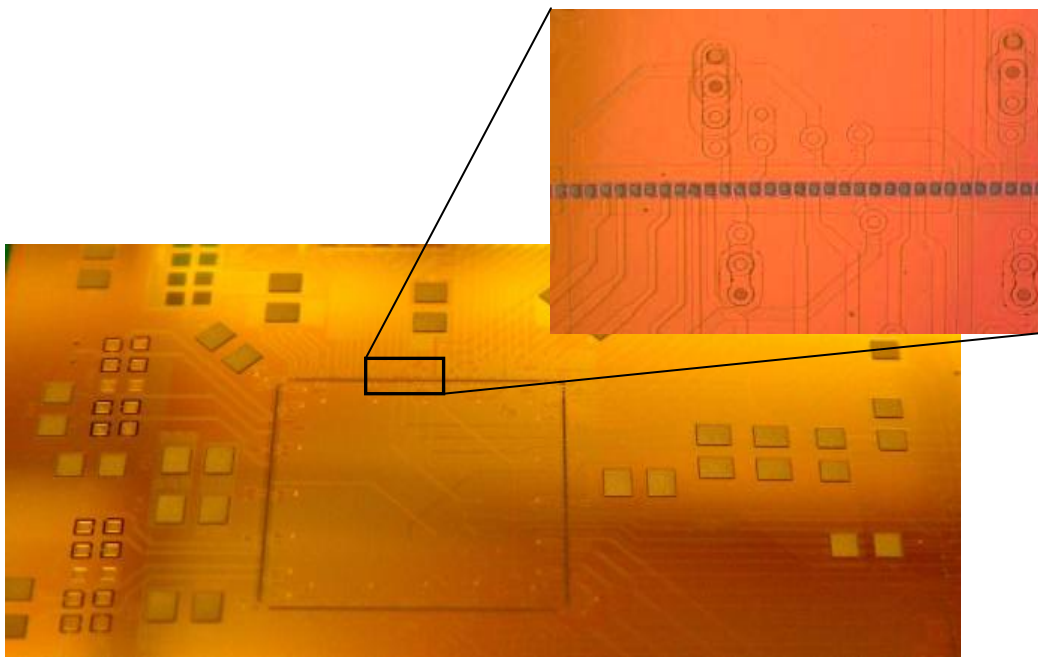
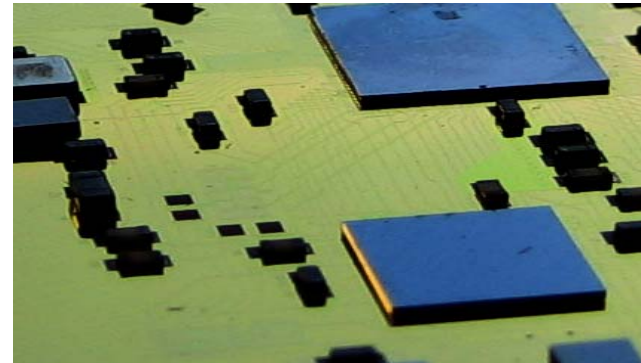
Manufacturing - Examples

- *Patent Pending* Through Silicon Vias (TSV)
 - High yield process
 - Variable Pitch
 - $\leq 20\text{m}\Omega$
- Metal Multilayers
 - Various metals
 - Choice of thickness
- ILD Multilayers
 - Various ILD's
 - Choice of thickness
- Open or Sealed TSV's
 - Open: fluidic/gas and electric
 - Closed: electric/environmental protection



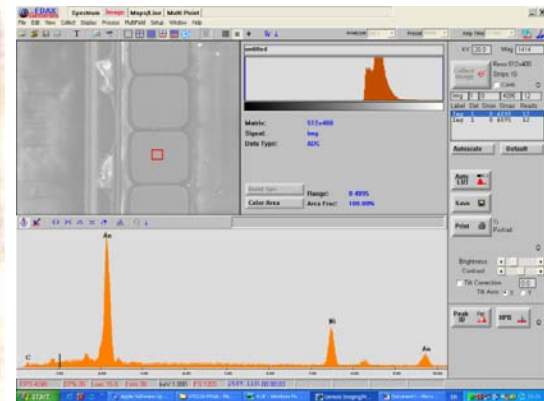
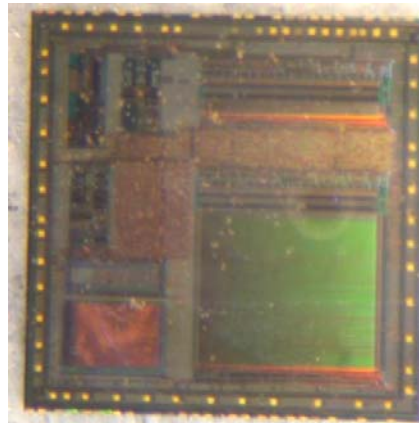
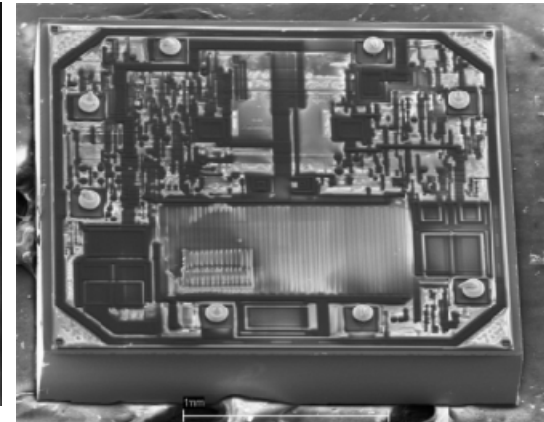
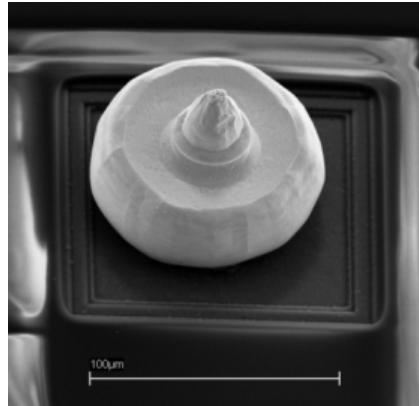
Manufacturing - Fine Pitch Chip Mounting

- Fine Pitch Capabilities
- Example
 - FPGA 350 MHz ACTEL 1MGate ProAsic3+
 - Pitch $57\mu\text{m}$, pad-pad $27\mu\text{m}$



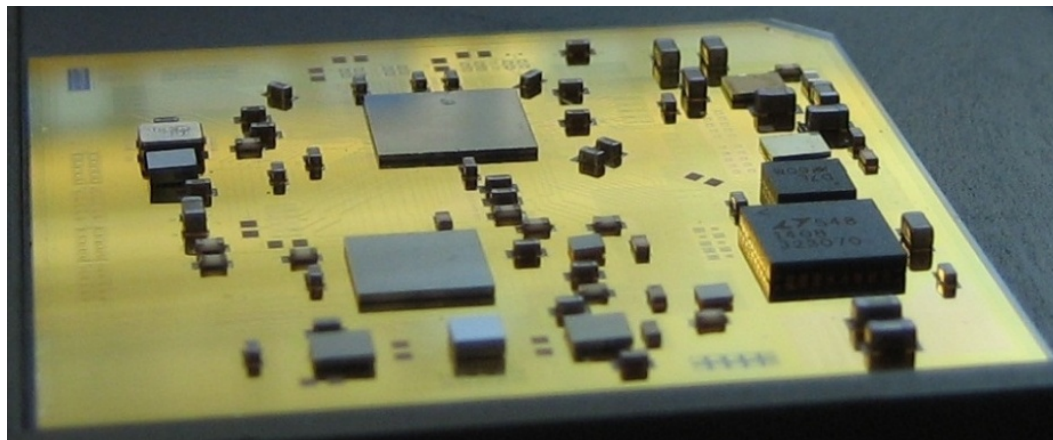
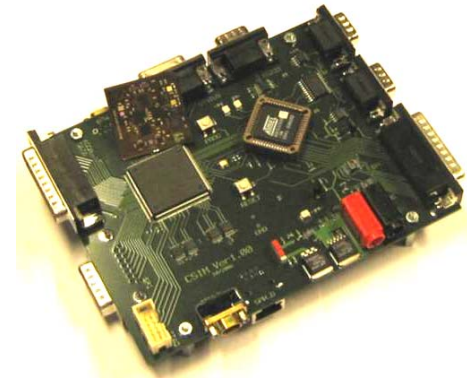
Manufacturing - Under-Bump-Metallization

- Flip Chip Technology
- Stud Bumping
- Remetallization at Chiplevel
 - Fine pitch
- Extensive Testing
 - SEM
 - EDS
 - ESCA
 - Roughness
 - Height



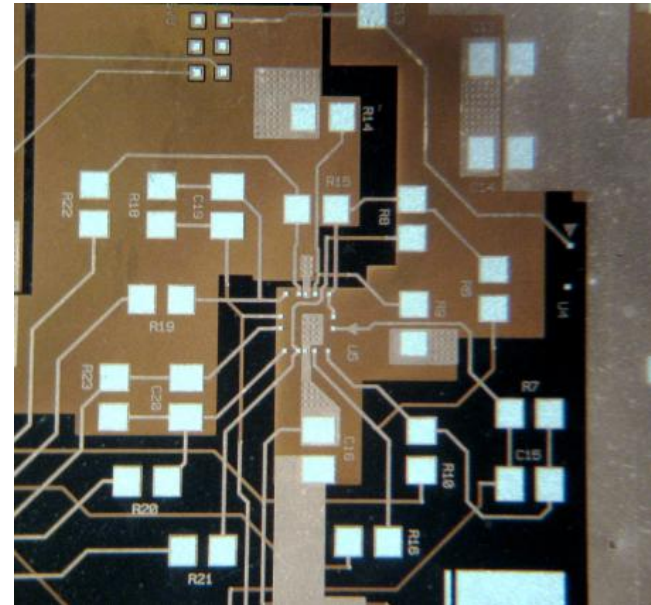
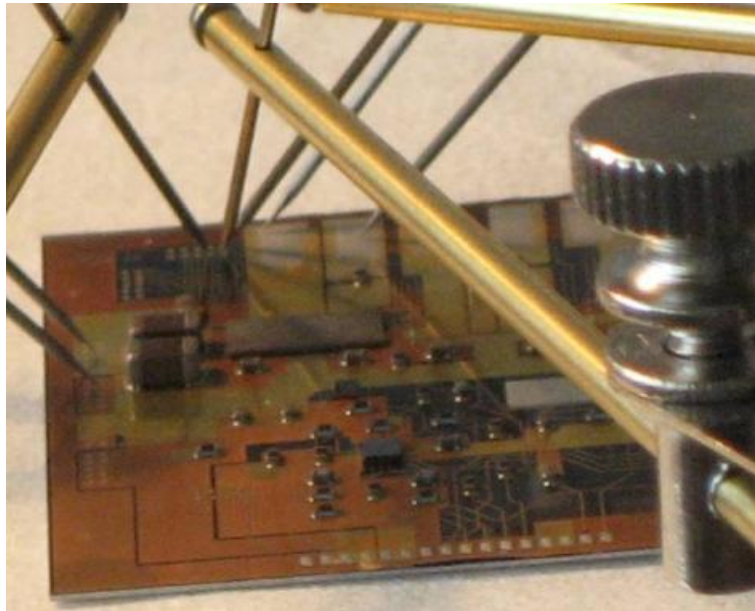
3D-SiP Examples -RTU

- 350 MHz ACTEL 1MGate ProAsic3+
- 60 MHz ATMEL T89C51CC03 Microcontroller
- Redundant Controller Area Network (CAN 2.0b compliant)
- Redundant high-speed LVDS drivers (SpaceWire or 1553)
- 6 x 14 bit Analog to Digital conversion user inputs (ADC)
- 4 x 12 bit Digital to Analog conversion user outputs (DAC)
- 48 bit CAN synchronizable System Elapsed time (32 bit seconds, 16 bit fractions)
- General 8-bit user I/O port (6 bit addressing and interrupts)
- Dimensions: 33 x 33 x 1 (mm)
- Mass: 3 grams



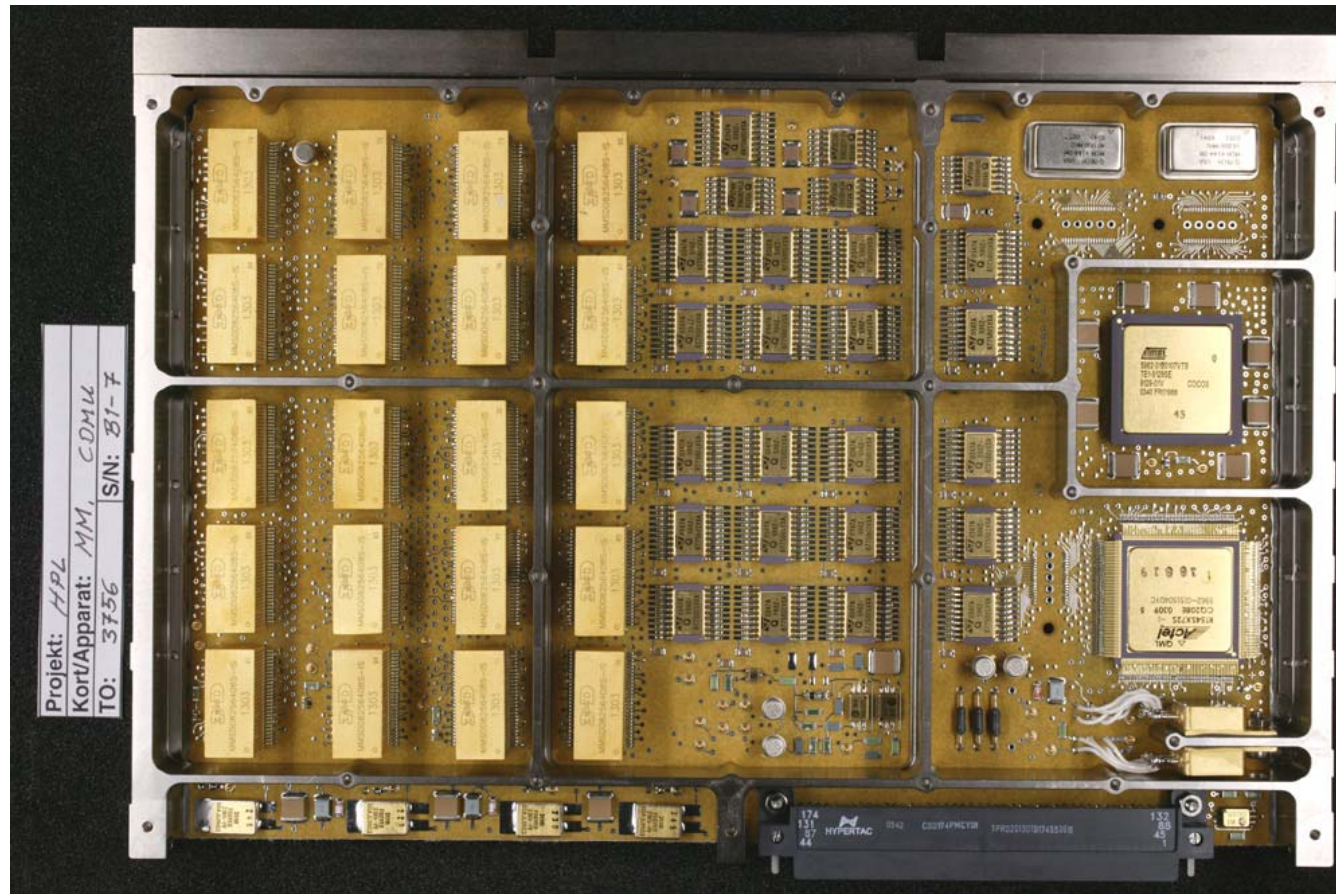
3D-SiP Examples -MACS

- 3 independent H-bridges 3A@12V, Max. 55V
- Filtering
- Pulse-width modulation (PWM) control
- Solderable to PCB and other substrates (optional)
- Analogue and serial magnetometer interfaces
- Dimensions: 33 x 33 x 1 (mm)
- Mass: 3 grams



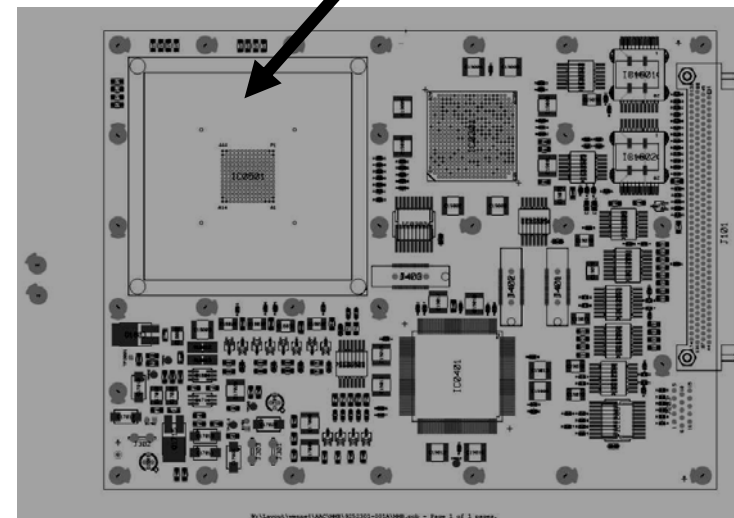
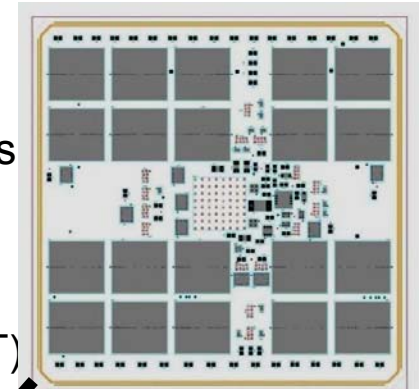
3D-SiP Examples - ÅAC / SAAB Space SSMM

- Solid State Mass Memory (SAAB Space, ESA Herschel Plank)

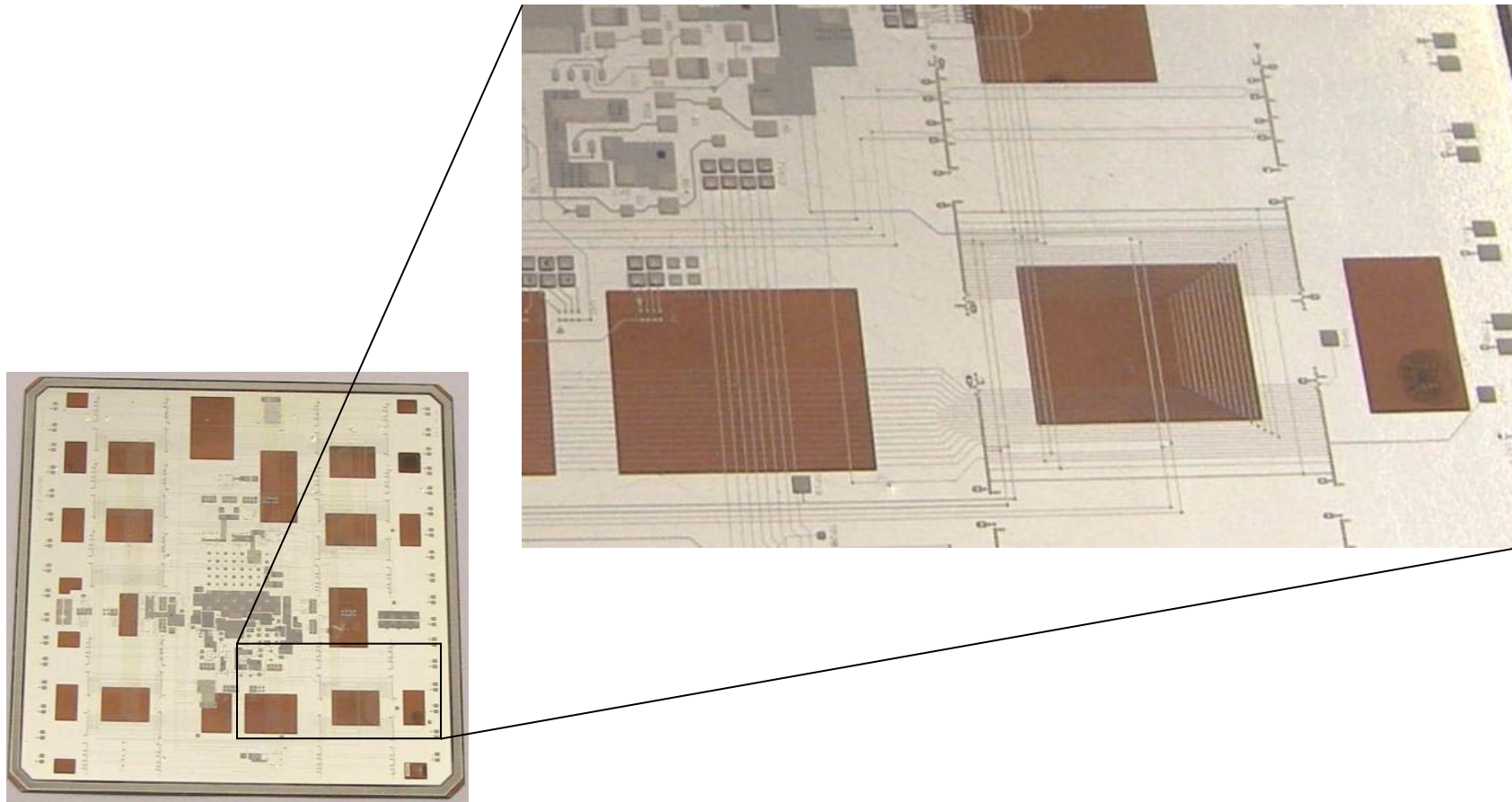


3D-SiP Examples - ÅAC / SAAB Space SSMM

- 32 Gbit (40 Gbit incl. EDAC) SDRAM Solid state MASS MEMORY
- 10 Gbit (incl. EDAC) / silicon wafer. Up to 4 stacked wafers
- Through Silicon Via (TSV) Technology
- Built in SEL protection in the silicon, response time ~ 100 ns
- All buffers built in the silicon
- Dimensions: 68 x 68 x 1(mm) , 8Gbit
- Only external part is memory controller (SAAB COCOS/NUT)



3D-SiP Examples - ÅAC / SAAB Space SSMM



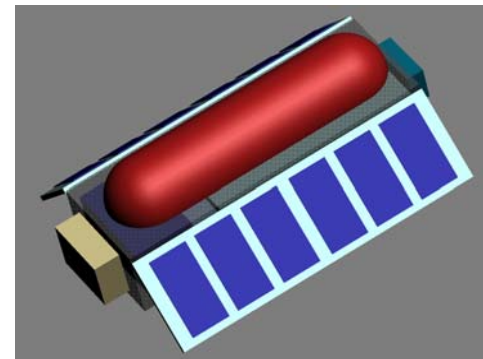
NanoRubin (Prime OHB System)

FLIGHT DATA

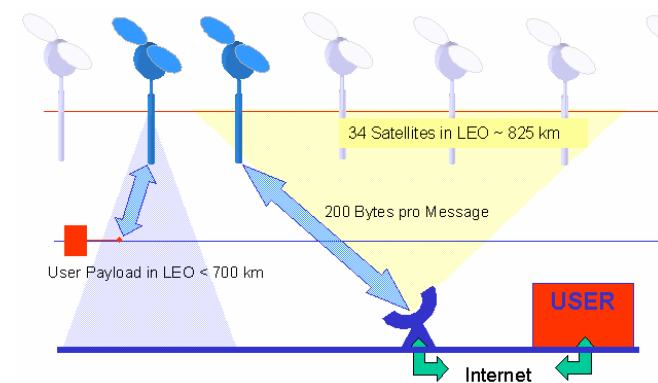
- NanoRubin-1
- Customer: SNSB
- Integrator: OHB System AG (Bremen)
- Launch vehicle: Russian COSMOS-3M rocket
- Launch: July 2008
- Satellite mission: Dedicated Technology Demonstrator Satellite
- Operation: Operation from AACs facilities in Uppsala for 1 year

ÅAC Contributions

- Prototypes of MACS
- Prototype of Mass memory with SAAB Space
- Prototypes of RTU
- Flight software validation



NanoRubin MNT internal (I1) and external (E1 & E2) payload accommodation



Communication with NanoRubin is performed via the ORBCOM network



Acknowledgement

