Wafer level high density 3D integration technologies for space applications

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Overview

- Introduction
- 3D integration:
  - 3D-"System-in-Package" (3D-SiP)
  - 3D-"Wafer-Level-Packaging" (3D-WLP):
    - die stacking
    - thin chip embedding
  - 3D-"Stacked-IC" (3D-SiC)
- Detector application examples
  - Custom analog design
  - BIB
  - Hybrid APS
  - Bold
  - RelaxD
- Conclusions & outlook

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Introduction

- Space requirements:
  - Ultimate performance
  - Small form factor, low volume, weight
- Evolution in radiation detection/imaging:
  - single pixel → linear array → 2D array
  - increase in resolution = decrease in pitch (down to few um)
- = thanks to development in **microelectronics fabrication technology**:
  - CMOS scaling
  - hybridisation using solder bumps
- Question: what's next ?
  - which new technologies become available ?
  - what are the benefits ?
- Answer: 3D integration technologies

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3D Integration approaches:
Introduction

- 3D integration drivers:
  - miniaturization
  - high density hybrid interconnection
  - interconnect speed and power
- 3D interconnects can be realized at different **levels** of the micro-electronic system, corresponding to different existing (commercial) microelectronic technology **platforms**:
  - die/package level → traditional packaging & interconnection technologies
  - post-processing of wafers → wafer-level packaging technologies
  - CMOS fabrication → IC-foundry technologies
- These technologies result in different 3D-interconnect densities and capabilities
- Choice of technology depends on the **interconnect requirements** of a given **application**

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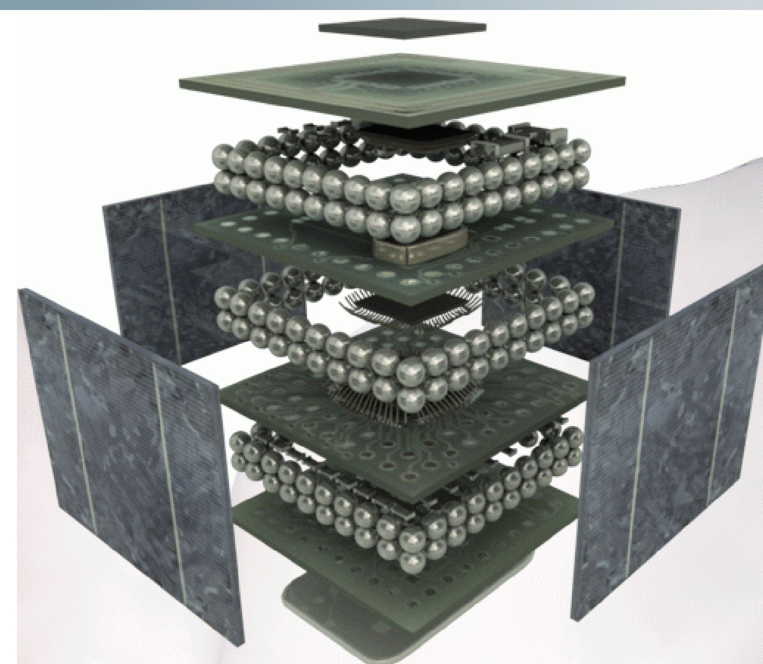
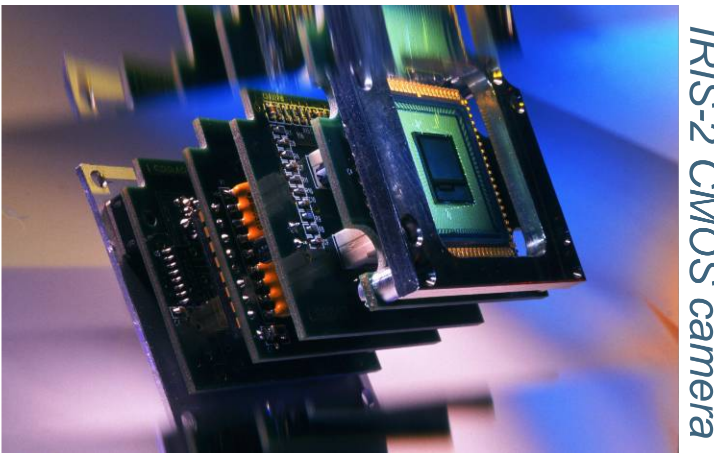
3D-SIP approach: Traditional packaging & interconnection

- Stacking of 2D-SIP "sub-systems"
  - each layer is an SIP PCB
  - different assembly technologies can be used
  - interconnect density: 2-3/mm, 4-11/mm^2
- Advantages:
  - generic 3D technology
  - each layer is fully tested before final assembly
  - best yield and manufacturability
- Limitations :
  - relatively low 3D interconnectivity
  - lack of standardization of package sizes
- Application:
  - intelligent/autonomous wireless sensor nodes
  - miniaturized imager systems





IRIS-2 CMOS camera

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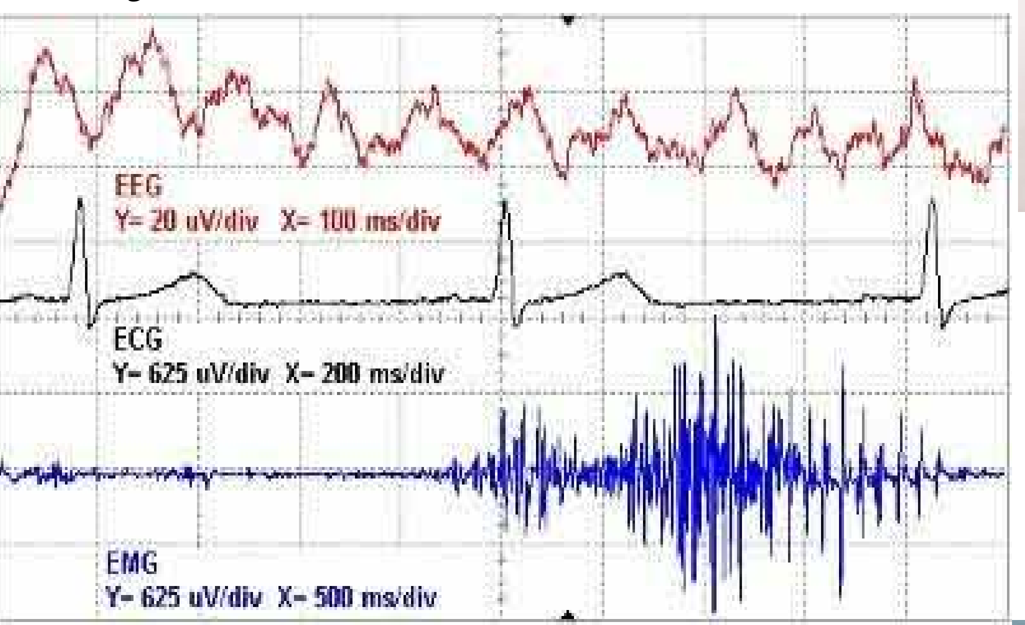
3D-SIP: Techno & application

- Technology:
  - stacking of PCB's
  - with individual components
  - using double solder ball for increased stand-off
- Application:
  - wireless EEG node

B. Gyselinckx et al., <u>ISSCC 2007</u>



1cm^3 wireless EEG/ECG SIP

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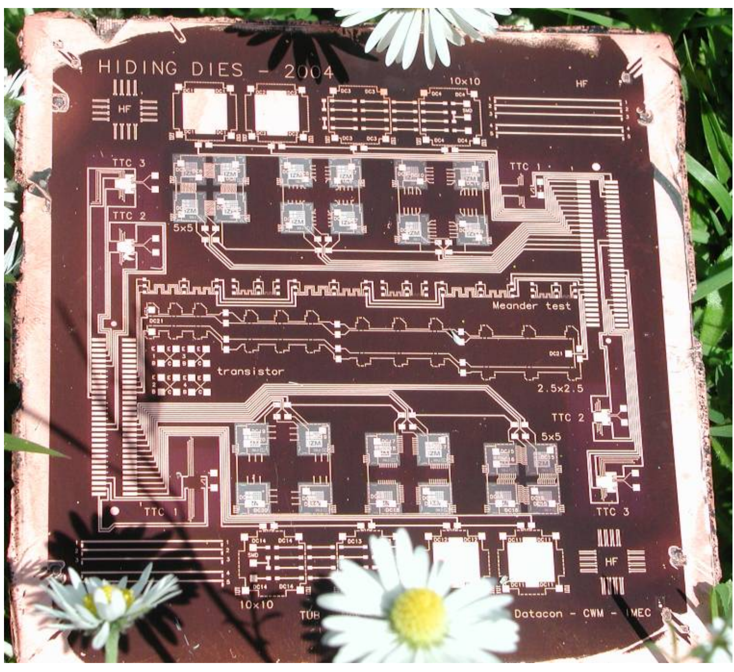
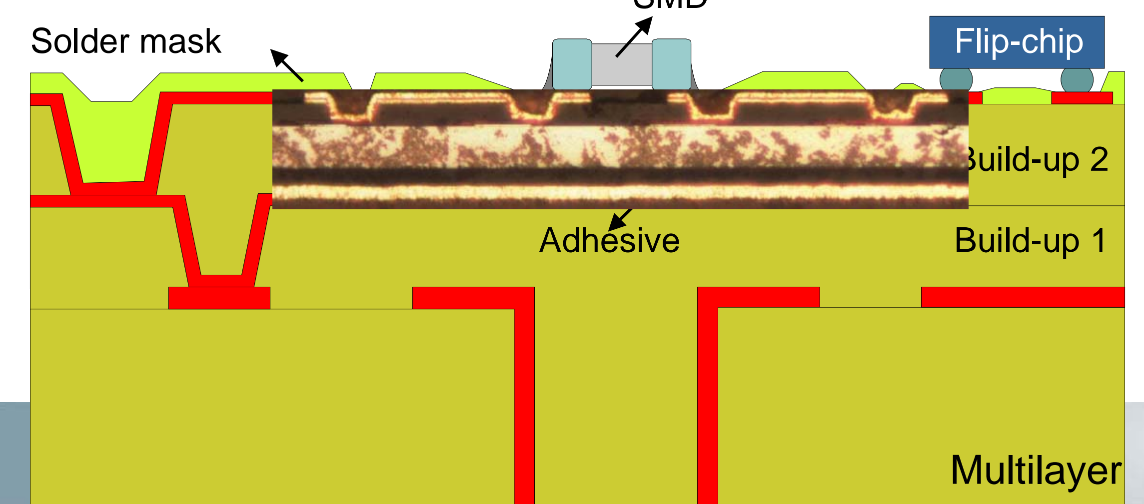
3D–SiP:
Example: PCB with embedded components

- Technology:
  - embedding of a 50 um thin die in a laminated PCB
  - interconnects made in PCB technololgy
- Applications:
  - very thin systems
  - flexible/foldable systems

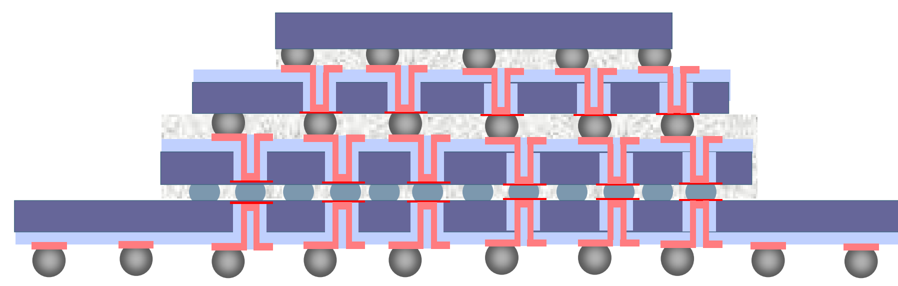


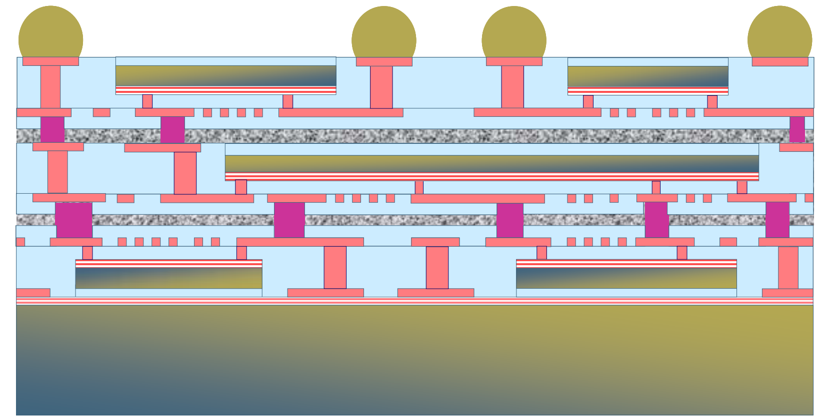


3D-WLP approach:
Wafer-level-packaging technology

- 3D interconnects:
  - realized at wafer level
  - processed on fully processed wafers
- Interconnect density:
  - 10-50/mm, 100–2.5k/mm^2
- Advantages:
  - no interference with process of individual layers
- Limitations:
  - not the highest interconnect density
- 2 technology approaches:
  - die stacking
  - ultra thin chip embedding

- Applications:
  - 3D sensor/imager systems allowing tiling/full buttability
  - thin flexible/stretchable systems





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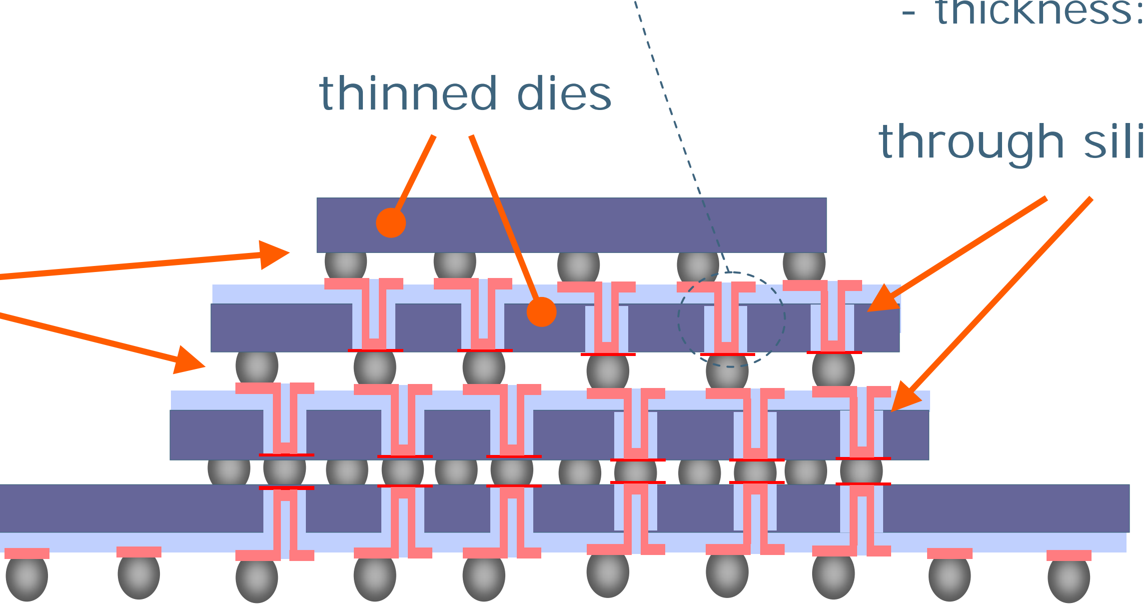
3D-WLP approach:
Process and specifications

- 3D-WLP chip stack process:
  - die/wafer thinning
  - through silicon vias (TSV)
  - micro-bumps
- Via last approach:
  - backside thinning
  - followed by TSV process
- Assembly:
  - micro-bumps

TSV specifications:

- pitch: 40-150 um
- diameter: 25-100 um
- thickness: 50-100 um



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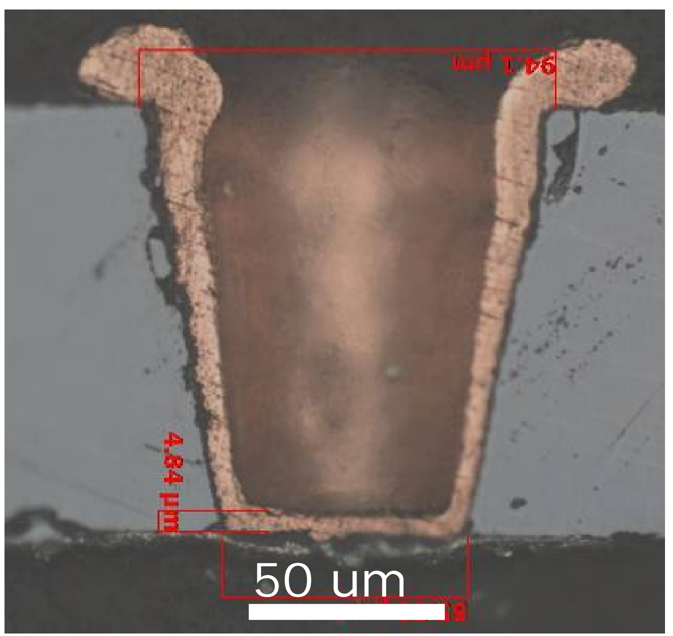
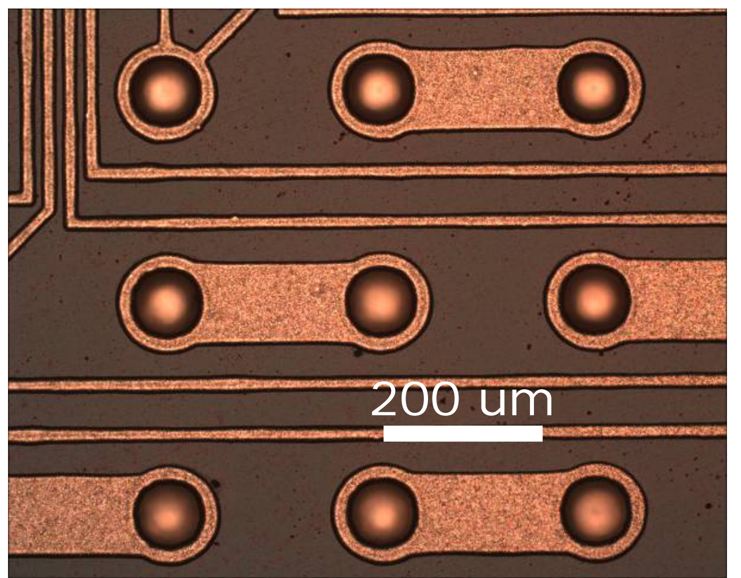
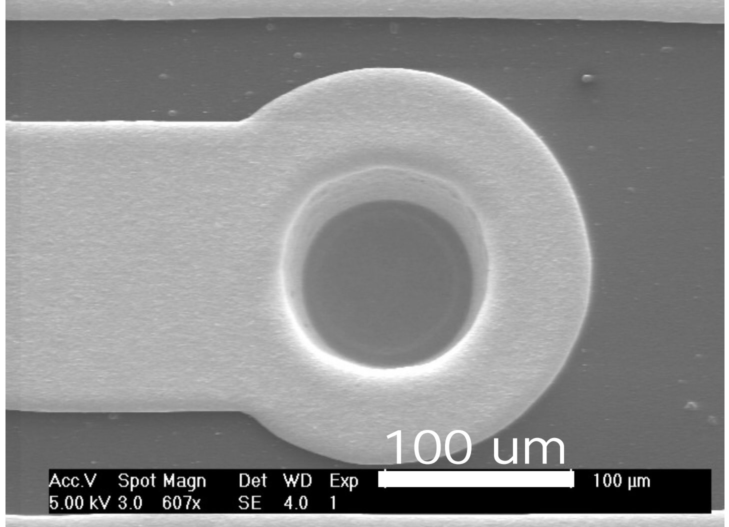
3D-WLP approach: Results

- Through wafer via:
  - resistance <= bond wire resistance

	3D-WLP via	1mm wirebond
R	20-30mΩ	~40mΩ *(25µm wire)*







D. Sabuncuoglu et al., ECTC 2007

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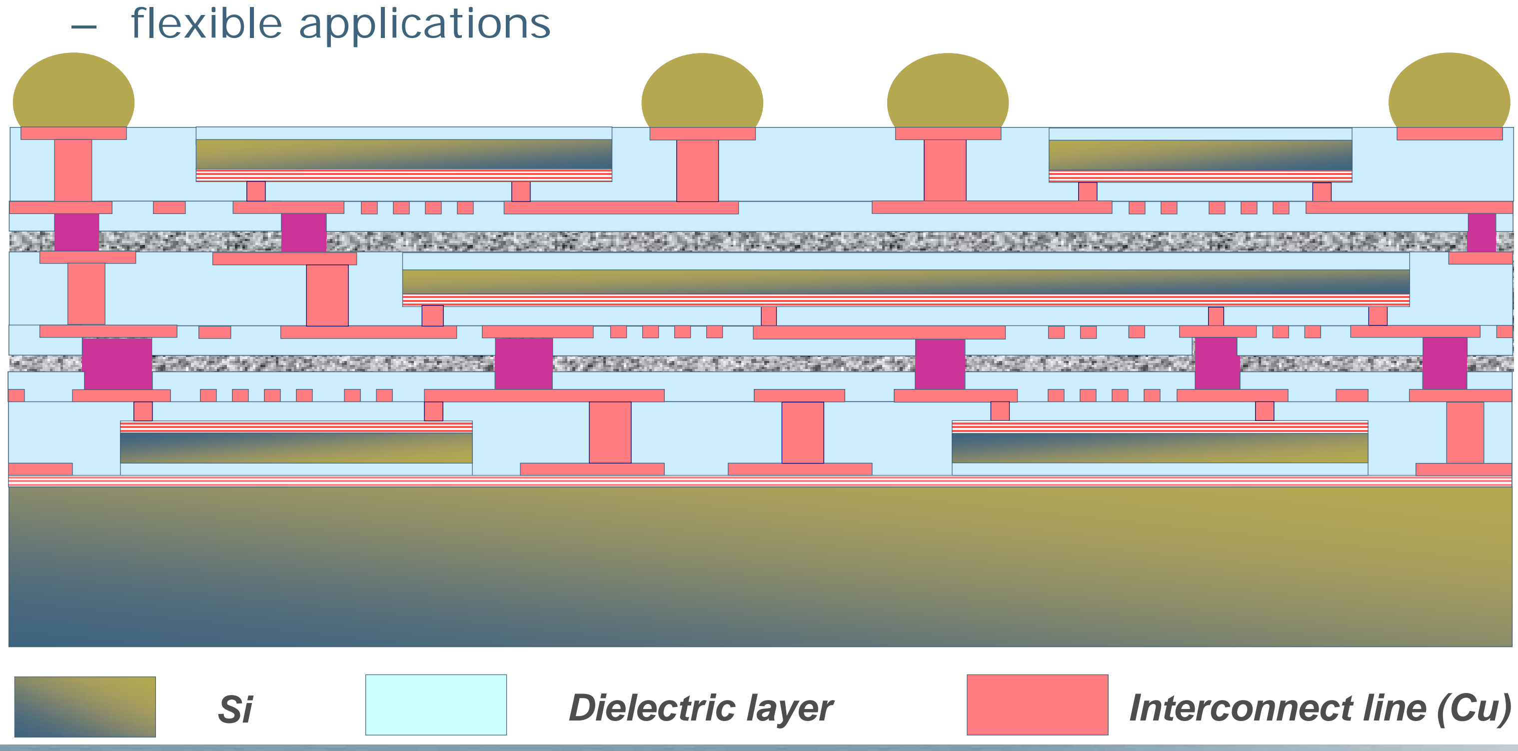
3D-WLP:
Ultra Thin Chip Embedding

- Approach:
  - ultra thin 10 to 20 μm thick die
  - embedded in a multilayer thin film build-up
- Advantages:
  - allows different die size
  - flexible applications



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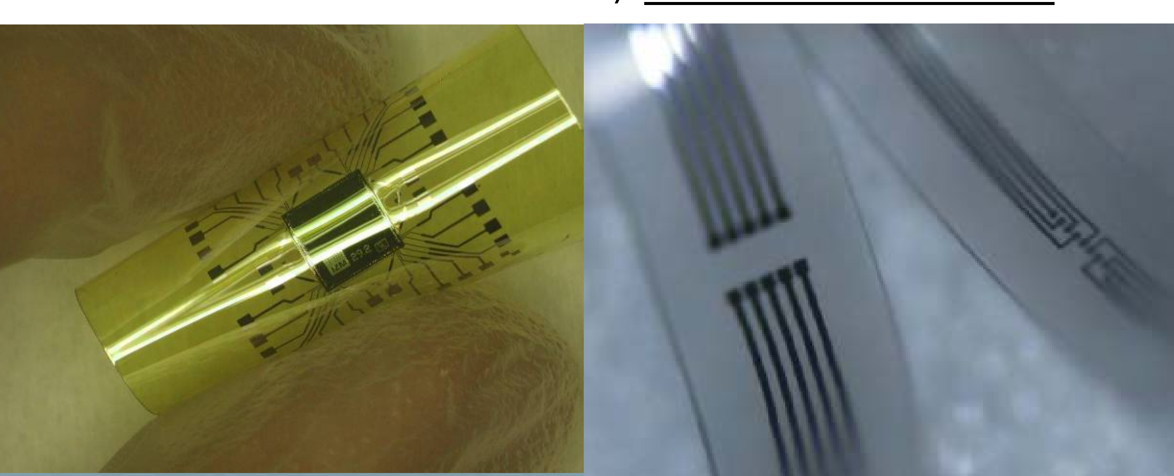
3D-WLP:
Ultra Thin Chip Embedding example

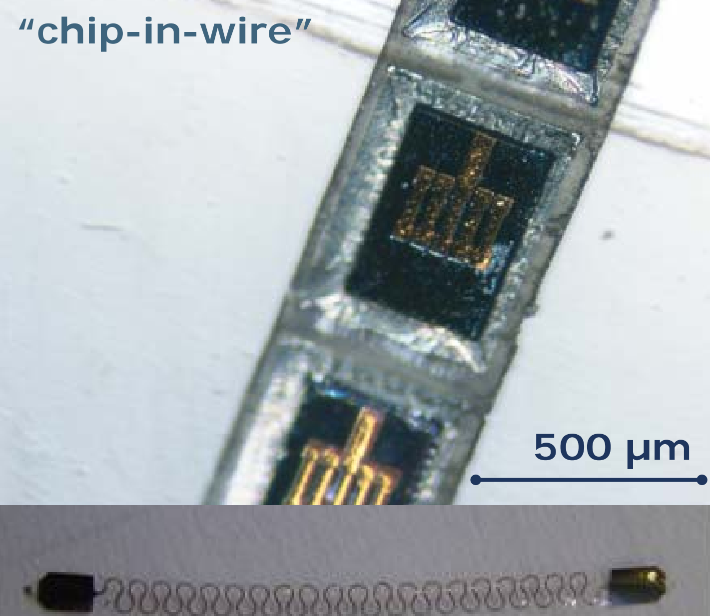
15 µm thin Si-die, transferred to a host substrate and electrically connected to that substrate

3D-WLP: Ultra Thin Chip Embedding:
Flexible electronic systems

- thin chip embedding on sacrificial layer
- release of sacrificial layer: chip-in-flex
- result: flexible/stretchable embedded electronics using e.g. Silicone dielectric

M. Vanden Bulcke et al., IEEE-EMBC 2006





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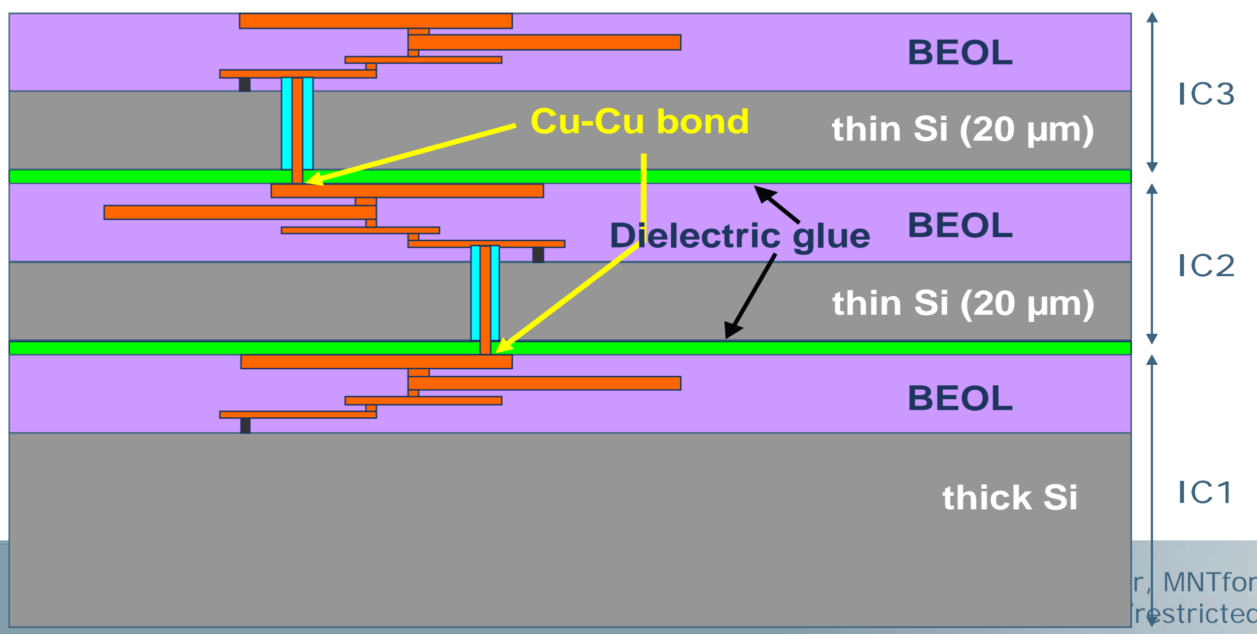
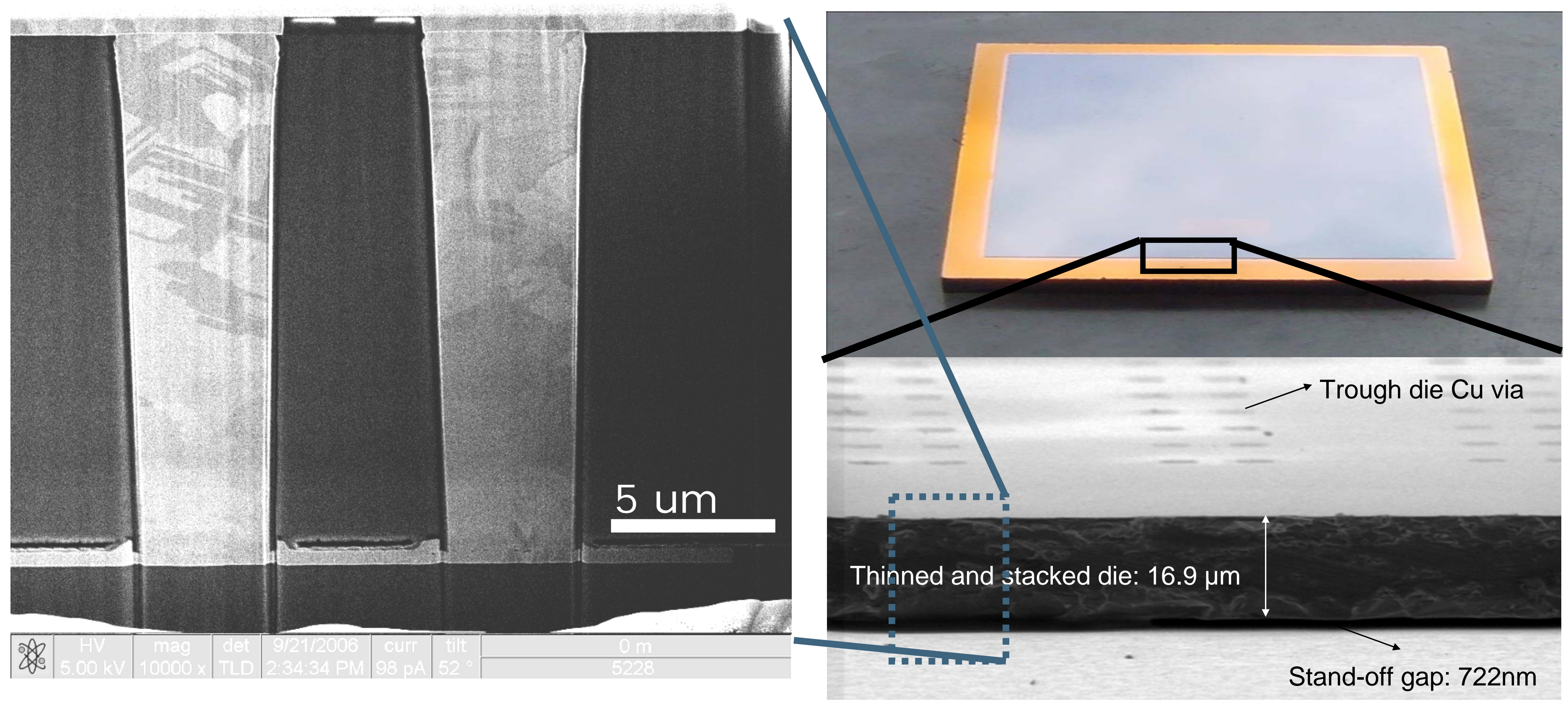
3D-SiC approach: Introduction

- Technology:
  - fabrication at device level, i.e. as a part of (CMOS) flow
- Specifications:
  - Si thickness: 10 – 20 um
  - via diameter: 3 – 5 um
  - via pitch: 10 um
- Applications:
  - CMOS/memory/imager stacking



3D-SiC approach:
Results

- Through Si vias:



B. Swinnen et al., IEDM 2006

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IMEC's 3D Interconnect R&D Roadmap

3D interconnect complexity

3D-SIC

3D-SIC 2-layer

3D-SIC n-layer

n-layer UTCS 3D-SIC

3D-WLP

Ultra Thin Chip embedding 2-layer UTCS

Chip-in-Flex UTCF

n-layer UTCS

n-layer UTCS 3D-WLP

Face-to-face Flip-chip

Face-to-face Micro-bumps

3D-WLP 2-layer Through-Si

3D-WLP n-layer

3D-SIP

Stacked-IC Package

3D-SIP BGA

3D-SIP CSP

3DSIP Die-in-board

2004 2005 2006 2007 2008 2009

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Positioning different 3D approaches

	3D-SIP	3D-WLP		3D-SIC
Technology	Package interposer	WLP, Post-passivation		Si-foundry, Post FEOL
3D interconnect	Package I/O	UTCS Embedded die	Si-through vias	Si-through "Cu nail" vias
Intercon. Density	'package-to-package'	'around' die	'through' die	'through' die
Peripheral	2 - 3 /mm	10 - 50 /mm	10 - 25 /mm	25 -100 /mm
Area-array	4 - 11/mm^2	100 -2.5k/mm^2	16 - 100/mm^2	400-10k/mm^2
3D Si Via pitch	-	-	40 – 100 µm	< 10 µm
3D interconnect pitch	300 – 500 µm	20 – 100 µm	-	-
3D Si Via diameter	-	-	25 - 100 µm	1 - 5 µm
Die thickness	> 50 µm	10 - 20 µm	50 - 100 µm	10 - 20 µm

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  - BIB
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  - Bold
  - RelaxD
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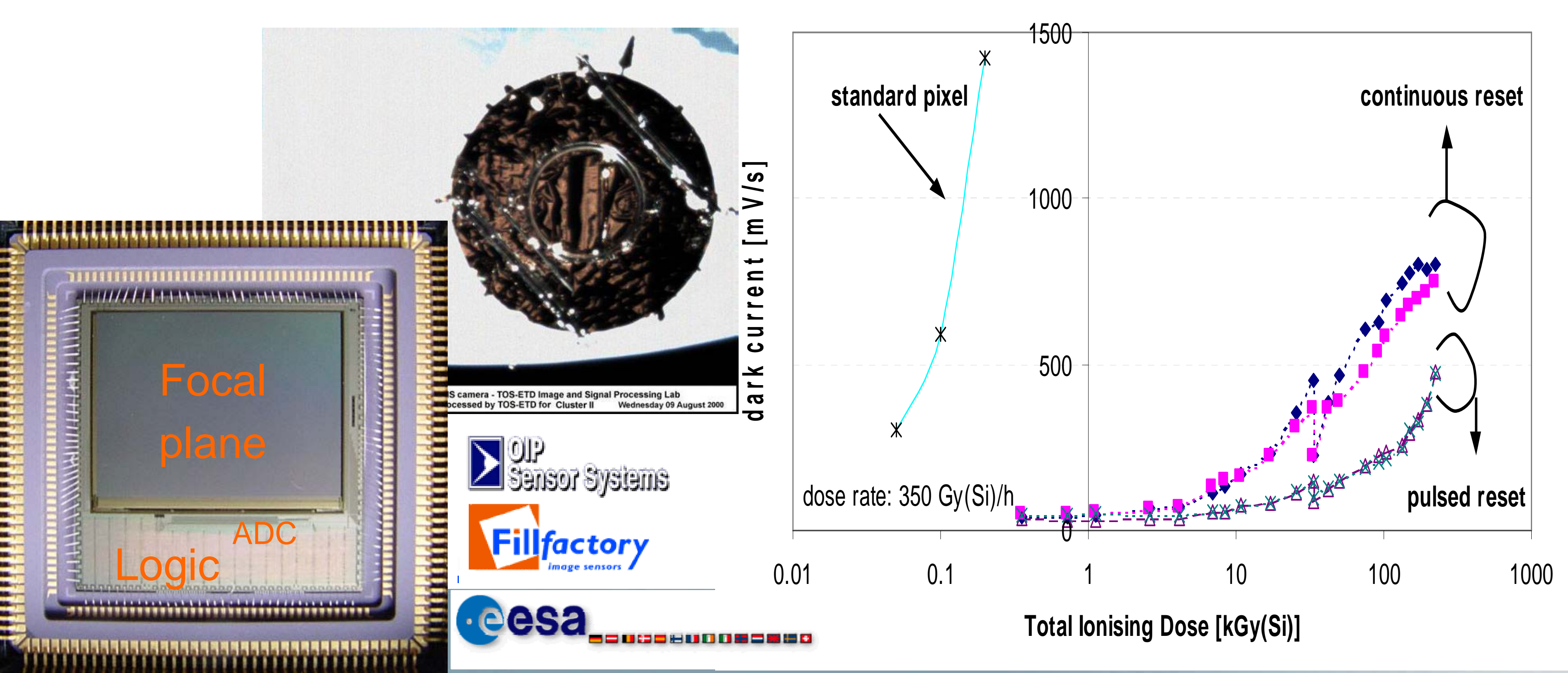
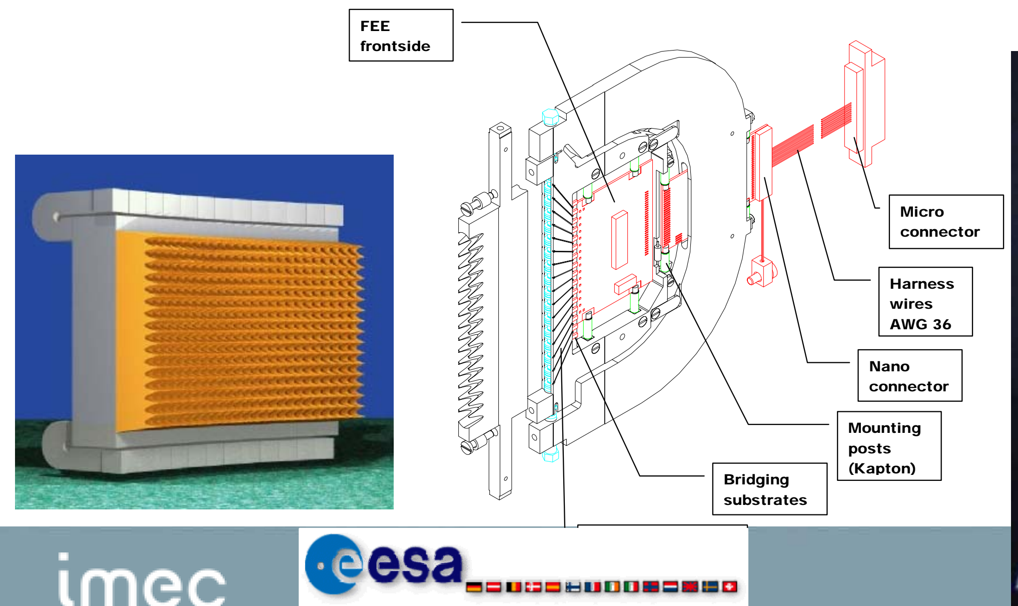
Custom analog design: radiation tolerant

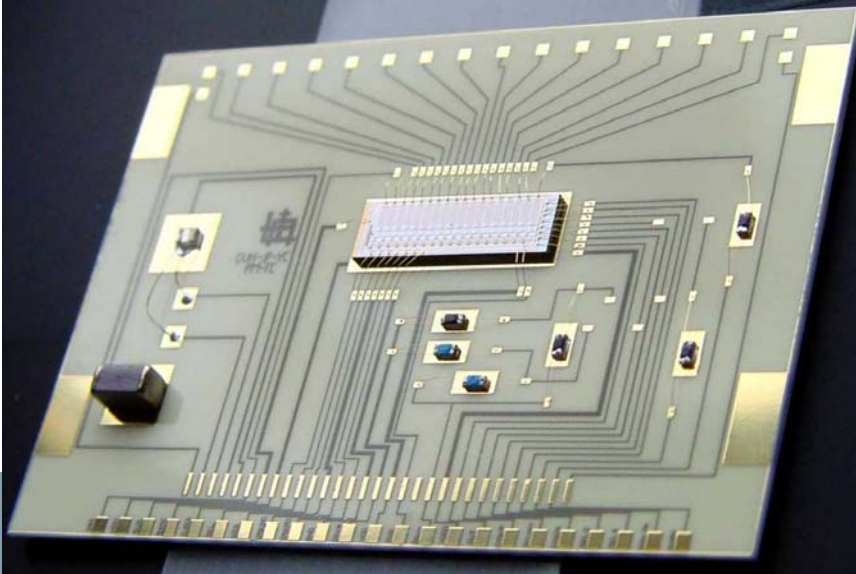
- Radiation-tolerant analog ROIC design:
  - nMOS pixel design (using 0.7μm Alcatel Microelectronics Technology)
  - 2-3 orders of magnitude less sensitive to total dose
- Example: Flight Model IRIS3
  - CMOS camera for imaging in space



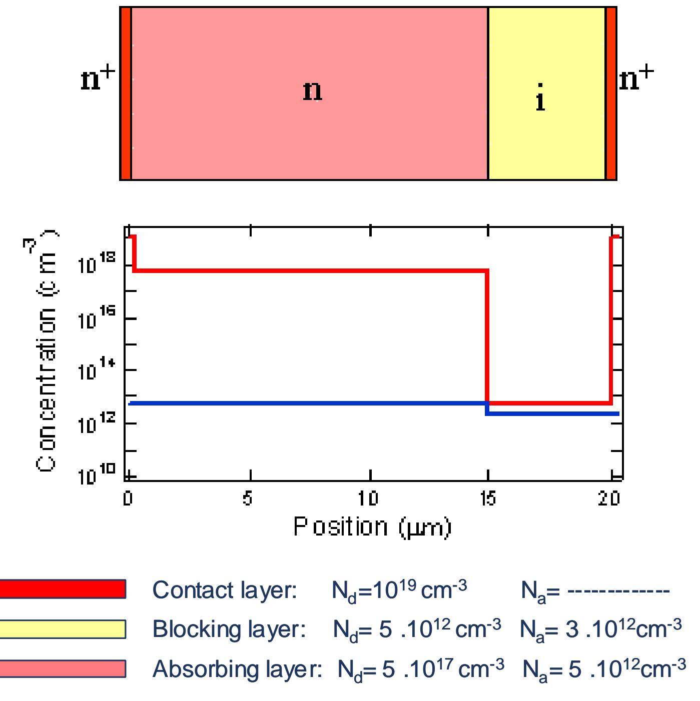
Custom analog design: cryogenic ROICs

- Analog design for 4 Kelvin operation:
  - special design to avoid anomalous behavior of standard CMOS < 20 K
- Example: PACS-CRE: ROIC for a far-infrared detector array
  - ~ 200 qualified assemblies delivered to ESA
  - Herschel satellite to be launched in 2008
  - very low noise: measures 10 fA – 100 pA
  - very low power consumption: 80 μW
  - irradiation tolerant @ 4 K

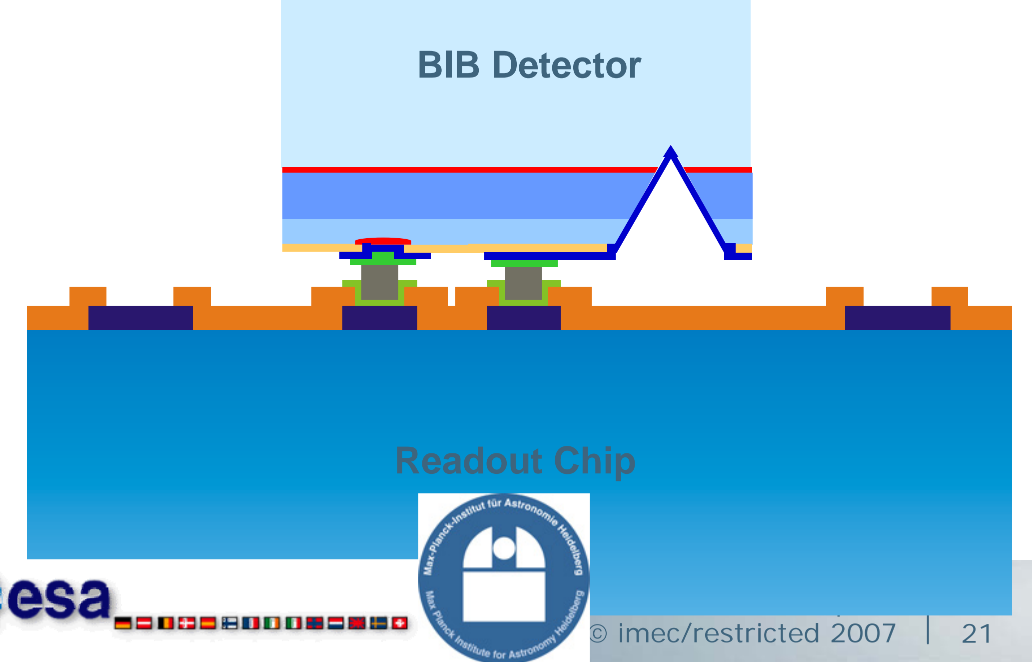




Space applications:
Cryogenic BIB detector



- Far IR detection: 6 – 18 um wavelength
- Si:As Blocked Impurity Band (BIB) detector array operating at 4 K
- Backside illuminated through high resistivity Si



- Hybridization on cryogenic ROIC using In bumps

esa

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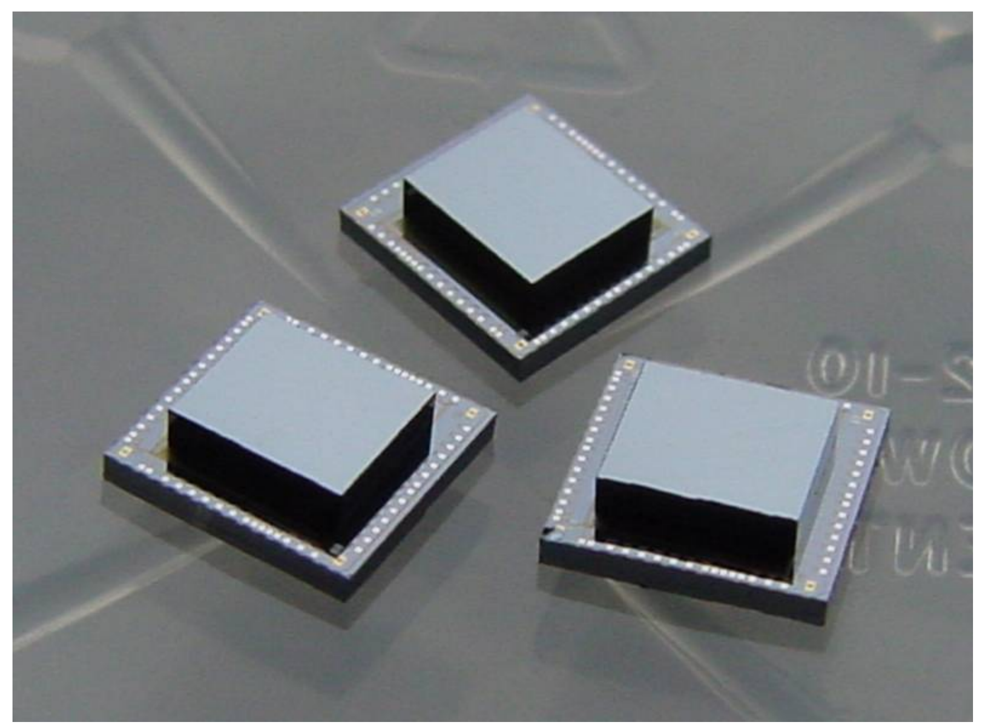
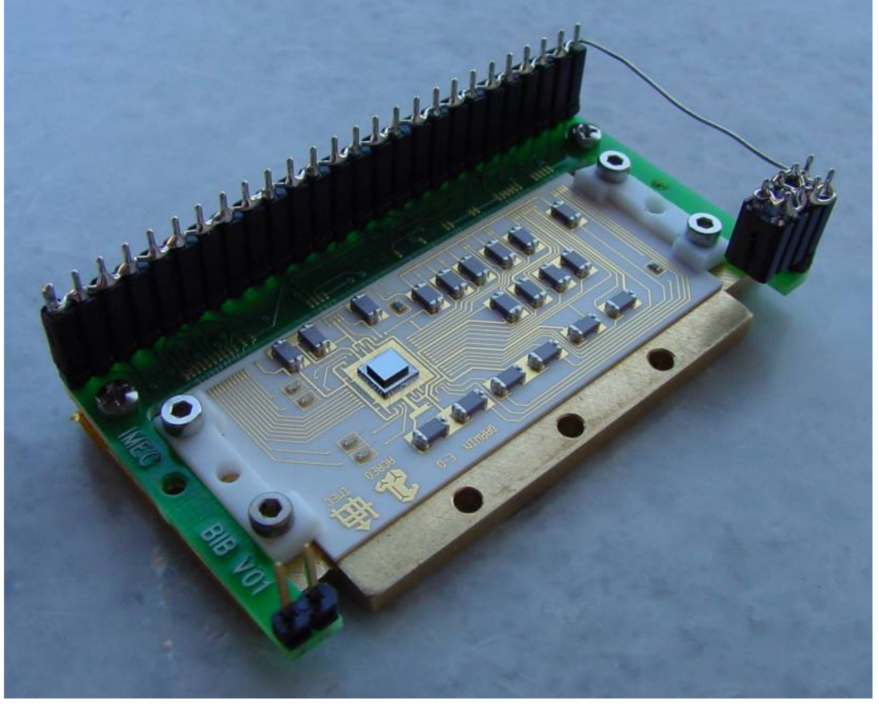
Space applications:
Cryogenic BIB detector

- Linear array: 2x 88 pixels
- Pitch: 30 um
- Application:
  - DARWIN mission: search for exoplanets





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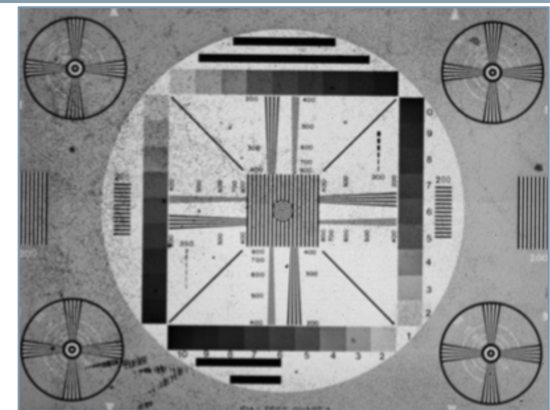
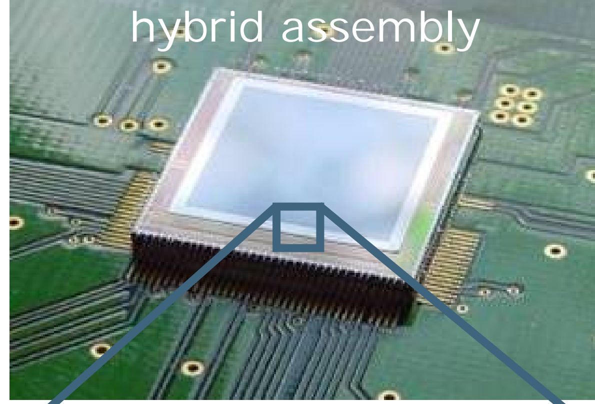
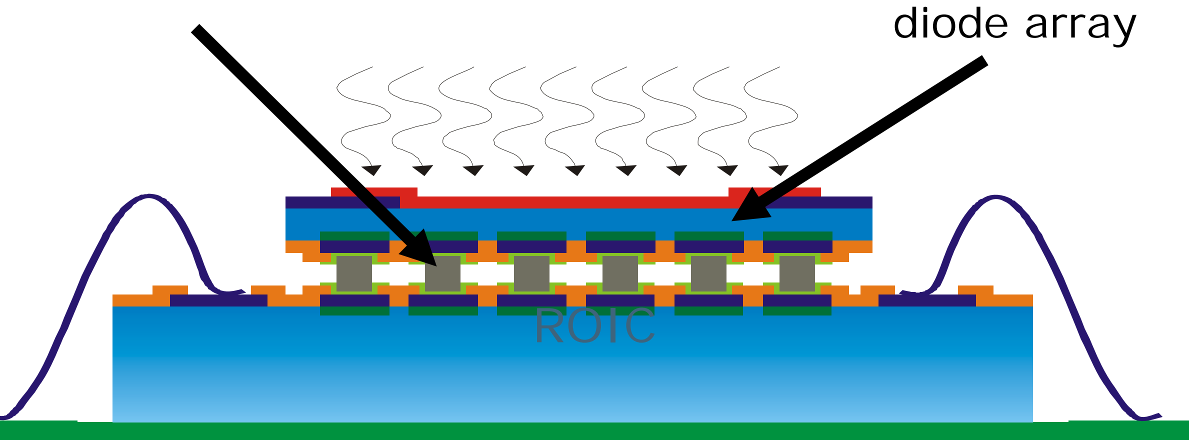
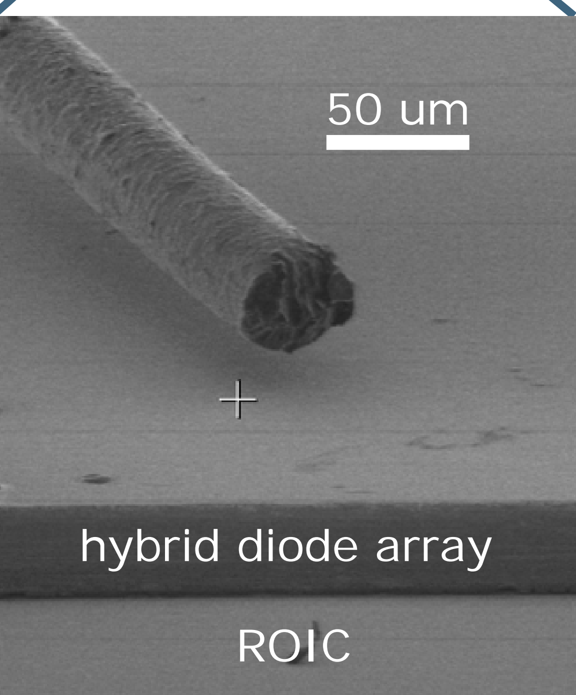
Space Applications:
Backside illuminated CMOS imager

- Specifications:
  - 22.5 um pitch
  - 1 Mpixel
  - thinned down to +/- 35 um
  - In bump yield ~ 99.95 %









K. De Munck et al., IEDM 2006

Space applications:
Backside illuminated CMOS imager

- Excellent QE:
  - > 80 % from 400 – 850 nm wavelength

Quantum efficiency [%]

Wavelength [nm]

simulation: ARC limited

measurement

simulation: ARC + implant

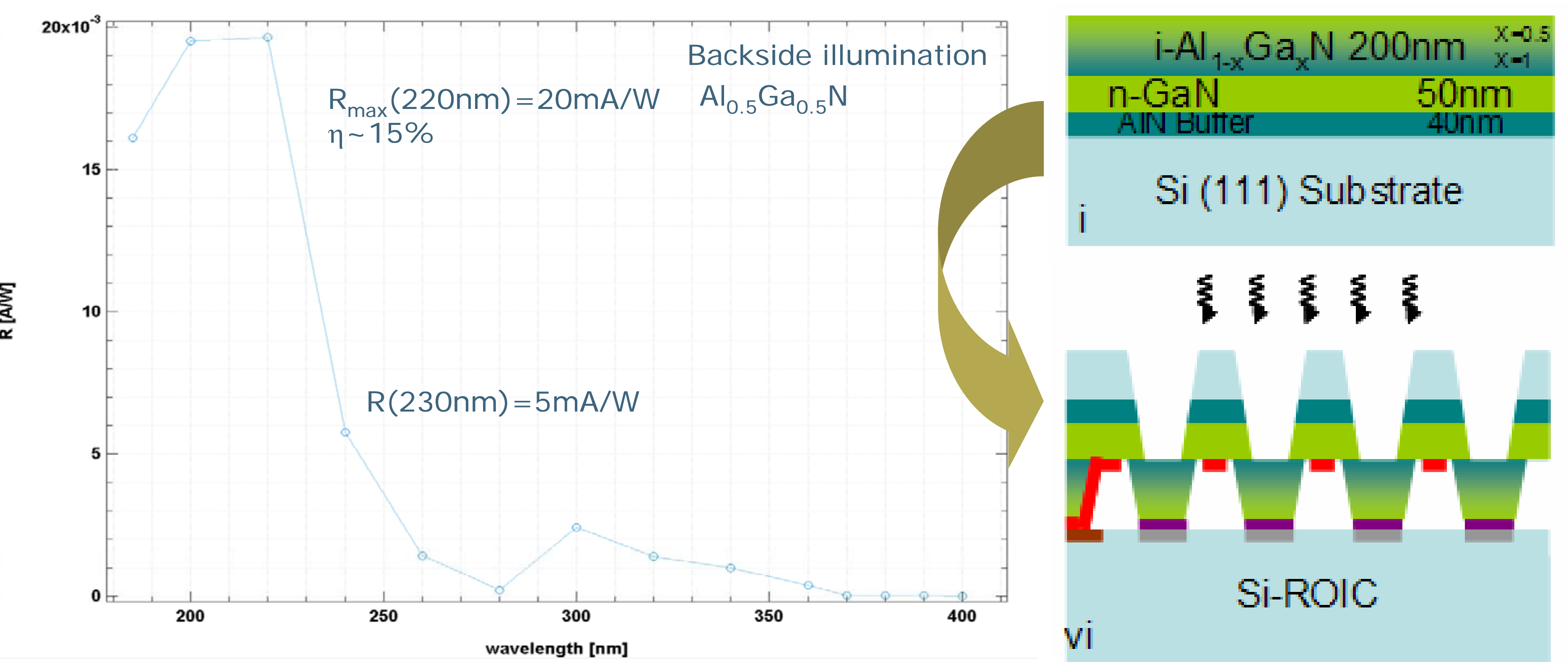
simulation: plain Si

0 nm
15 nm
0 nm
10 nm
15 nm
0 nm
10 nm
15 nm

dead layer thickness

Space applications:
BOLD: 2D (X)UV detection

- AlGaN Schottky diode detector
- Backside illumination possible thanks to wafer thinning, thin layer transfer, through Si optical access holes
- Result: factor 10 increase in sensitivity @ 200 nm wavelength
- Will be hybridised on 2D ROIC with 10 um pitch



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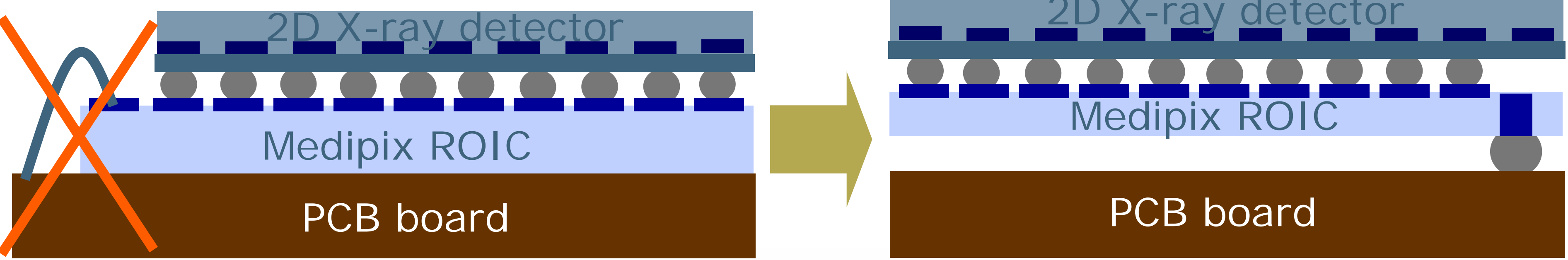
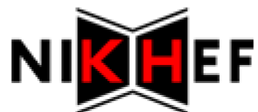
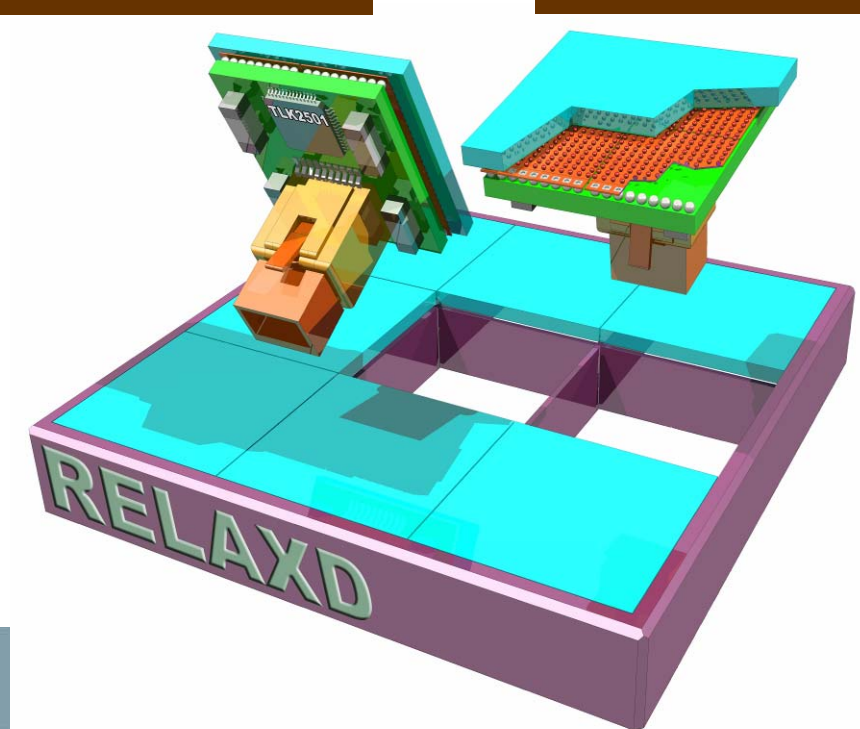
Space applications:
RelaxD: tilable X-ray imagers

- 3D integration of 2D X-ray imager
- tiling of modules for large area detection

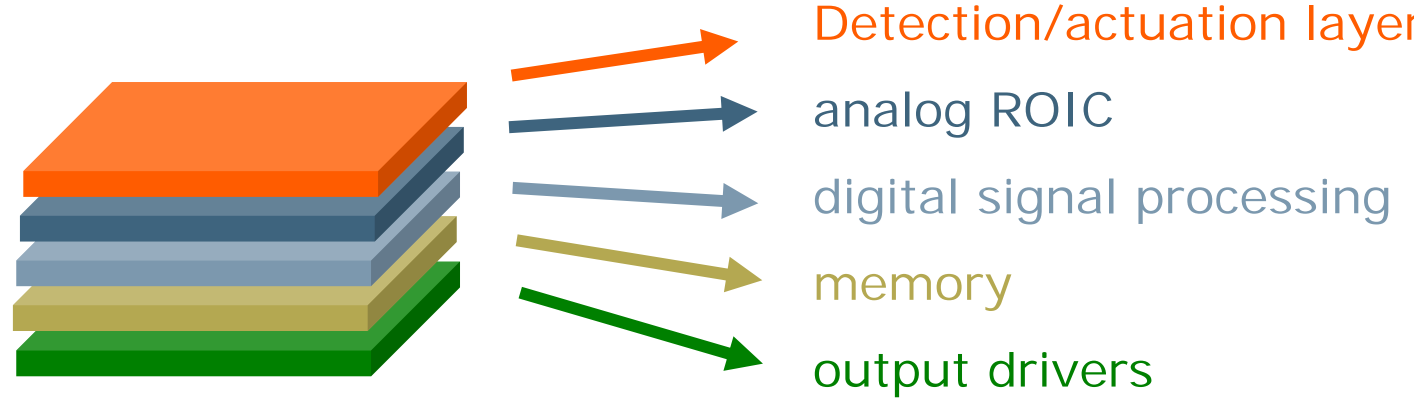






Conclusions & outlook

- 3D integration technology is developing fast
- It will allow manufacturing of imager systems:
  - highly **miniaturized**, i.e. very small in vertical dimension
  - **tilable**, i.e. enabling large area detection with minimal non-sensitive area
  - **complex** microsystems using high density 3D interconnects between different intelligent layers



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