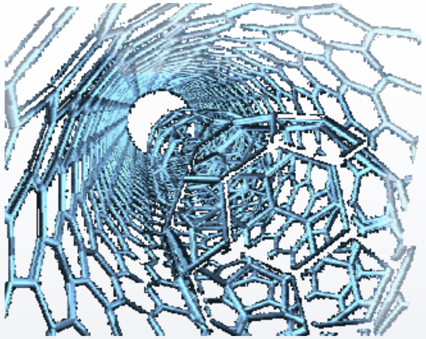
Carbon nanotube based transistor: high frequency performance and applications



H. HAPPY
Institute of **E**lectronic **M**icroelectronic and **N**anotechnology

A. LE LOUARN, IEMN
G. DAMBRINE, IEMN
V. DERYCKE, CEA
J.P. BOURGOIN, CEA

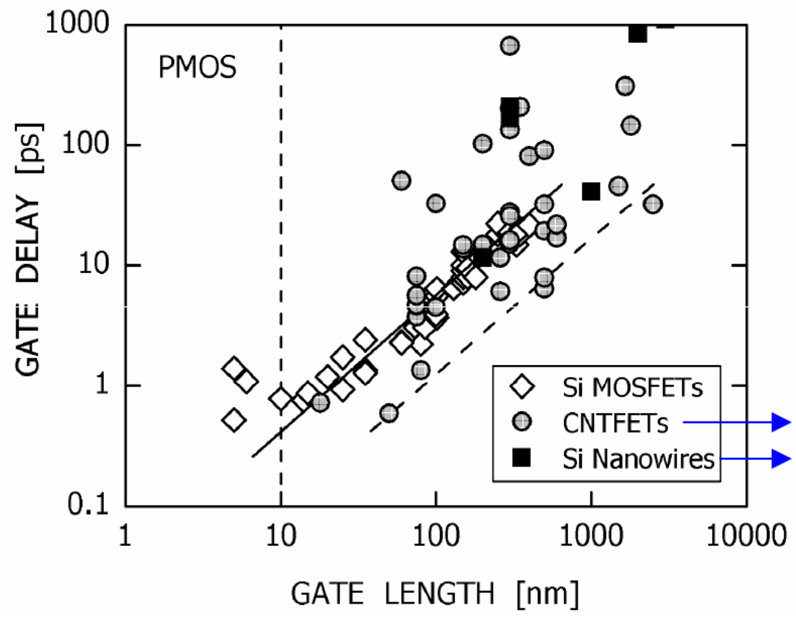
ESA Workshop:
Round table on micro/nano technologies for space

OUTLINE

- Nanotubes based-transistors technology: Status
- Nanotubes based-transistors HF performance: Status
- Microwave measurements of CNTFET:problematic
- High f_T CNTFET
- Conclusion and perspectives

CNT for transistor: Why?

Conduction	Metallic or semiconducting
Energy gap	Eg [eV] = 0.9/d[nm]
Electrical transport	Ballistic, $\lambda_\varepsilon > 1$ μm
Maximum current density	10^{10} A/cm²
Diameter	1 - 50 nm
Length	Up to mm
Thermal conductivity	6000 W/(Km)
Young Modulus	Ca 1 TPa
Fermi Velocity	8 10^5 m/S



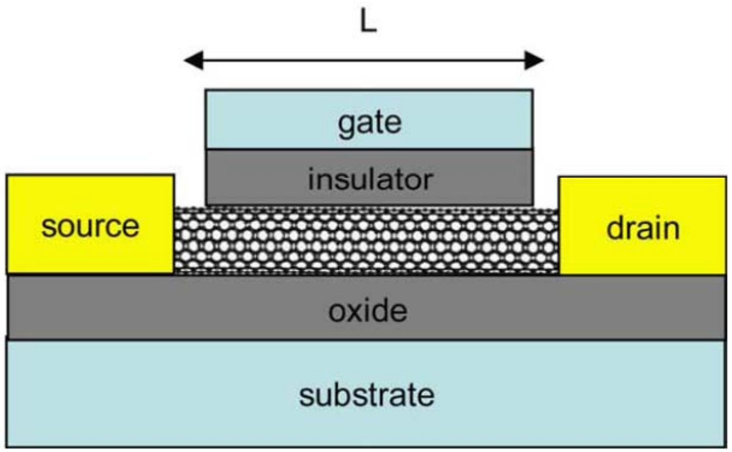
Robert Chau, Intel Proc. Proc. of DRC 2006

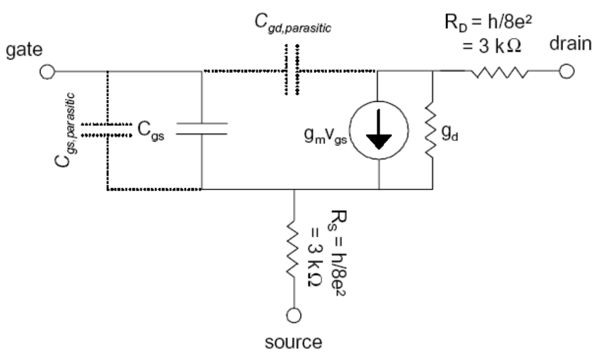
- The CNTs open many prospects for applications in the field of electronics in term of integration, and new functionalities;

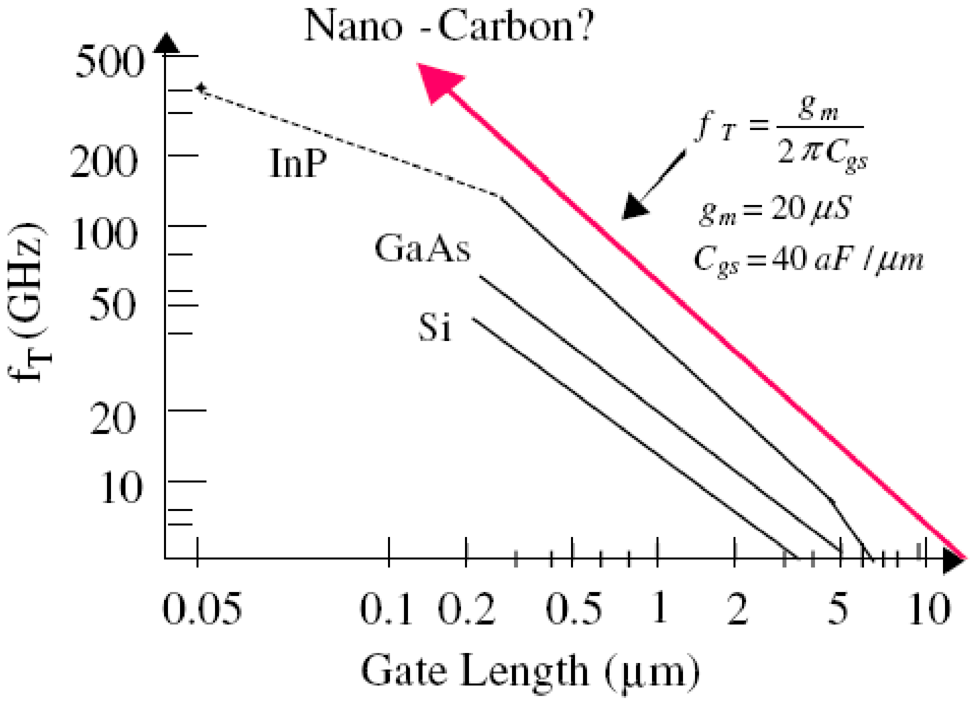
- their electronic (electron/hole transport) and mechanical properties open ways for low cost high performance electronics (for instance electronic on flexible substrate).

CNTFET for HF: Why ?

Theoretical HF performance



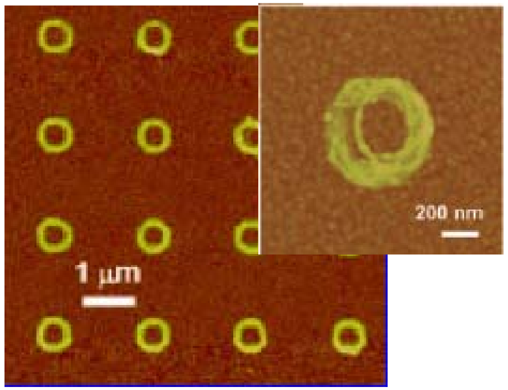




P. Burke AC performance of nanoelectronics: towards a ballistic THz nanotube transistor; Solid-State Electronics 48 (2004) 1981–1986

Some conditions for the development of CNTs in electronics

- ❑ Material control (diameter, length, SC vs M)
- ❑ Hybridation onto CMOS or with flexible electronics technologies
- ❑ Development of cheap handling techniques



Mirkin, Smalley, Schatz et al PNAS 2006

Wet self-assembly techniques

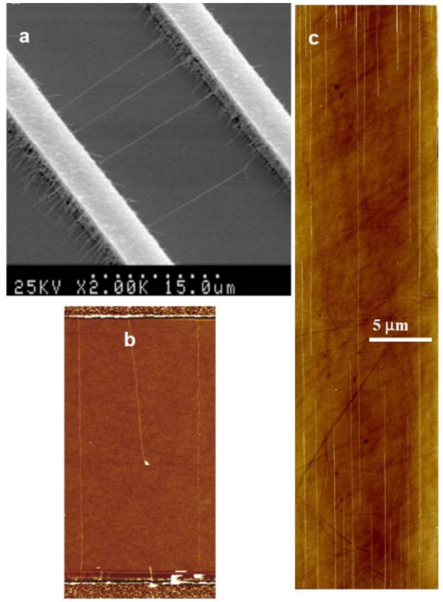


Figure 3. Oriented growth of SWNTs. (a) Aligned suspended SWNTs grown in an electric field. (b) Aligned SWNTs grown on SiO_2 substrate in an electric field. (c) Aligned SWNTs grown by PECVD on crystalline quartz substrate and aligned along the quartz crystal lattice.

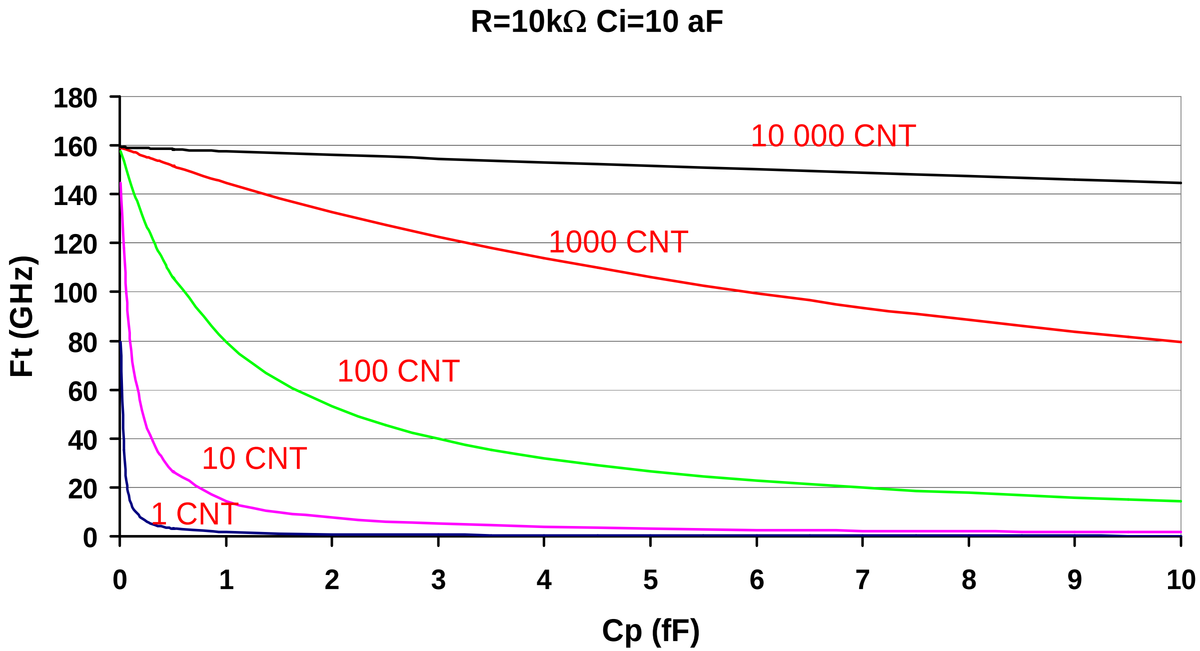
G. Zhang et al. / Proc. of IEDM 2006
Stanford University, Stanford CA 94305, U.S.A;

Localized growth

Some conditions for the fabrication of CNT-based-transistors for High frequency transistors

$$f_T \approx \frac{n}{2\pi\, R\,(nC + C_p)} \quad with \quad R = \frac{h}{4e^2} + 2R_c > 6k\Omega$$

$$C \approx few\ aF; \quad C_p \approx few\ fF$$



- ❑ Strong influence of **parasitic**
- ❑ **Parallelization** seems to be the solution to increase the current level and to screen the parasitic...

Needs technological improvements in term of:

- ❑ CNTs **placement**
- ❑ SC/Metal **Separation**

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CNTs placement by di-electrophoresis process:

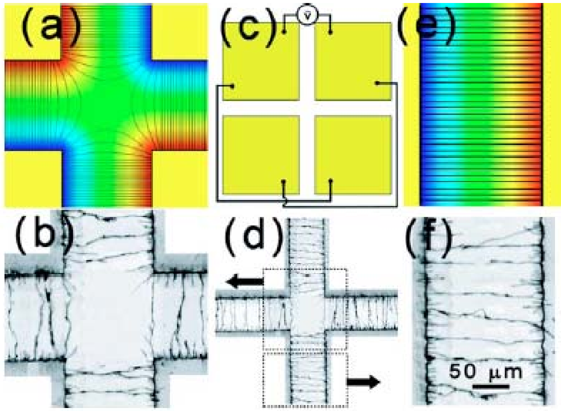


FIG. 1. (Color online) (a) "Cross" gap defined by four rectangular electrodes. (c) The diagonal pairs of electrodes are electrically connected, and between the pairs an ac voltages is applied. Calculated electric field lines and equipotential contours in color are shown in (a) for the central region and (e) away from the central region. The actual assemblies of nanowires under $V_{ac}=5$ V and $f=1$ MHz are shown in (d) with the enclosed areas enlarged in (b) and (f).

NW illustration

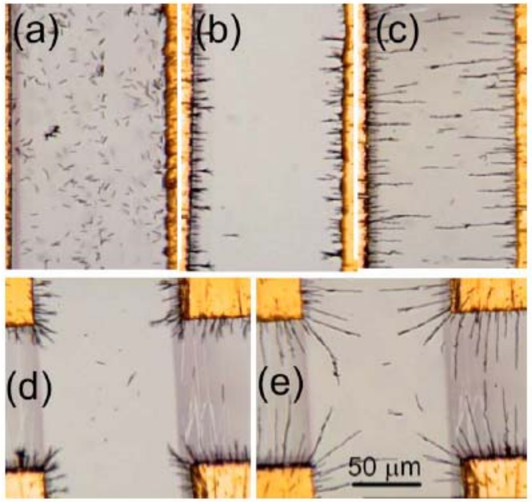
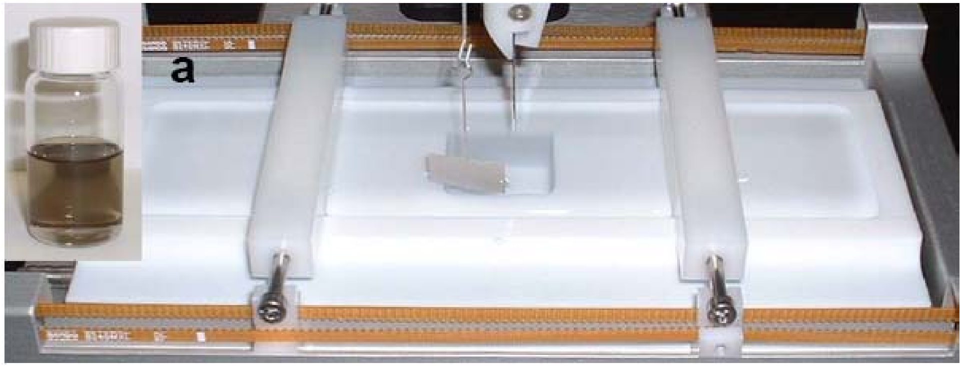


FIG. 2. (Color online) Photographs of nanowire assemblies under electric fields of (a) 2 V dc; [(b) and (d)] 10 kHz, 7.5 V ac; [(c) and (e)] 0.5 MHz, 7.5 V ac.

D. L. Fan et al. Appl. Phys. Lett. **89**, 223115 2006
Johns Hopkins University, Baltimore, USA

CNTs placement by Langmuir Bloddget method



G. Zhang et al. / Proc. of IEDM 2006
Stanford University, Stanford CA 94305, U.S.A;

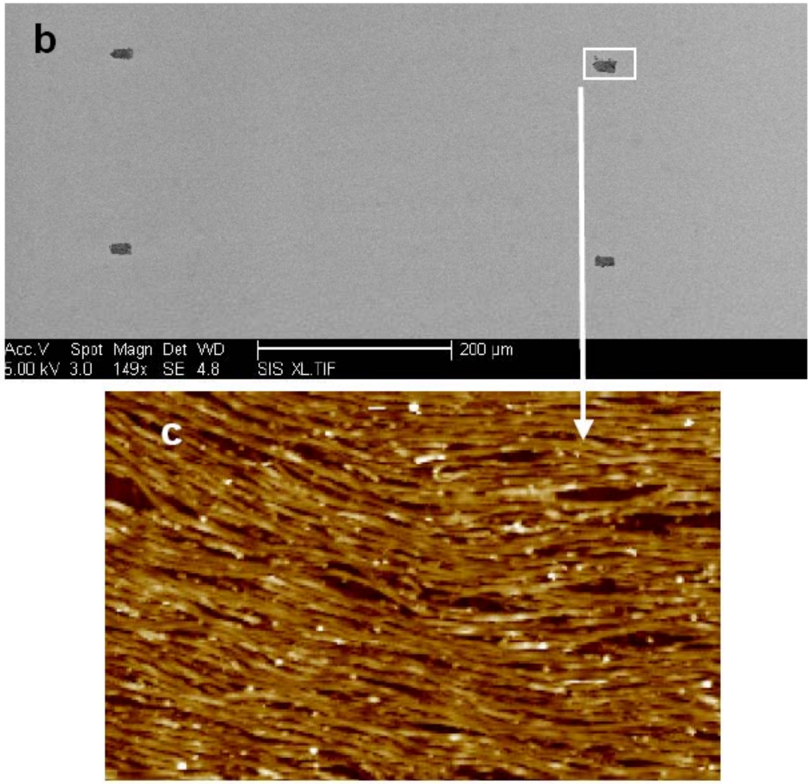


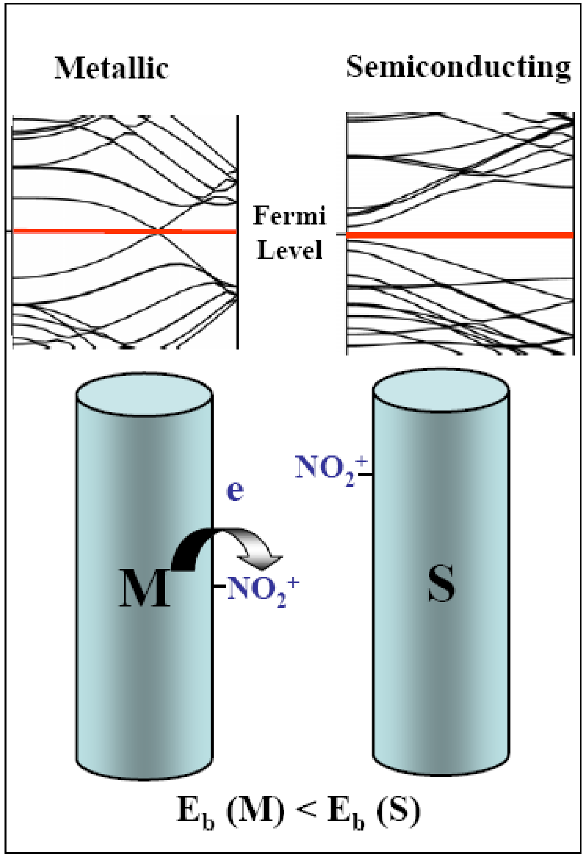
Figure 5. Langmuir bloddget LB assembly of SWNTs. (a) A photo of a LB trough. Inset: a SWNT suspension in DCE. (b) A SEM image showing a patterned SWNT LB film on SiO_2. (c) A zoom-in AFM image of SWNTs LB film in a patterned region.

SC / Metal CNTs selection:

Chemical solutions:

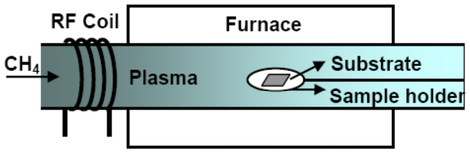
K.H. An et al. / Current Applied Physics 6S1 (2006) e99–e109
Sungkyunkwan University, Republic of Korea

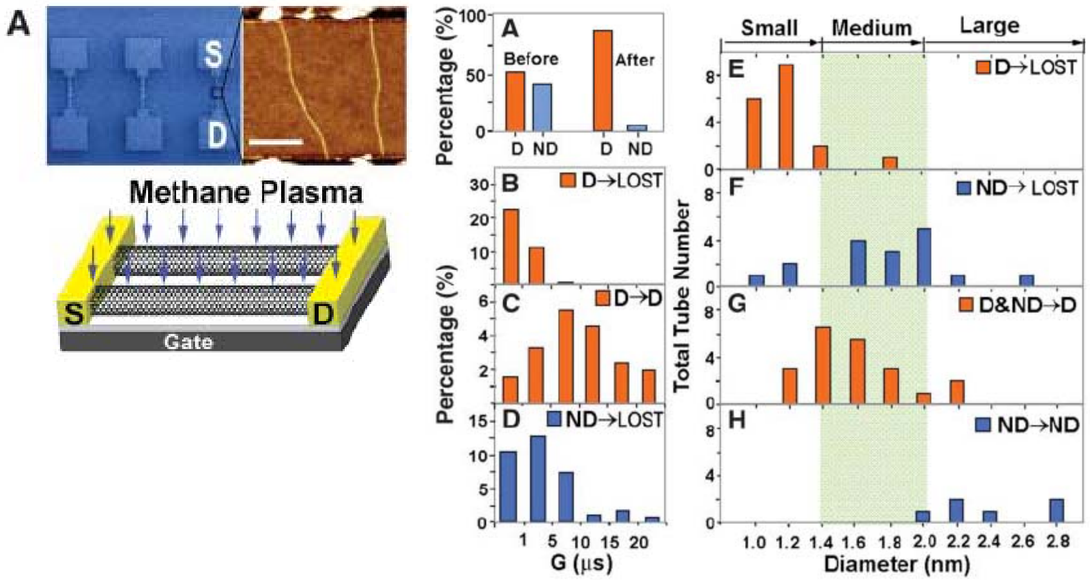
C. Ménard-Moyon et al.
CEA-Saclay; Univ. of Montpellier; LSB Uni. Strasbourg
JACS 2006, 128, 6552-6553

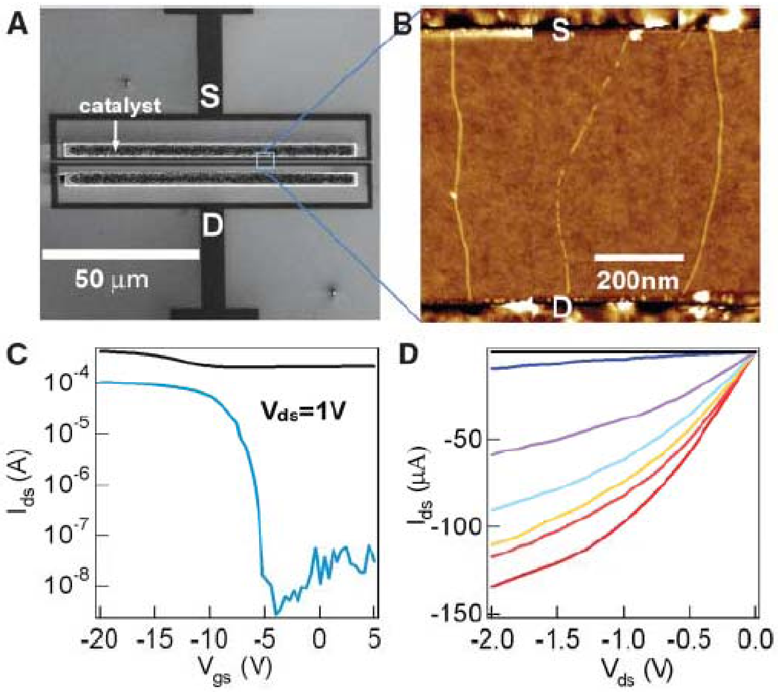


SC / Metal CNTs selection

Selective etching: Plasma hydrocarbonation reaction







(Guangyu Zhang *et al*. 10 NOVEMBER 2006 VOL 314 SCIENCE)

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CNTFET HF Performance: Status

State-of-the-art

HF measurements: heterodyne & homodyne (detection) mixers, other…

- 100 MHz IBM, 2004 (detection)
- 580 MHz IBM, 2004 (detection)
- 2,6 GHz Burke et al, Irvine, 2004 (cryogenic resonator)
- 50 GHz McEuen et al, Cornell, 2005 (heterodyne mixer)
- 23 GHz Pesetski et al, Northrop Grumman, 2006 (heterodyne mixer)

Lot of works with frequency increase but no actual demonstration of the active nature of CNTFETs…

HF transistor measurements (S-paramters; HF gain)

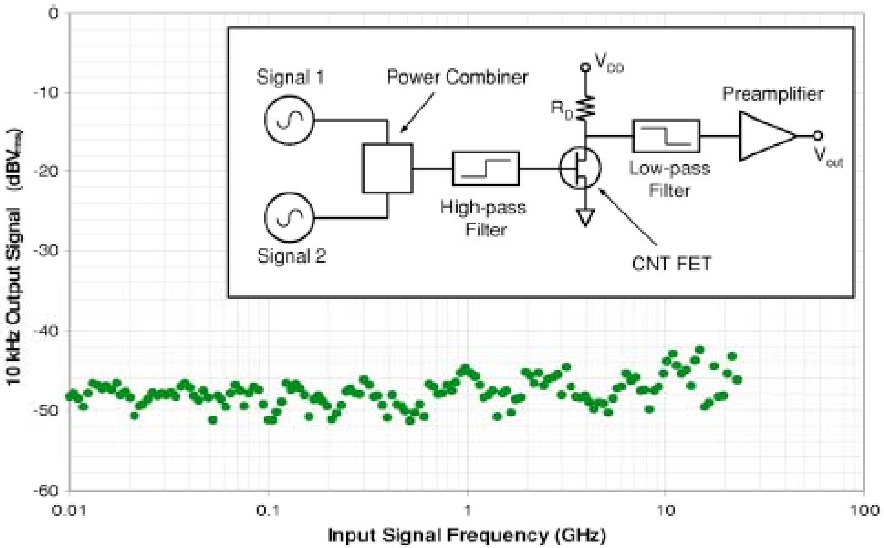
Very few reports

- Kim et al, Purdue, MTT symposium, I.M.S. 2005 ***ft*=2.5 GHz**
- Bethoux et al. EDL, VOL. 27, NO. 8, AUGUST 2006 LEM/IEMN ***ft*=8 GHz**
- Narita et al. NEC research Lab. TNT2006, 2006 ***ft*=10.3 GHz**

CNTFET HF Performance: Status

Heterodyne Mixer: examples

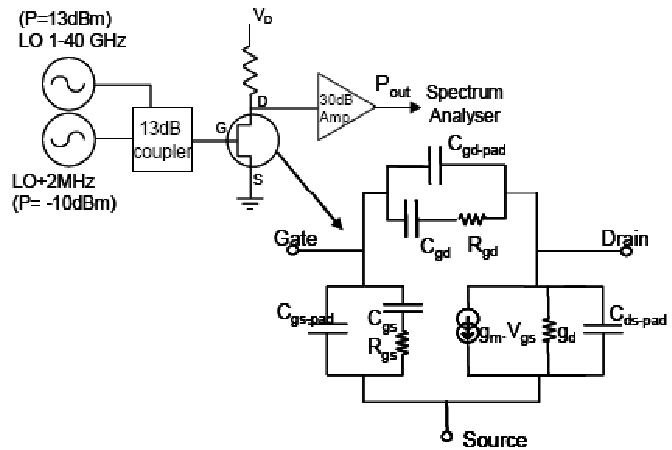
10 MHz < f_{AC} < 23 GHz IF=10 kHz

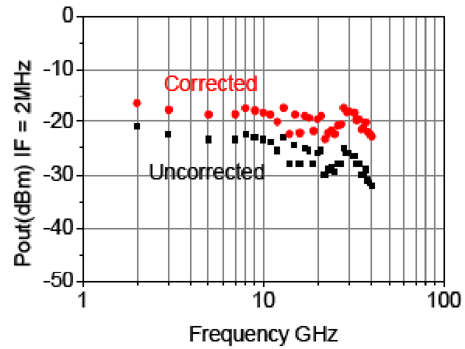


Architecture: « Top gate »
CVD NT d~1.2nm
L_g=1µm
t_{ox}=220nm (Si_3N_4)
Quartz substrate

Aaron A. Pesetski et al.
APPLIED PHYSICS LETTERS **88**, 113103 2006
Northrop Grumman Corporation,

2 GHz < f_{AC} < 40 GHz IF=2 MHz



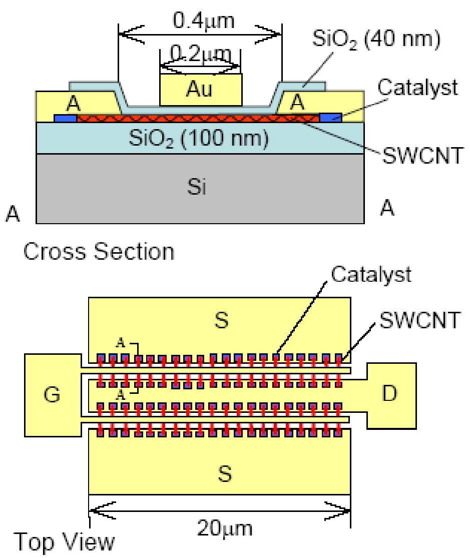


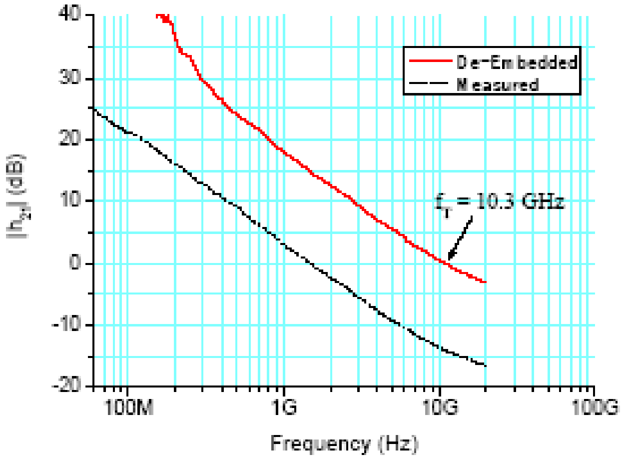
Architecture: « Back gate »
Self-assembling deposition (10 NTs /µm)
L_g=200 nm (recouv. 50nm)
t_{ox}=2nm (Al_2O_3)
SOI HR substrate

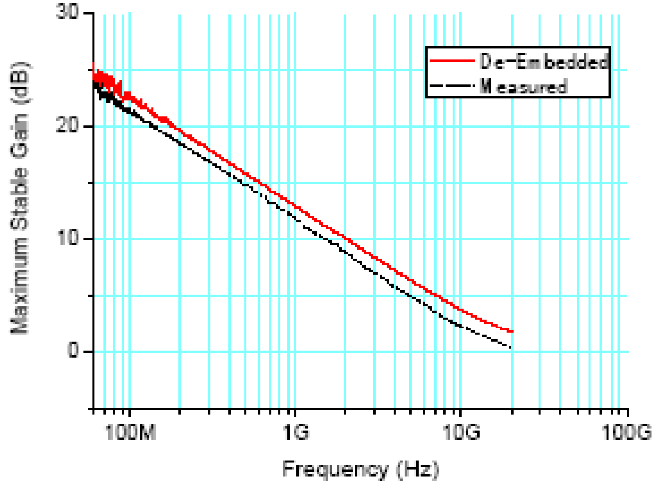
JP Bourgoin et al. Proc. of IEDM 2006
CEA LEM - IEMN

CNTFET HF Performance: Status

Active Transistor HF measurement: example







Architecture: « Top gate »
NTs CVD (10 NTs /µm)
L_g=200 nm
t_{ox}=40nm (SiO_2)
W= 2 doigts x 20 µm
SOI HR substrate

gm ~ 220 µS

Ft ~ 1.5 GHz extrinsic

Ft ~ 10 GHz intrinsic

MSG ~ 13 dB à 1 GHz

(>3dB à 10 GHz)

Narita et al. NEC Research Lab. TNT2006, 2006

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CNTFET HF measurements

CNTS or CNTFETs HF measurements: Why?

- To quantify the actual HF performance
- Extraction of small signal equivalent circuit
  - ✓ Estimation of intrinsic / extrinsic HF performance
  - ✓ Optimization of transistor architecture and topology
  - ✓ Electrical modeling

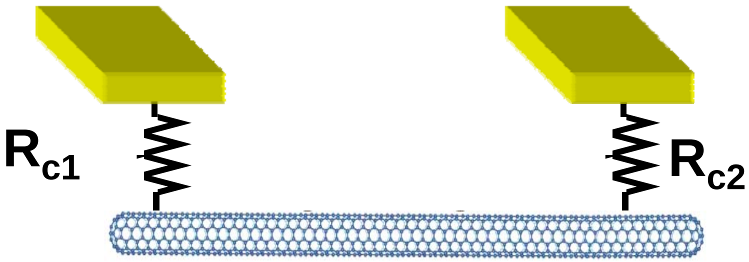
Measurement techniques in spectral and time domains

- ✓ **Spectral: Vectorial Network Analyzer,**
- ✓ **time domain: Laser impulsion fs**

CNTFET HF measurements

Challenges to overcome

Nanoscale device



R_{int}, R_L

$$R_{int} = \frac{h}{4.e^2}$$

$$R_L = \frac{h}{4.e^2} \cdot \frac{L}{L_m}$$

- **High impedance value (> 6.5 KΩ)**
- **Low current for a single nanotube**

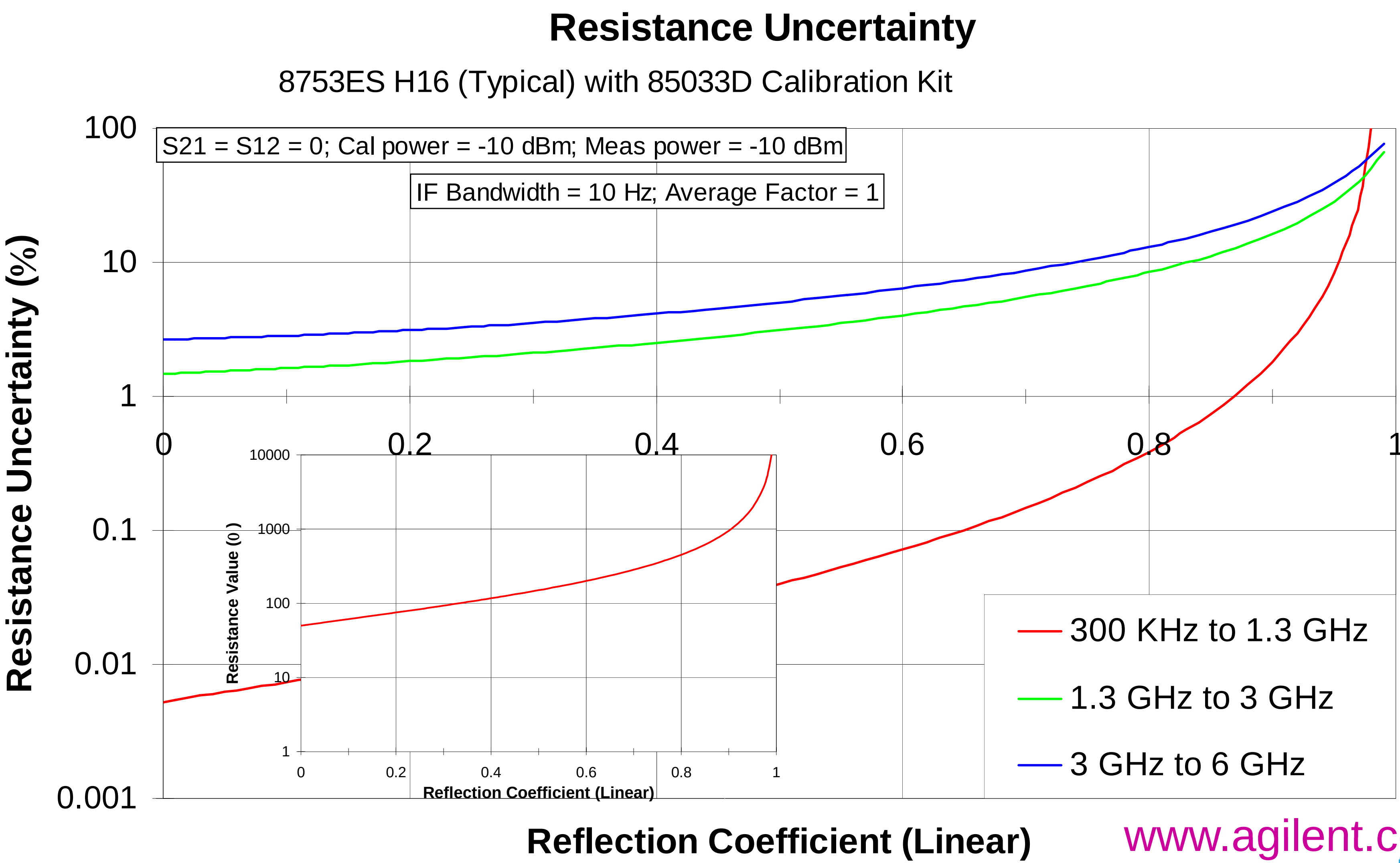
A few µA

HF Equipments

- **50 Ω system's impedance**
- **Problem of accuracy in S-parameters measurement of high impedance Structures**

CNTFET HF measurements

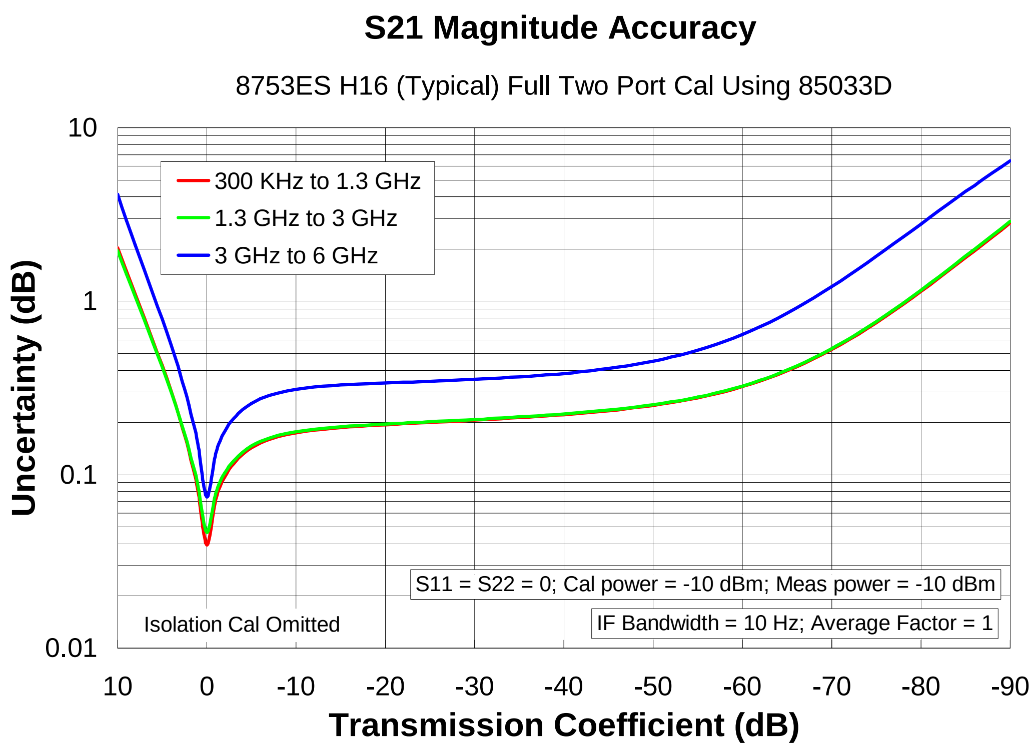
Spectral Domain: VNA, reflection uncertainty in coaxial (7mm) environment

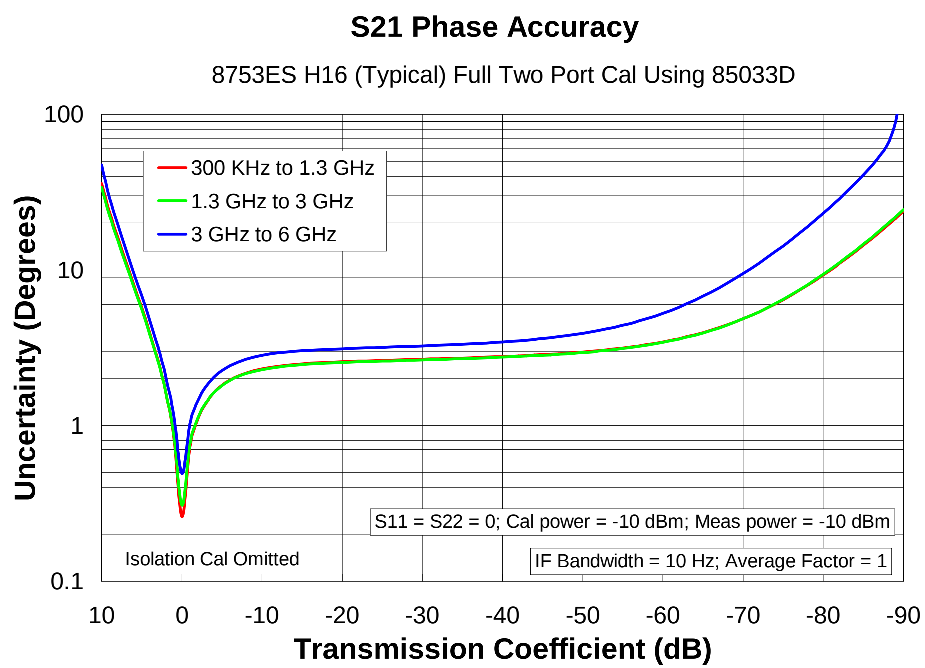


www.agilent.com

CNTFET HF measurements

Spectral Domain: VNA, transmission uncertainty in coaxial (7mm) environment



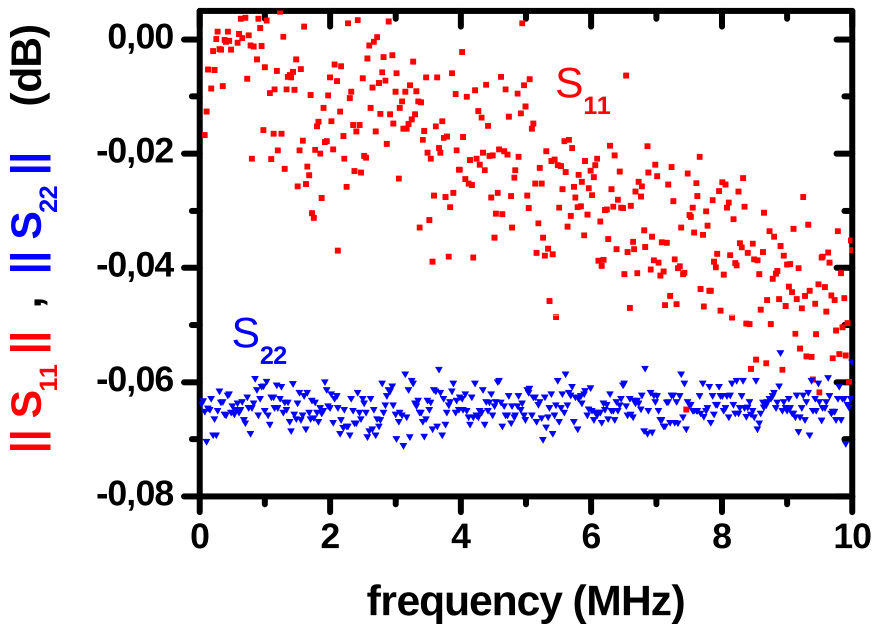


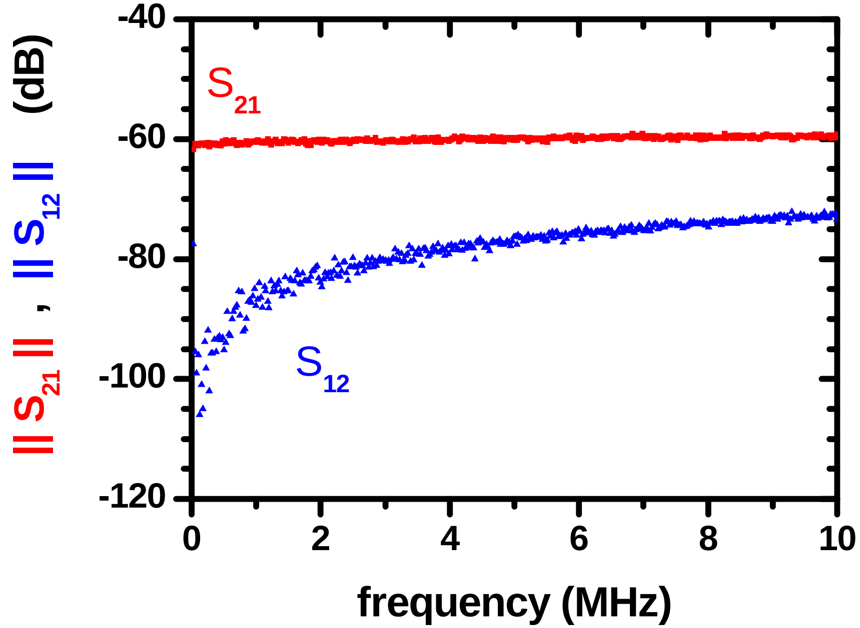
www.agilent.com

CNTFET HF measurements

S-parameters Uncertainties: Impact in the case of nanodevices

On-wafer Measurements: calibration SOLT, RBW= 10Hz





Rin >50kΩ

gm ~ 10 µS

Rout ~ 11 kΩ

J.M. Bethoux and al. IEEE Trans. On Nano, July 2006

IEMN-CEA LEM

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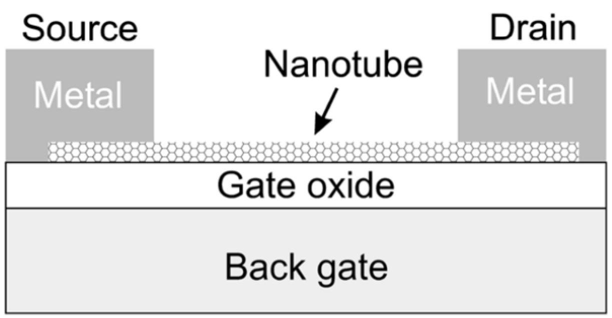
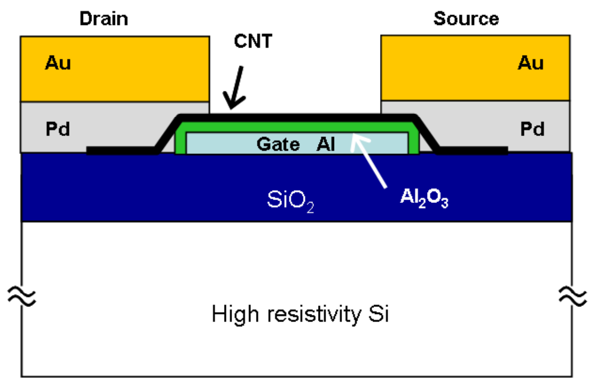
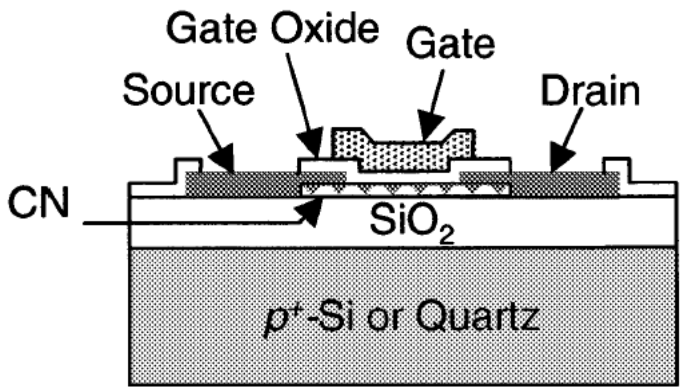
HF CNTFET Architectures

“Back Gate MOSFET”

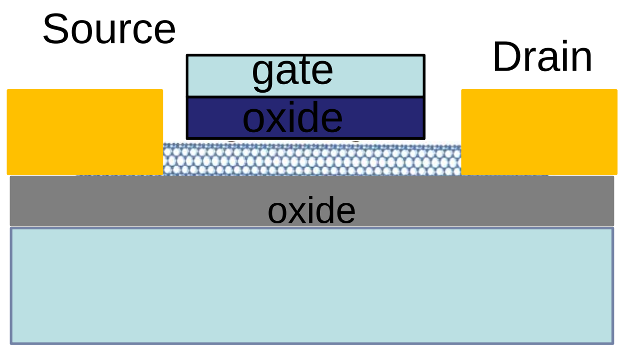




“Top Gate MOSFET”



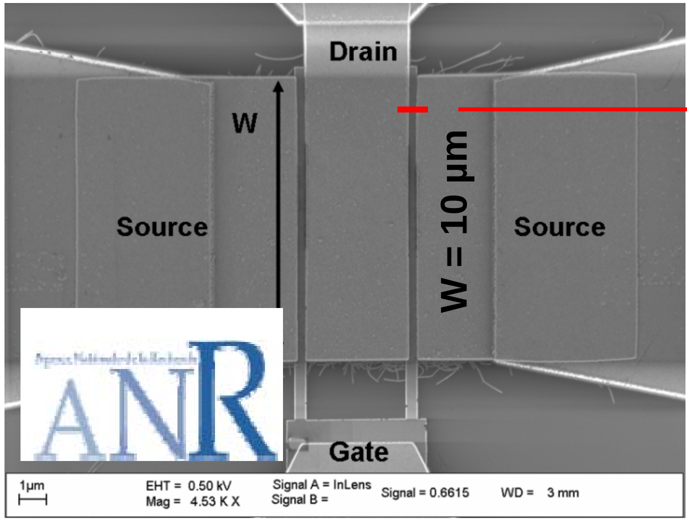
IEEE TRANS. ON NANOTECH., VOL. 3, NO. 3, SEPTEMBER 2004
IBM group.

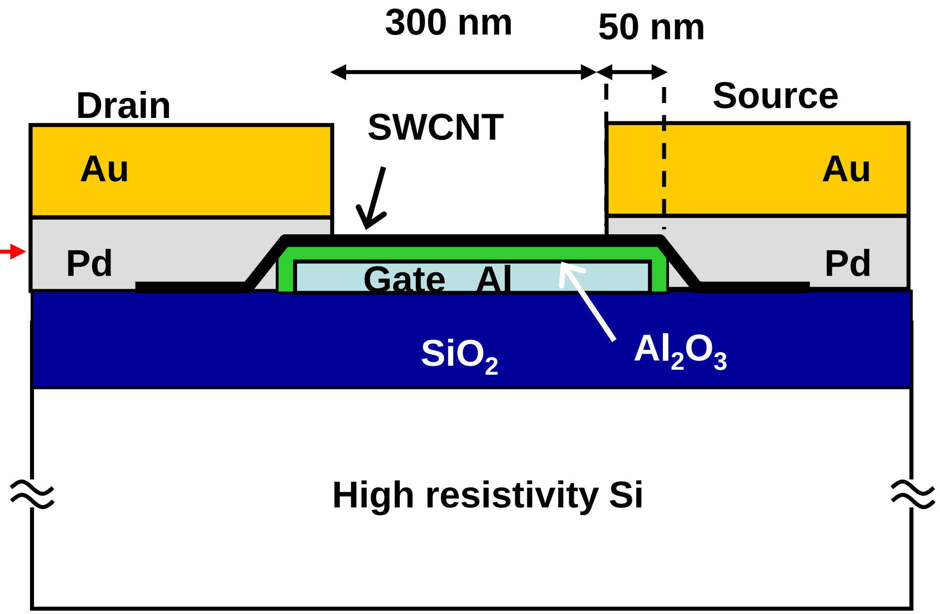


Interests:
Lower parasitic gate-to-source & gate-to-drain capacitances

8GHz f_{t_int} HF CNTFET

IEMN device structure

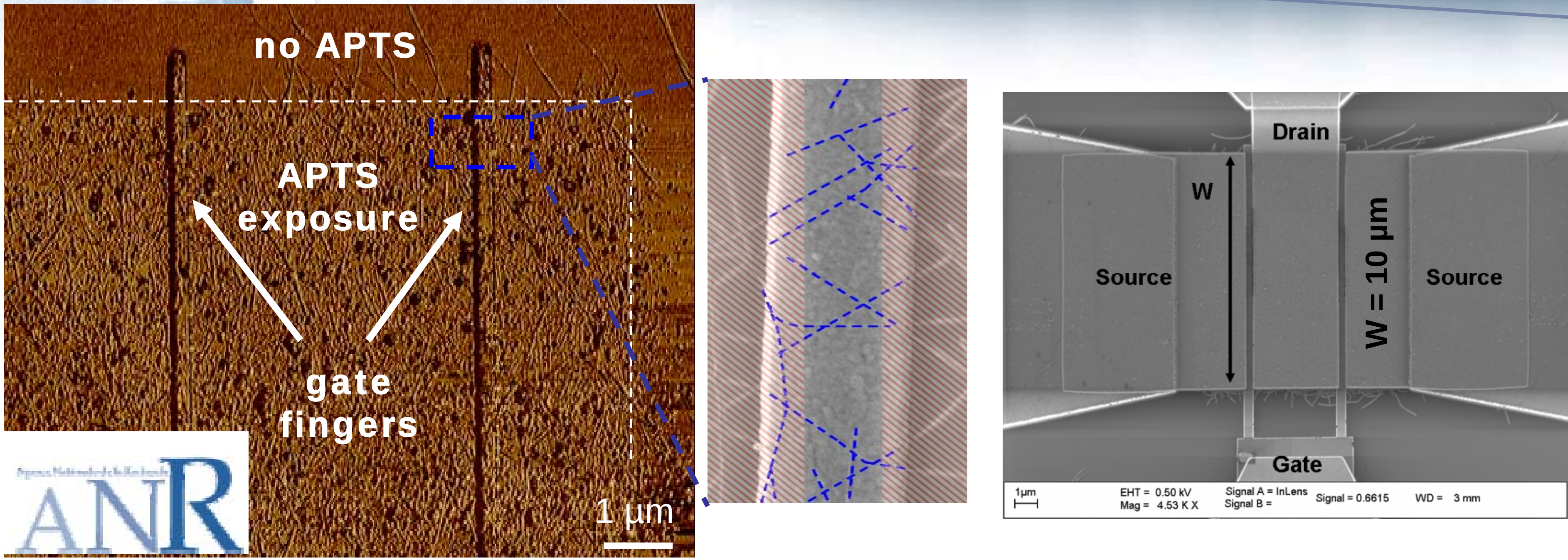




Device cross section

- High resistivity silicon substrate to reduce microwave loss
- Back gate process – Metallic Gate (Al / Al_2O_3)
- SWCNTs (Ø 1.4nm) deposition: self assembly method

8GHz f_{t_int} HF CNTFET

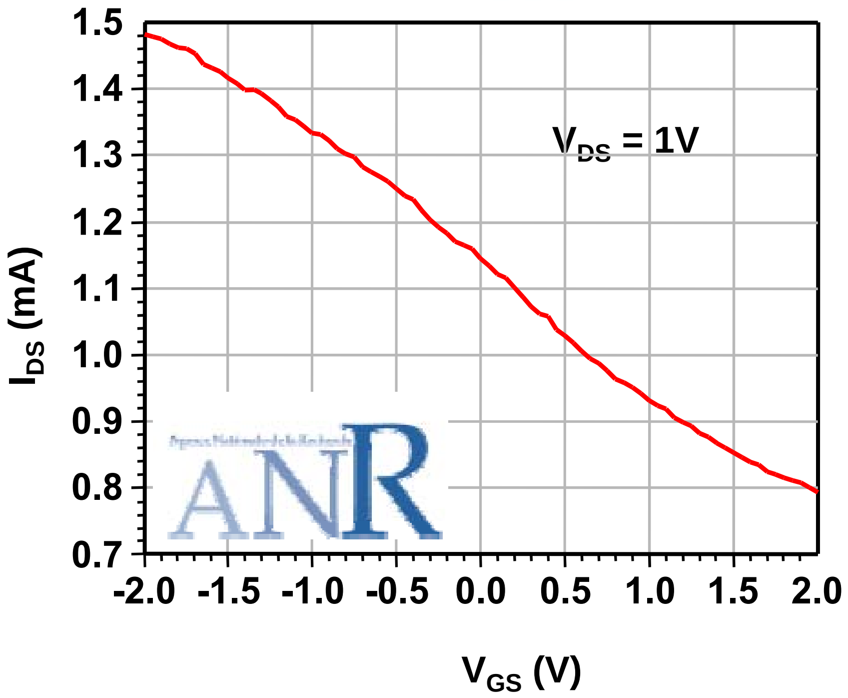


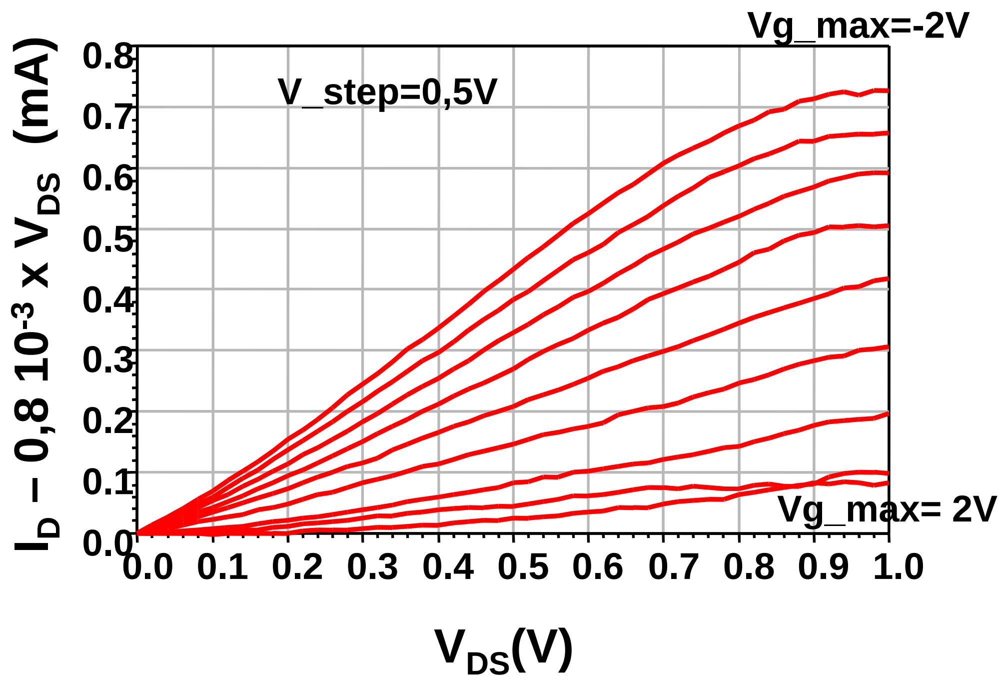
- Deposition of aminopropyl-triethoxy-silane (APTS) as sticky patch
- Selective deposition of SWCNTs (in dispersion in inorganic solvent) in the gate area define with APTS (random deposition)
- CNT density of about 10 NTs / µm

J.P. Bourgoin group – CEA LEM

8GHz f_{t_int} HF CNTFET

IEMN device structure





- Deposition of a large number of CNTs I_{ON} ~ 0.7 mA
- There is no pinch-off (High I_{OFF}): Influence of metallic CNTs
- Gm # 0.2 mS   Gd # 0.8 mS

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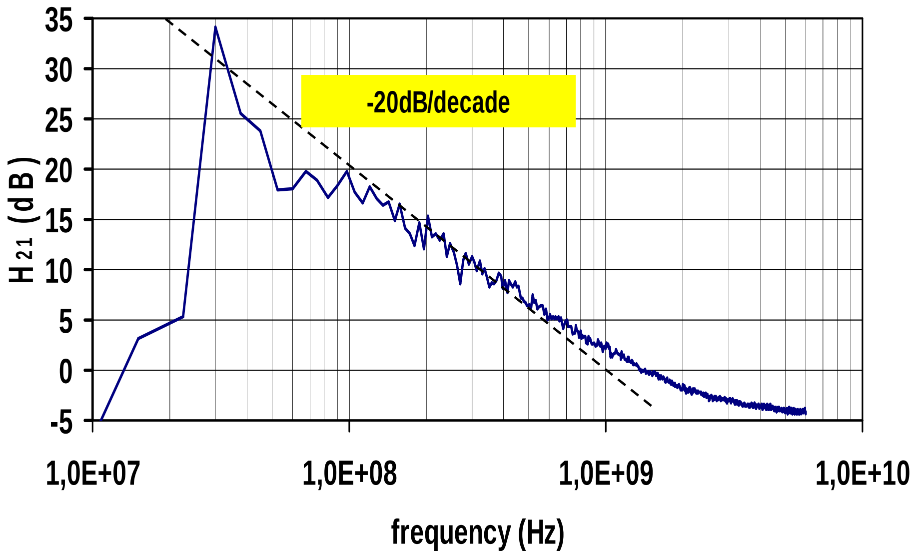
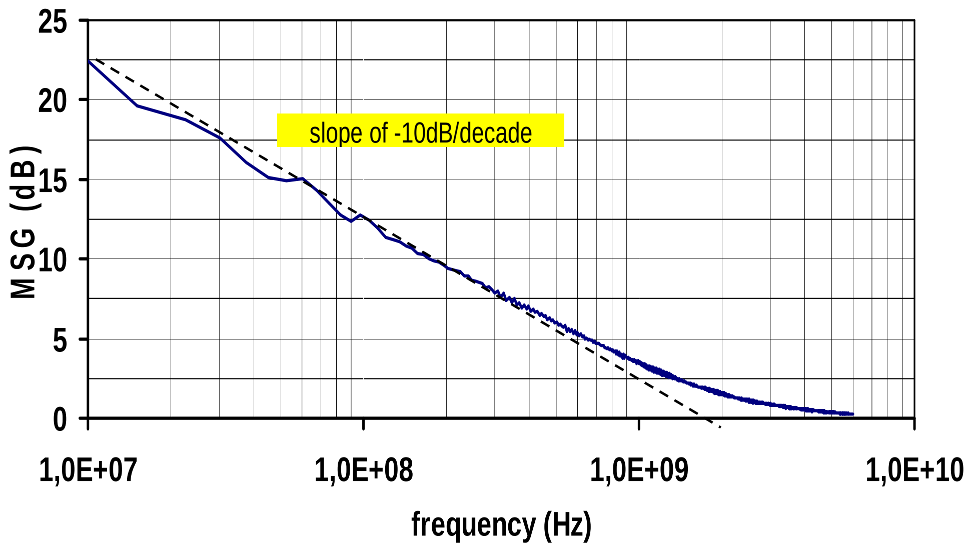
8GHz f_{t_int} HF CNTFET

Extrinsic device performance

- In the device reference plane, gains are deduced from S-parameters

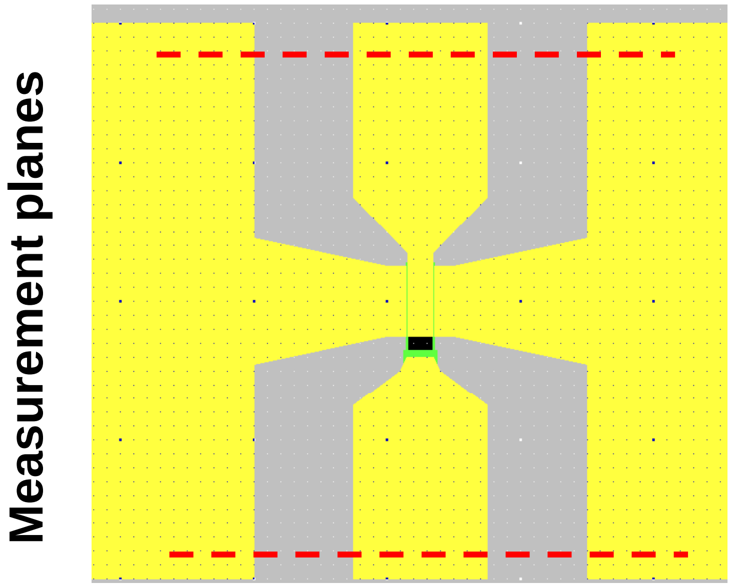




V_{DS} = 1 V V_{GS} = 0V

Calculation of intrinsic device performance

- For any device with CNTs, similar structure without CNTs, is fabricated on the same wafer. This structure is considered as "Open structure"



- From S-parameters, pads are de-embedded using this expression

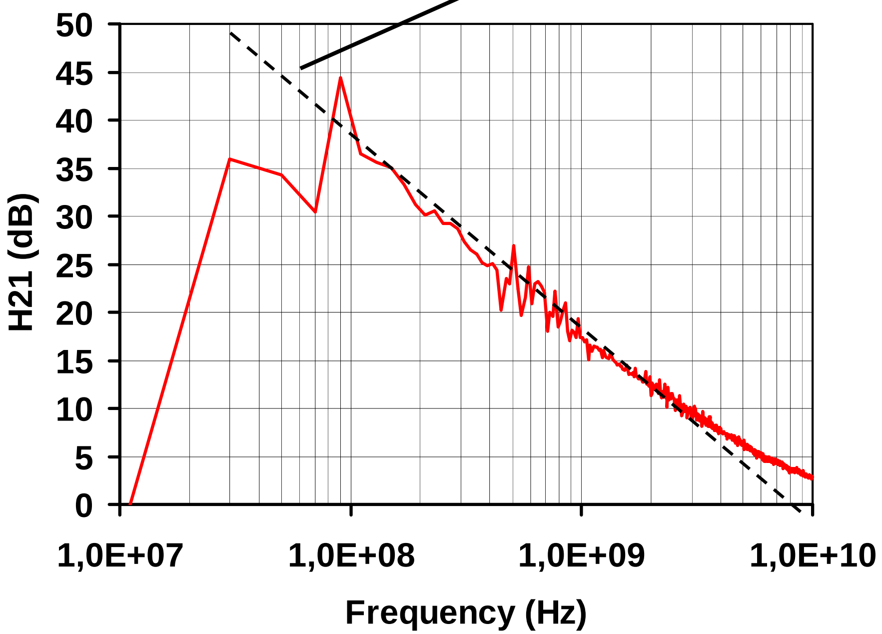
$$[Y_{intrinsic}] = [Y_{meas}] - [Y_{open}]$$

8GHz f_{t_int} HF CNTFET

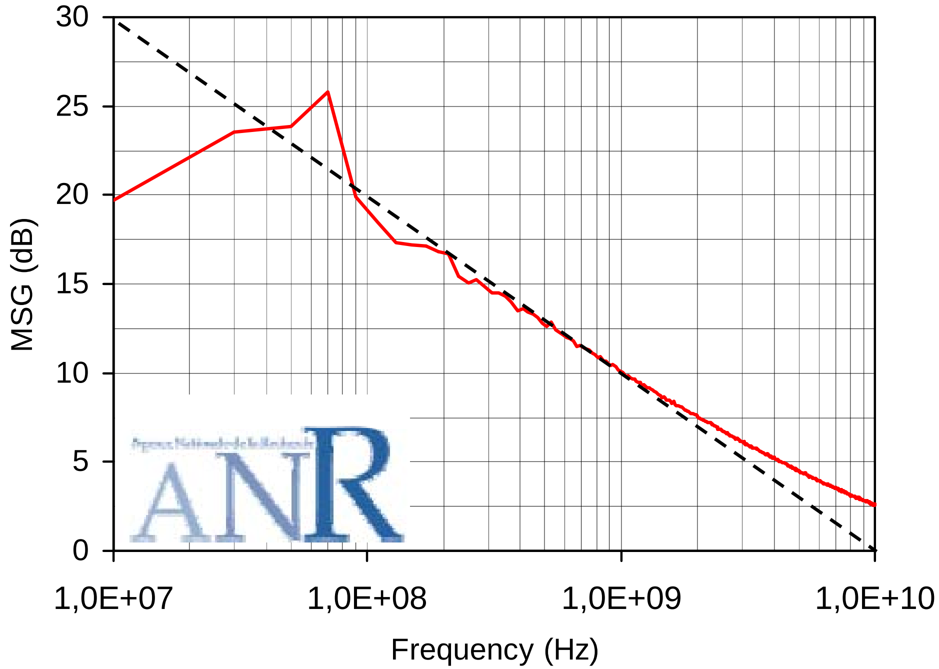
Intrinsic device performance

Current Gain

Slope of
-20 dB / decade



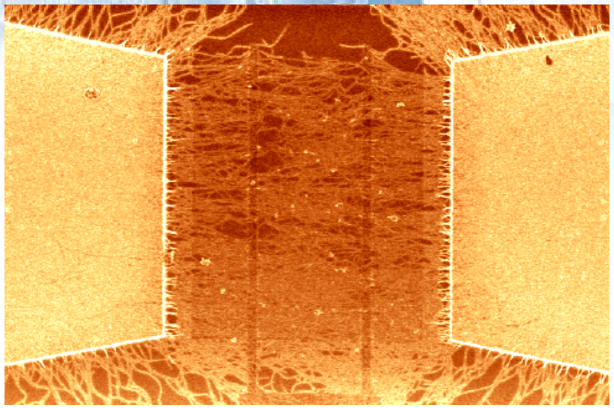
Maximum stable Gain
10 dB @ 1GHZ
Slope of
-10 dB / decade

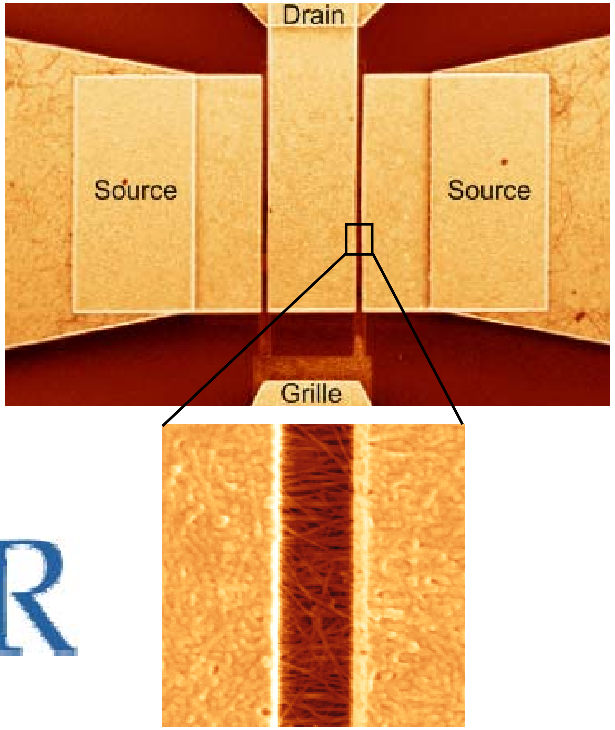


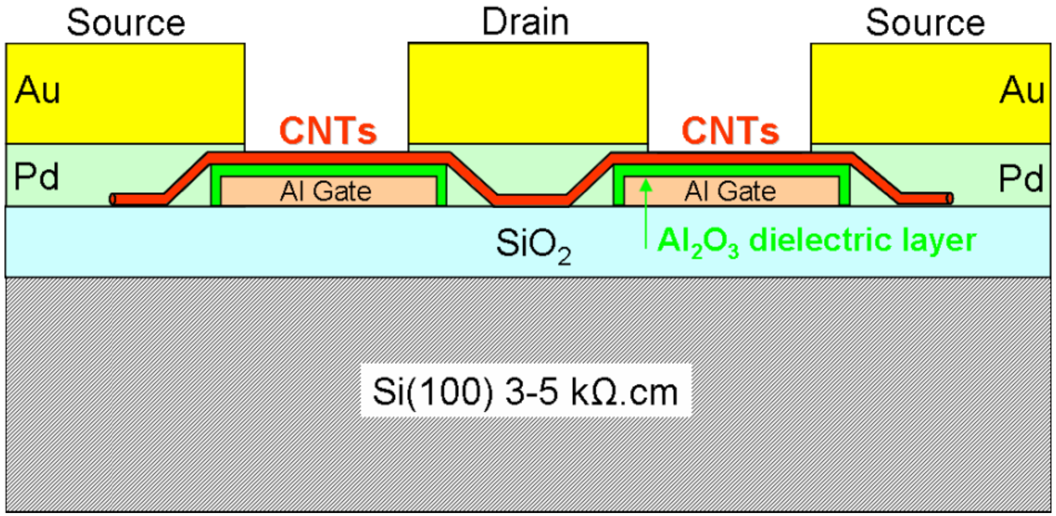
F_T = 8 GHz

J.M. Bethoux and al. EDL, August 2006
IEMN-CEA LEM

30GHz f_{t_int} HF CNTFET





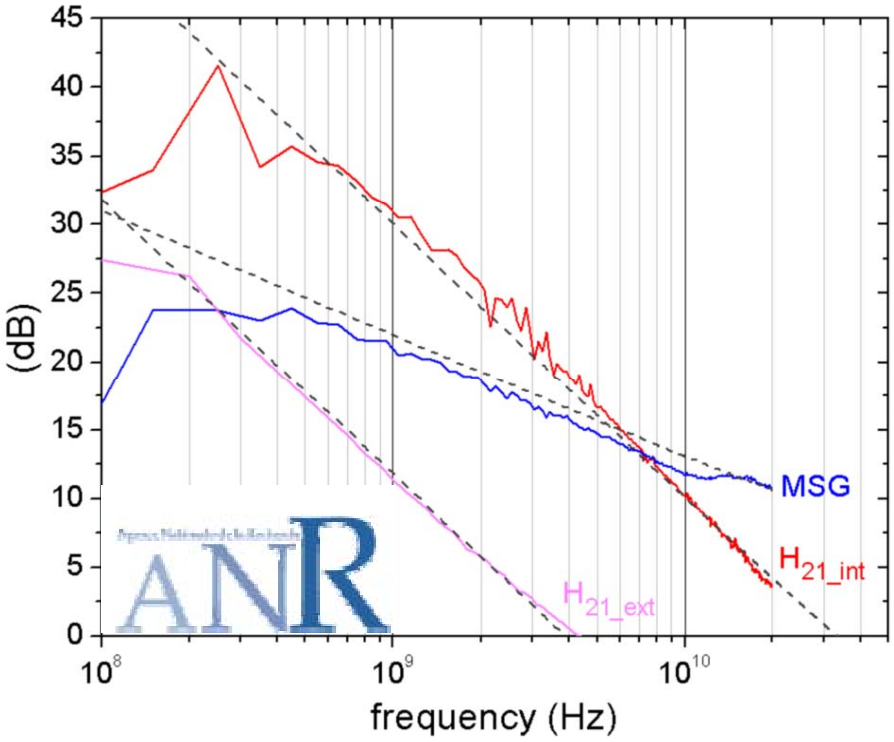


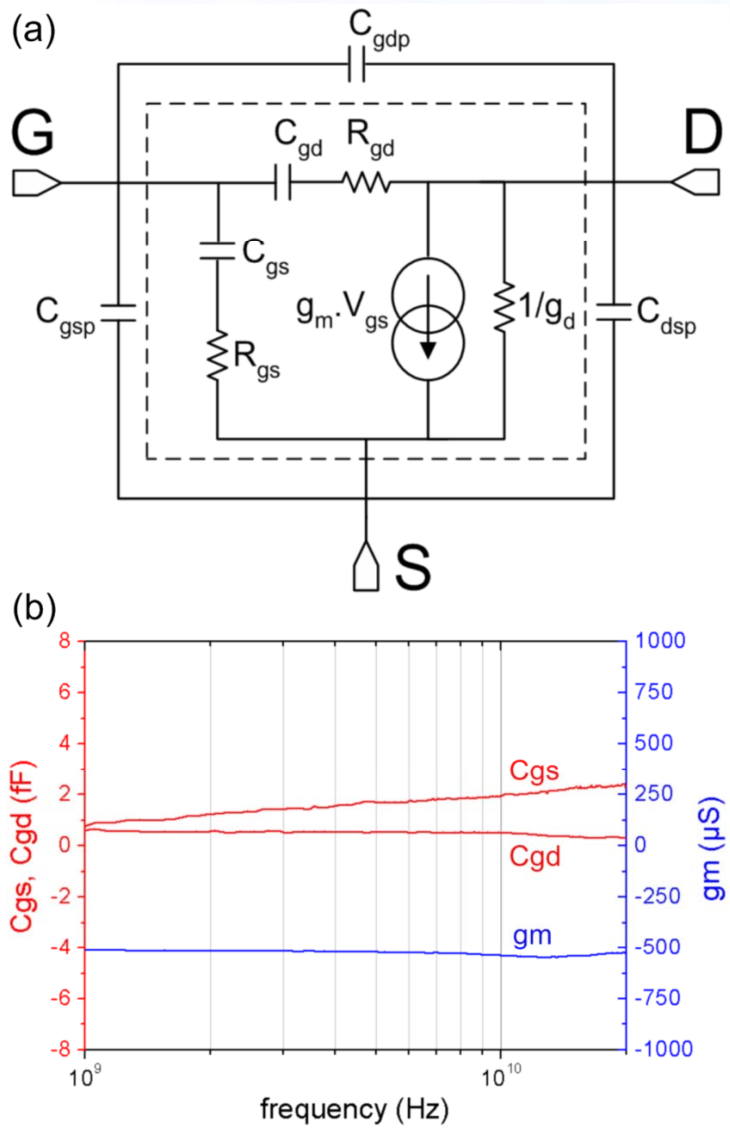
Same architecture
But CNTs deposition method different

CNTs density ~ 10-20 times higher
Total current range : 15 – 30 mA

no SC/metal CNTs selection
or metal CNTs destruction

30GHz f_{t_int} HF CNTFET





V_{DS} = 1.5 V and V_{GS} = -2 V

A. Le Louarn et Al. *APL* june 2007

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Summary & Perspectives

- ❑ CNT-based transistors & circuits one of best candidates

- ❑ for low cost high performance electronic; new functionalities in "More than Moore" scheme

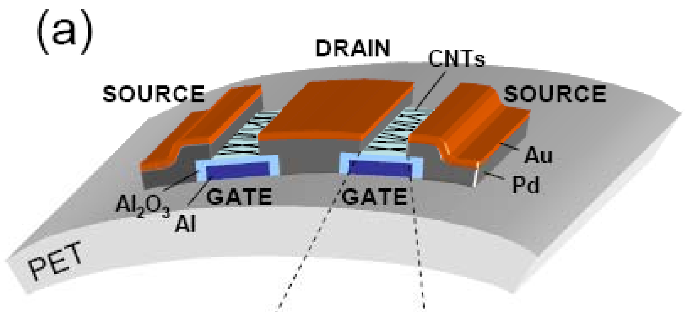
- ❑ Actual recent improvements in term of CNTs technology

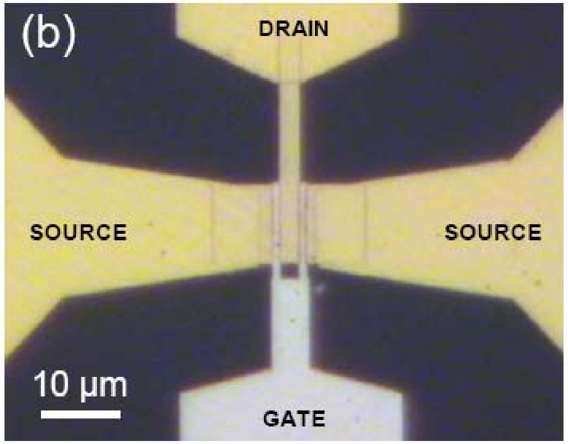
- ❑ By the realistic improvement of electrical characteristics of CNTFET: conventional
  measurement set-up (VNA, LSNA, on-wafer...) are now suited.

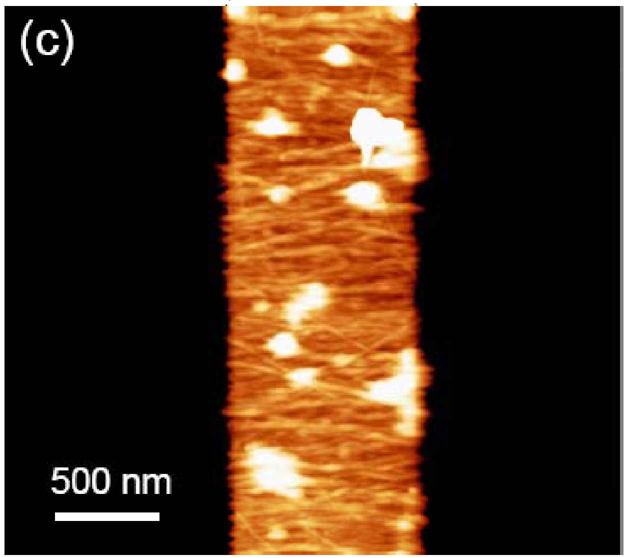
- ❑ CNTFET may be considered as microwave transistor with cut-off frequency in the cm wave range

Summary & Perspectives

GHz CNTFET on flexible substrate







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