Interuniversity Microelectronics Center
Kapeldreef 75
B-3001 Leuven

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ENDORFINS

***EN**ABLING **D**EPLOYMENT **O**F **RF** MEMS TECHNOLOGY **IN S**PACE TELECOMMUNICATION.*

Summary Report

Author(s):	Ingrid De Wolf		
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ESTEC technical manager	Laurent Marchand		

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Review list:

Name	Date
Ingrid De Wolf	
Jean Roggen	

Distribution list:

ESA-ESTEC	L. Marchand (TEC-QCT) I. Aupetit (RES-PTM)
IMEC	Ingrid De Wolf (MCP/REMO) Piotr Czarnecki (MCP/REMO) Philippe Muller (MCP/REMO) Philippe Soussan (MCP/PMT) Xavier Rottenberg (MCP/DARTS) Walter De Raedt (MCP/DARTS) Philip Ekkels (MCP/TOP) Harrie Tilmans (MCP/TOP) Jean Roggen (BD/CA)

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1 Introduction

ENDORFINS is the acronym for '**En**abling **d**eployment **o**f **RF**-MEMS technology **in** **s**pace telecommunication".

The objective of the project was to "*Perform an in-depth assessment of the reliability and related failure modes of RF-MEMS, in view of their deployment in space and improve this reliability (for switches) through processing optimization*". Key in this definition is that the reliability improvements have to be achieved through processing optimizations only and not through design optimizations. For this reason, only one mask set was designed while a lot of processing iterations of different complexity levels took place.

To summarize, the ENDORFINS purpose can be detailed as

- study the possible applications of RF-MEMS in space,
- study the reliability issues and failure modes that prevent the deployment of RF-MEMS in space,
- define corrective actions to improve the reliability with focus on processing steps and materials used (focus on RF-MEMS capacitive switches), taking into account the packaging
- apply these corrective actions (where possible) to the processing and investigate their effect on the reliability of the RF-MEMS devices.

To achieve the ENDORFINS objectives, the work was subdivided into several workpackages. These workpackages and their results are discussed below.

1.1 WP110: Survey

WP110 was composed of 2 main activities. A survey was made of the applications of RF-MEMS in space (WP111) and of the existing reliability issues and failure modes in RF-MEMS switches (WP112) that at the start of ENDORFINS (August 2006) slow down, prevent or could be expected to prevent the introduction of such switches in space applications.

1.1.1 WP111: Survey of RF-MEMS for space applications.

This survey was performed in collaboration with *Alcatel Alenia Space (Olivier Vendier*.

A list was given of ESA standards that any new components need to be compliant with prior to space use. Next the context of RF MEMS switches application within satellite payloads was described, followed by the specifications of these devices for selected applications.

It is concluded that RF-MEMS switches in thin-film technologies (addressed within ENDORFINS) can be the potential basic blocks of many new generation microwave sub-assemblies and innovative integrated microwave functions such as controllable phase-shifters, redundancy matrices, and variable oscillators. Besides these devices, removing some thicker parts of the substrate (typically silicon), allows to create small cavities (basis for high-frequency filters), and air-suspended lines (inducing much lower RF-loss than other planar circuits). Therefore, combining switches and other passive low-loss and high-Q components, opens the way to very compact and performant MEMS microwave assemblies.

RF MEMS exhibit excellent RF properties as low insertion loss, low power consumption, and high isolation. They can be integrated into telecom satellite payload to achieve a higher degree of functionality and reconfigurability. However, several challenges remain that are associated with high reliability and packaged RF MEMS switches. The reliability challenges were addressed in the ENDORFINS project.

1.1.2 WP112: Reliability survey and corrective actions.

A reliability survey was performed at the start of ENDORFINS. Several failure modes were defined and discussed. It was defined whether they are catastrophic (causing a total and irreversible loss of functionality) or cause drift 'out of specs' and, as far as this is known, which physical or chemical process is causing this failure. The discussed failure modes are:

- creep
- plastic deformation
- temperature induced elastic deformation
- fatigue
- stiction
- electromigration
- self biasing
- friction and wear
- whisker formation
- corrosion
- fracture
- structural short
- poor down state capacitance
- fusing
- electrical breakdown

Next in a Failure Mode and Effective Analysis (FMEA) was made. The general definition of FMEA is "*a systematic and structured study of the potential failures that might occur in any part of the device to determine the probable effect of each on all other parts of the system and on probable operational success, with the aim of improvement in the design, product and process development*". We applied this FMEA to RF-MEMS and studied their failure mechanisms, failure defect, failure mode and possible failure cause, as known at the start of ENDORFINS, from literature and from in-house experience. The result of this study is shown in Table I.

Table I: FMEA analysis of a capacitive switch. Sev = severity parameter; Occ = occurrence parameter; Det = Detectability; P.N= Priority Number = Sev x Occ; R.P.N. = Risk Priority Number = Sev x Occ x Det.

	Potential Failure Mechanism	**Sev**	**Failure Defect**	**Failure Mode**	**Occ**	**P.N**	**Possible Failure Cause**	**Det.**	**RPN.**
1	Dielectric charging of the insulator of capacitive switches	8	Stiction to bottom electrode. Not-permanent (charges flow away when charging cause is taken away).	Drift in CV curves, drift in Pull-in and Pull-out voltages, Dead device	10	80	1. Electric Field Charge Injection 2. Air-gap Breakdown 3. Electron emission 4. Radiation	2	160

	Potential Failure Mechanism	Sev	Failure Defect	Failure Mode	Occ	P.N	Possible Failure Cause	Det.	RPN.
2	Micro welding (ohmic switches and capacitive switches with contact metal on dielectric)	9	Stiction	Dead Devices, drift in contact resistance, anomaouls switching behaviour (temporary stiction).	7	63	1. soft metals coming into contact (cold welding) 2. high current through metal-metal contacts (often at asparities) (hot welding) 3. ESD	4	252
3	T-induced elastic deformation of the bridge (ohmic and capacitive switches)	7	Non-permanent) deformation of the bridge (is restored when T-source is removed);, possibly stiction if large deformation (to bottom electrode or top of cavity if packaged).	Shift of electrical parameters (pull-in/pull-out V, capacitance, contact R…); change of mechanical properties	7	49	1. Different Thermal Expansion Coefficients (CTE) 2. Environment Temperature 3. Power RF Signal induced Temperature 4. Non uniform temperature repartition	5	245
4	Plastic deformation of the bridge (ohmic and capacitive switches)	7	Permanent deformation of the bridge, possibly stiction if large deformation (to bottom electrode or top of cavity if packaged).	Shift of electrical parameters (pull-in/pull-out V, capacitance, contact R,…); change of mechanical properties	7	49	1. Creep 2. Thermal induced changes in material properties (for T>Tc)	3	147
5	Structural Short (electrical and non-electrical connections) (ohmic and capacitive switches)	9	Particles, shorted metals, contamination, remains of sacrificial layer, stuck bridge	Changes in electrical parameters, dead devices	5	45	1. Contamination; Particles; remaining sacrificial layer material 2. Wear Particles 3. Fracture 4. Lorenz Forces 5. Shocks	4	144
6	Capillary Forces (ohmic and capacitive switches)	10	Stiction	Dead device	4	40	Presence of humidity (Package leaks, incorrect release step)	4	160
7	Fusing (ohmic and capacitive switches)	10	Opens, roughness increase	Dead Device	4	40	High RF power pulses, ESD	2	80
8	Fracture (ohmic and capacitive switches)	10	Broken bridges and hinges	Dead device	4	40	1. Fatigue 2. Brittle materials + shock	2	80

	Potential Failure Mechanism	Sev	Failure Defect	Failure Mode	Occ	P.N	Possible Failure Cause	Det.	RPN.
							3. High local stresses + shock		
9	Dielectric breakdown of the insulator. capacitive switches)	9	Dead device, possibly stiction	Short between bridge and actuation electrode	4	36	1. ESD 2. Excessive charging of Insulator	4	144
10	Corrosion (ohmic and capacitive switches)	7	Dendrites formation, oxidization, changes in color	Degradation of electrical and mechanical properties, shorts	5	35	1. Presence of water or other fluid (chemical reaction), enhanced by bias 2. Corrosive gases induced chemical reaction (ex. Oxidation)	2	70
11	Wear Friction Fretting corrosion (ohmic and capacitive switches)	8	Surface modifications, Particles (Debris), Stiction	Shorts, opens, shift of electrical parameters, contact resistance shifts	4	32	1. Sliding Rough Surfaces in contact	6	192
12	Creep (ohmic and capacitive switches)	6	Deformation of the bridge in time	Electrical and mechanical parameters shifts	5	30	High metal stress and high temperatures, creep sensitive metal.	4	120
13	Equivalent DC Voltage (ohmic and capacitive switches)	7	Self biasing Stiction	Anomalous switching behaviour, changes in electrical parameters	4	28	High RF power inducing spontaneous collapsing or stiction of mobile part	6	168
14	Lorenz Forces (ohmic and capacitive switches)	7	Self Biasing Stiction	Anomalous switching behaviour, changes in electrical parameters	4	28	1. High RF power in two adjacent lines 2. External Magnetic Field	6	168
15	Whisker formation (ohmic and capacitive switches)	7	Bumps in metal, holes in insulator on top of metal layers, ...	Anomalous down capacitance or contact resistance, possible increase of charging sensitivity	4	28	High compressive stress in metal resulting in grains extrusions; might be enhanced by T-steps	6	168

	Potential Failure Mechanism	Sev	Failure Defect	Failure Mode	Occ	P.N	Possible Failure Cause	Det.	RPN.
16	Fatigue (ohmic and capacitive switches)	8	Broken bridges and hinges, cracks, microcracks, deformation of the bridge	Electrical and mechanical properties shifts, dead devices	3	24	Large local stress variations due to motion of parts (intended or due to vibrations or thermal cycles). Enhanced probability if cracks are present or surfaces are rough	5	120
17	Electromigration (ohmic and capacitive switches)	8	cracks, opens, thickness changes (mass transport) in metal lines	Increase of resistance, opens, shorts	2	16	High current density in metal lines enhanced by too thin and/or narrow, and steps.	4	64
18	Van der Waals Forces (ohmic and capacitive switches)	10	Stiction	Dead device	1	10	Large very smooth and flat surfaces in close contact	4	40

The first 4 failure mechanisms can indeed be considered as the most important ones, the same conclusion was drawn both from literature and from existing experience at IMEC.

The 5th failure mechanism got a high importance because remaining residues of the processing, including incomplete release of structures, is included in this mechanism. This is clearly processing related.

The 6th mechanism is indeed important when occurring, but can be avoided by a proper release process and correct protection of the switches from a humid environment. So, although it ranks high, it can be easily prevented and was not studied within Endorfins.

Next, we these failure mechanisms with processing steps and mitigation opportunities to avoid the faults, minimize their impact or reduce their probability of occurrence.

This FMEA was used during the ENDORFINS project to choose the failure mechanisms to be addressed in the different phases of the project.

2 Processing at the start of ENDORFINS

The switches of the ENDORFINS project are capacitive, thin-film metal-based switches and thus are processed using so called “cold process”. This allows integrating and using these devices on glass, ceramics, sapphire substrates or above-IC.

So far, IMEC has based its RF-MEMS metal technology on the “boosted” switch architecture. Simply put, the reliability of this type of devices is affected by the properties of the substrate, the CPW metal, the dielectric, the top floating metal, the sacrificial layer and the membrane (bridge) metal (Figure 1).

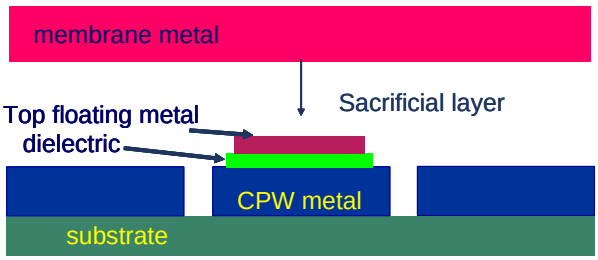

Figure 1: Schematic representation of the different layers constituting the RF-MEMS.

The process flow developed within ENDORFINS was based on the mainstream process of IMEC. Different variations of that process flow were envisioned at the start of ENDORFINS to improve the reliability of the switches in view of the different failure mechanisms listed in the FMEA table. These variations consisted of different dielectrics, different CPW metals and bridge metals, different patterning processes for dielectrics and bottom metal, different sacrificial layers, different release processes etc. Depending of the results gathered during the project, some of these solutions were looked into, others not. This was decided at the start of each new phase of the project. There were in total three phases.

3 WP120: Selection, design, test plan

3.1 Introduction

In this work package, using input from WP110, a selection was made (WP121) of failure mechanisms that would be addressed in the three different phases of the project. For this selection, input was used from the FMEA study (Table 1) and, for later phases, from test results. After the first selection, a design (WP122) was made in which test structures were defined which allow to study not only the selected failure mechanisms, but also additional failure mechanisms that might have to be studied in a later phase. In WP123, test plans were defined to address the failure mechanisms. The focus was always on solving or preventing the addressed failure mechanisms through processing optimization.

Orignially three different processing RUNs were forseen. However, because much more than 3 ‘RUNs’ were done during ENDORFINS, including many short loop tests, we use the phrase PHASES in the current deliverable. So, the project had 3 PHASES: Phase I, Phase II and Phase III. After each phase a new selection of failure modes and corrective actions was made and a new test plan for the next phase was defined.

3.2 WP121: Selection of failure modes and corrective actions

3.2.1 Phase I

3.2.1.1 Introduction

From the list of possible failure mechanisms, some were selected to be addressed in Phase I.

This selection also took into account processing possibilities, restrictions and *ease*. With the latter we mean that it is better to first tackle failure modes that can be studied using very simple processing steps, and that might occur in an early process step. As a result, the first failure modes assessed in this phase were not per se the most stringent ones as selected

through the FMEA. A failure that might occur in layers from the first processing steps, ex. whiskering, has for example a low ranking on the FMEA table, but if occurring it will hamper studying failures such as charging that occur in layers that are deposited at a later stage of the processing. Also, it is not effective to study failure mechanisms where a complete RF-MEMS process is required before studying failure mechanisms that can be investigated using very simple processing such as uniform layer deposition. The following failure mechanisms were selected from the FMEA study to be studied in Phase I:

3.2.1.2 Whisker formation

Whisker formation can occur in metals due to the combination of compressive stress and high temperature. Whiskers are grains popping out of the metal. They increase the local roughness. If more than one grain pops-up, hillocks can form giving the same increase in roughness. Whiskers were reported for thin aluminium films. This failure mechanism was selected because of several reasons.

- Whisker formation can be studied in a very easy way on uniform wafers with deposited CPW metal. Different metals can be selected and studied. If whiskers occur, it is easy to test different combinations of metal layers or compositions.

- If whisker formation occurs, this will have inpact on the insulator quality and on the roughness and will make the study of other failure mechanisms such as charging (the most important one) difficult to impossible. For this reason it should be tackled first.

3.2.1.3 Charging

Charging is clearly the “nr. 1” failure mechanism in the FMEA list. Although the exact mechanism of the charging is not understood yet, one can expect that different dielectrica will have a different charging behaviour. From processing point of view, it is important to choose the ‘best’ dielectric, i.e. the one that shows the best switching lifetime and can still be easily processed. For this reason the charging behaviour of different dielectrica was studied in Phase I on simple test structures (uniform bottom metal layers with uniform insulators consisting of different dielectric and patterned bridges.).

3.2.2 Phase II

Using the tests results on whisker formation, a bottom metal combination was chosen that was proven to be thermally stable (no whisker formation) and to have a low roughness, also after thermal treatment and with dielectric on top.

The selection of failure mechanisms to be studied in Phase II was the following:

3.2.2.1 Charging

Charging experiments were started in Phase I on uniform bottom metal layers with uniform insulators consisting of different dielectric and patterned bridges. The results gave some first conclusions on the charging properties of the dielectric, but due to possible processing effects on the dielectric at the bridge feet, the experiments had to be verified on completely processed RF-MEMS, i.e. with patterned bottom metal and dielectric.

3.2.2.2 Elastic deformation of the bridges due to high temperature steps

The failure mechanism that ranks 3rd highest in the FMEA study is temperature (T) induced elastic deformation of the bridge. The failure defect is a non-permanent

deformation of the bridge (if visible), which is restored when the T-source is removed. However, it might also cause stiction if the deformation is so large that the deformed bridge touches the dielectric or even the bottom side of the cap of the package. The failure mode is a shift of electrical parameters such as capacitance in up and down state, pull-in and pull-out voltage. There are different possible failure causes. One is the environmetal temperature which when changing causes a deformation of the bridge either because of expansion, or because of a difference in thermal expansion coefficient (CTE) between materials used for the bridge, another possible cause is the temperature caused by the power of the RF-signal. This temperature is expected to be non-uniform in the bridge, resulting in a deformation.

3.2.2.3 Plastic deformation of the bridges due to high temperature steps

The 4th failure mechanism on the FMEA list is plastic deformation of the bridge. In this case the failure defect is a permanent deformation of the bridge, also possibly stiction if this deformation is large. The failure mode is irremediable. The device is not necessary non-functional, but its electrical parameters will show a permanent shift. Possible failure causes are creep in the metal of the bridge and temperature or stress induced changes in material properties.

3.2.3 Phase III

In Phase III the focus was still on charging and temperature effects (mainly elastic). During Phase II, new insights in charging were obtained, especially on the possible important role of the substrate in this failure mechanism. For this reason, the following points were addressed in Phase III:

- Charging (nr. 1 in the FMEA study). Including a study of
    - the influence of the thickness of the dielectric.
    - the influence of the shape of the bridges (planar or not)
    - substrate charging
- Temperature induced elastic deformation of the bridge (nr. 3 in the FMEA study)
- The effect of 0-level packaging of the MEMS (using BCB and glass caps) on the reliability.

3.2.3.1 Charging: Dielectric thickness

If bulk dielectric charging occurs, it will be larger for thinner dielectrics because the electrical field across the dielectric increases with decreasing thickness. In that case one expects less charging for a thicker dielectric. A second reason to test a thicker dielectric is that the breakdown voltage of these dielectrics typically increases with increasing thickness. A third reason to use slightly thicker dielectric layers is that these would result in higher pull-out voltages and as a result a larger “charging margin” while only slightly increasing the pull-in voltage of the devices. For this reason, in Phase III, a thicker dielectric layer was studied.

3.2.3.2 Charging: Planarization

Charging of the dielectric results in a shift of the CV curves, to the right or to the left, depending on the charge sign. But often this shift goes together with a narrowing of the CV-curves. When testing with bipolar actuation, narrowing is dominant. It was confirmed in Phase II experiments that such a narrowing of the CV-curves can be caused by non-uniform charging. To obtain uniform charging, it is mandatory that the bridge touches the dielectric in a flat, uniform way. Dedicated structures were implemented in the design to test this effect.

3.2.3.3 Charging: Substrate

During Phase II experiments, it was suspected that the substrate might affect the charging behaviour, or even charge itself. To study this, switches were fabricated on different substrates in Phase III: glass, HR Si and quartz.

3.2.3.4 Temperature induced elastic deformation of the bridge

It was found in Phase II experiments that switches with 1 µm thick AlCu beams highly deform when subjected to the packaging temperature. In Phase III, new samples were made with 1 and 2 µm thick AlCu beams. The effect of the temperature on the bridge deformation and the pull-in voltage was studied using a new micro heating chuck in combination with an optical profilometer.

3.2.3.5 0-level packaging

Some devices were capped in a die-to-wafer approach using glass caps and BCB as bonding material. The focus was not to optimize the packaging process for an enhanced hermeticity, but to check whether the packaging process affects the lifetime of the switches. The reliability (with focus on charging) of packaged switches was compared to the one of non-packaged switches.

3.3 WP122: Design

In the design of the test structures for the ENDORFINS project a basic test structure with constant width of the metal part was used. To determine the dimensions of the test structure some calculations and simulations were performed.

The design included dedicated test structures that could be used to address as many failure mechanisms from the FMEA list as possible. In addition, it had many structures of the same kind distributed over the wafer. This allowed doing reliability tests giving statistically meaningful results.

The design was also such that it can cover a wide variety of different possible processing steps. It included several sizes optimized for different processing steps (beam thickness, gap size). Structures dedicated to one experiment were placed in one chip, to reduce possible non-uniformity effects. It was made such that automatic wafer level tests could be done. There were also dedicated cells for packaging tests.

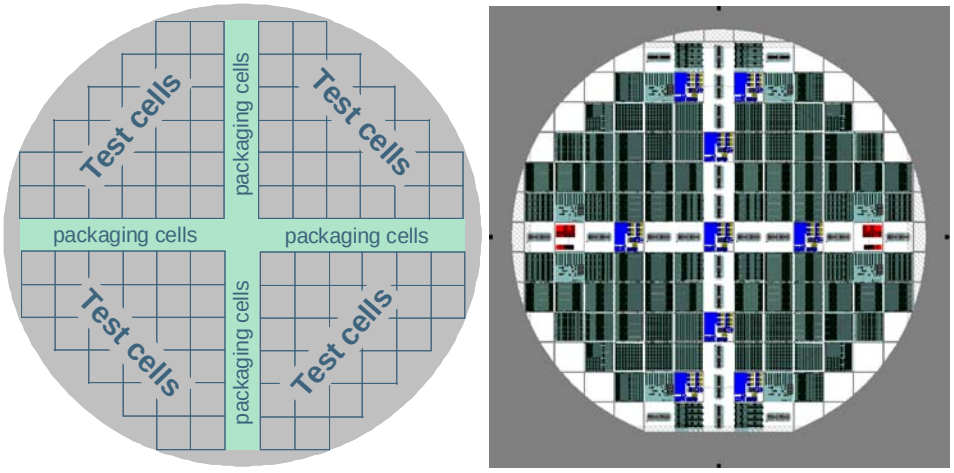

Figure 2: Design on wafer: left schematic, right: picture of the design.

As the list of failure mechanisms to be studied was not fixed at the start of the project, a rather broad design was required, including a very large set of test structures that allowed different processing options. At the end of the project, this design was obviously suboptimal from the reliability point of view. A large improvement of the reliability, this time through design, is still possible. This single design within ENDORFINS proved however to be very valuable for the intended study: optimizing the reliability through processing.

3.4 WP123: Test plan

For each of the failure mechanisms defined for the different phases, test plans were defined and described in technical notes for the respective phases.

Different instruments were used for the tests. The main ones are: AFM, SEM, ELT (electrical lifetime test system, dedicated to test the CV of RF-MEMS, and upgraded during this project), PAV (vacuum probe chamber), profilometry (Veeco,Wyko), micro heating stage, RF measurement equipment.

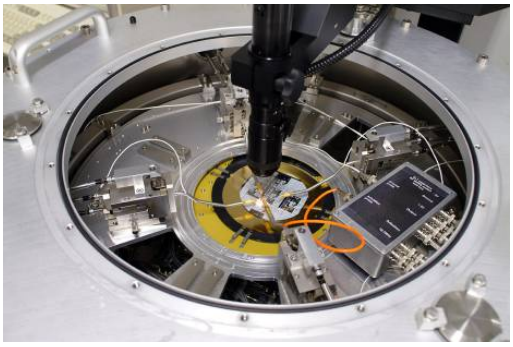

Figure 3 Fully automated ELT, C-V and stepping procedures within a controlled atmosphere chamber(PAV150, Suss MircoTec)

4 WP130 Manufacturing and testing

4.1 Introduction

This is the main part of the ENDORFINS project. It contains three sub-WPs:

- WP131: Fabrication of switches.
- WP132: 0-level packaging
- WP133: Reliability testing.

For clarity, we discuss the results of these three WPs together for each of the three phases.

4.2 Summary of the main results from Phase I

4.2.1 Introduction

In Phase I two kinds of samples were fabricated:
- Wafers (glass or Si substrate) with non-patterned metal stack and dielectric (see Figure 4)

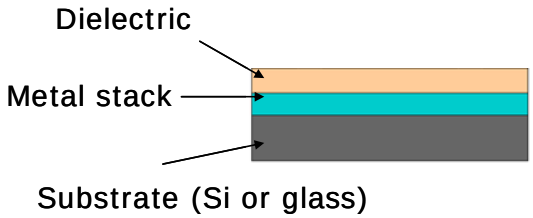

Figure 4 Schematic cross-section of whisker formation test structures

- Wafers (glass or Si substrate) with non-patterned metal stack and dielectric with a patterned bridge on top (see Figure 5)

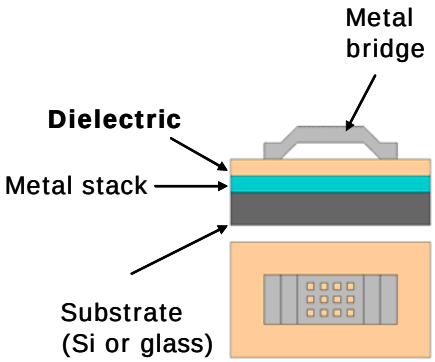

Figure 5 Schematic cross-section of simple MEMS test structures

4.2.2 Whisker-pinholes

In total 78 wafers with uniform non-patterned bottom layers (metal + dielectric), as shown in Figure 4, were used to check whisker and pin-hole formation, i.e. stability of the bottom layers before and after 1 hour annealing at 270 ^{o}C. It was shown that depending on the selection of bottom metals, whisker formation could indeed occur after the anneal (Figure 6). The following conclusions were made:

- Experiments revealed best roughness around **8nm**
- Thick-layers are more T-stable but present an increased roughness (27nm)
- There is hillock/whisker growth by Al_2Cu grain formation in AlCu films
- Ta prevents a dramatic increase of roughness after a thermal step

Several bottom layers were found that showed only small changes of their roughness and no whisker formation after anneal. The best of them (low roughness), a combination of AlCu and Ta, was used in all further processing.

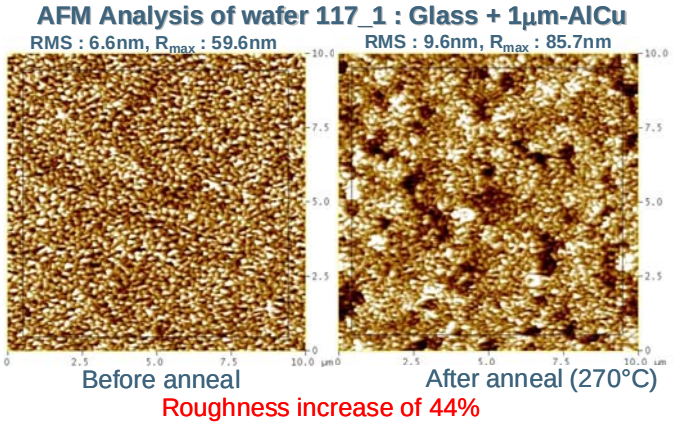

Figure 6: Whisker formation in AlCu on glass after an annealing step.

4.2.3 Charging

Different dielectrics were tested with unipolar positive (+ 13V), negative (-13V) and bipolar (switch between 0, +13, 0 and -13V) actuation voltages at 100Hz, in N_2 environment, at room temperature. Tests were done using the electrical probing configuration as shown in Figure 7. A typical result (TaO dielectric) is shown in Figure 8. AlN showed slightly better results than TaO. It was shown that there is an effect of the release step on the lifetime: the longer the release, the shorter the lifetime.

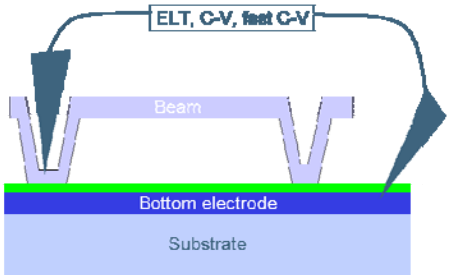

Figure 7: Probe configuration for Phase I structures

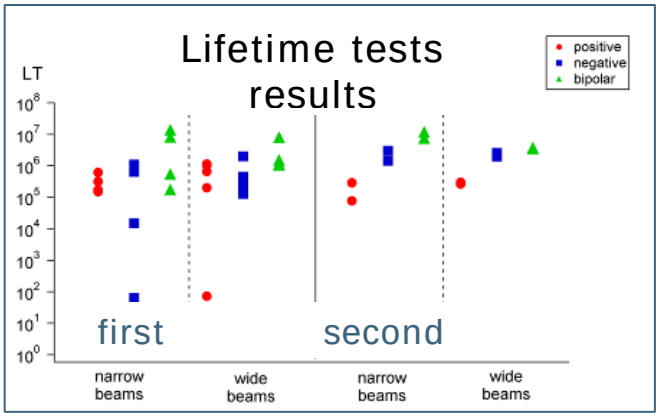

Figure 8: Lifetime test results for two similar wafers of Phase II devices (uniform TaO dielectric, patterned bridge).

4.3 Summary of the main results from Phase II

4.3.1 Introduction

In Phase II the main tests were performed on fully processed devices, i.e. patterned bottom metal, dielectric and bridge. Some additional tests were done on Phase I devices.

4.3.2 Temperature

A T-step of 170°C during 5 min and 250°C during 10 min in a N_2 furnace resulted in a large deformation of the 1 µm thick AlCu bridges (up to 8 µm, depending on the design). The effect was slightly smaller for 2 µm thick bridges. It was demonstrated that this deformation can result in stiction of the bridge to the bottom electrode or even to the bottom of the 0-level cap. This problem can be solved through design.

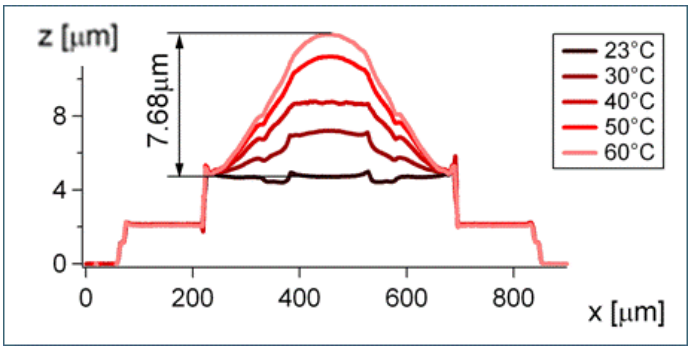

Figure 9: Effect of temperature on bridge curvature

4.3.3 Charging

Different charging tests were performed on devices with and without (native AlO) dielectric. The following main conclusions were made:

- Promising reliability (switching cycles) results were obtained for wafers with various dielectrics.
- Wafers without deposited dielectric but with native AlO showed very good lifetimes (> 10^8 at 6V, 100Hz, 50% duty cycle, unipolar actuation, in N_2).
- It was confirmed that there is an impact of the release step on the lifetime: the longer the release, the lower the lifetime
- Tests on dedicated test structures confirmed that non-uniform charging can cause a narrowing of CV curves.
- A very good uniformity over the wafers is obtained, allowing having statistical information (Weibull plot).
- It is shown that for some dielectrics there is an optimal actuation voltage, i.e. corresponding with an optimal lifetime. Actuation above or below that optimal voltage resuts in lower lifetimes.
- It was shown that there is a large influence of the substrate on the lifetime of capacitive RF MEMS switches.
    - Glass wafers charge much faster than HR-Si wafers – especially in air.
    - Charging of the glass is enhanced by the presence of humidity.
    - A thermal treatment should be done to remove humidity of the wafers before test or before packaging

4.4 Summary of the main results from Phase III

4.4.1 Introduction

In Phase III, packaged RF-MEMS were fabricated and studied. But because still many questions remained on the charging failure mechanisms, several non-packaged RF-MEMS devices were also fabricated to study this. Only one dielectric was further studied to reduce the number of experiments.

4.4.2 Processing

From the processing point of view, the focus of Phase III was put on

- The 0-level packaging step using a BCB ring
- Various substrates to study charging
  - Quartz
  - High Resistivity Silicon

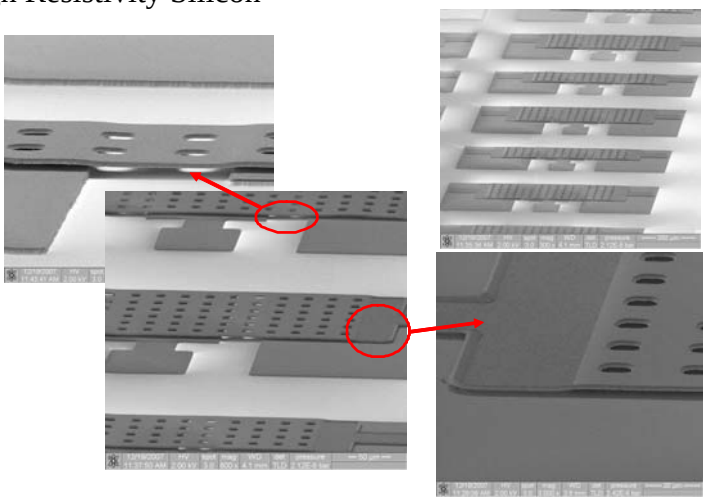

Figure 10: SEM pictures of PHASE III devices

4.4.3 Dielectric thickness

Experiments were performed with a thicker dielectric (500 nm instead of 200 nm). They indicated that the 'optimal actuation voltage' as found in Phase II, had shifted to higher voltages.

In general two different mechanisms are at play in the wafers: At low actuation voltages positive charge trapping dominates (probably not in the interposer dielectric but in the substrate or on the surface), giving a negative shift of the CV and causing early failure. At higher voltages, negative charge trapping is also present (in the interposer dielectric) and compensates for the positive charge trapping, resulting in a longer lifetime. The two mechanisms compete with as a result that there is an optimal actuation voltage where they cancel each other maximal.

For thicker dielectrics, the charging of the dielectric reduces (smaller electrical field) and the negative charge trapping reduces. As a result, the optimal voltage shifts to higher values.

Conclusions: A thicker dielectric improves the lifetime: it increases the pull-out voltage causing more room for charging and slows down the charging itself. The thicker dielectric charges less in the same electric field. It traps negative charges, probably in the bulk. The "other" charging mechanism that is present, i.e. with positive charges, probably substrate charging was dominant and caused the stiction. A thicker dielectric causes also a lower C_{down}. The choice of the dielectric thickness should be a trade off between reliability and RF performance.

4.4.4 Planarization

There were several different test structures present in the design which allowed studying the influence of the bridge planarity on the charging on the same wafer.

Planarized structures showed an optimal actuation voltage around 25V, ehich is lower than for non-planarized switches. An optimal actuation voltage is present if there are two charging mechanisms, positive charging (probably in the slots between ground and CPW)

and negative charging (in the bulk of the dielectric interposer). A lower optimal actuation voltage can be due to less influence of the positive charges trapped in the substrate in the slots on the bridge, i.e. on the CV curves.

4.4.5 Substrate charging

Tests on quartz wafers showed that quartz is not a good substrate and charges. The end-of-life of switches tested on quartz is caused by CV narrowing due to charging of the substrate, probably in the slot between CPW and ground.

Also glass substrates show charging, although less fast than quartz.

The best substrate is HR-Si, although also in that substrate there is charging present in the slots. In this case, the charging might cause accumulation or depletion, which will alter the electric field distribution in the slots and thus the force acting on the bridge. The CV-characteristics of switches are sensitive to light, confirming this effect.

Conclusion: It is shown that the type of substrate has a large influence on the lifetime of capacitive RF MEMS switches. The glass wafer shows a lot of charging, probably due to absorbed water (on the surface or/in the bulk). The quartz wafer, a promising candidate from first experiments, turned out to be not so good at higher actuation voltages. HR silicon wafers are the best but still show some charging.

4.4.6 Temperature stability

One of the problems identified during the Phase II study was the thermal stability of the beams. The structures can be heated (Joule heating, external heat sources) and can change the shape due to different beam and substrate coefficients of thermal expansion (CTE). So, the beam will buckle when heated up. We wanted to obtain an estimation of the amount of buckling and the effect of the thickness of the beams on this buckling. Different samples were tested: with 1µm and 2µm thick beams; and on HR-Si and on glass substrate. The main results are listed in Table 1.

Table 1: Maximal deflection ($\mu m \pm 0.1\ \mu m$) of the bridge between room temperature and 60°C.

Maximal deflection ($\mu m \pm 0.1\ \mu m$)	07-028-13 1 µm bridge HR-Si	07-144-01 2 µm bridge HR Si	06_252-01 1 µm bridge glass
Narrow beam 1	7.7	6.20	6.75
Wide beam 1	7.55	6.25	7.40

Conclusions: It is clear that this temperature induced deflection is high. It can result in stiction of the beams to the bottom side of the cap of the zero-level package, if the distance between cap and bridge is low. During the packaging process the temperature seen by the switch will probably be higher, making this failure mechanism very likely to occur.

The deflection is lowest for the thicker beam. This is expected because that beam has a higher stiffness. So, the problem can be reduced by increasing the thickness of the beam. However, this will go together with an increase of pull-in voltage.

The best way to solve this problem is through design. Temperature induced elastic changes of the shape have to be compensated by a proper design of the beams.

4.4.7 Test results packaging

Most RF-MEMS devices were still working after packaging and showed a very good lifetime (Figure 11). Some devices failed because of deformation due to the packaging temperature step. This in some cases caused stiction to the dielectric interposer or to the

bottom of the 0-level cap (depending whether the deformation caused down or upward buckling).

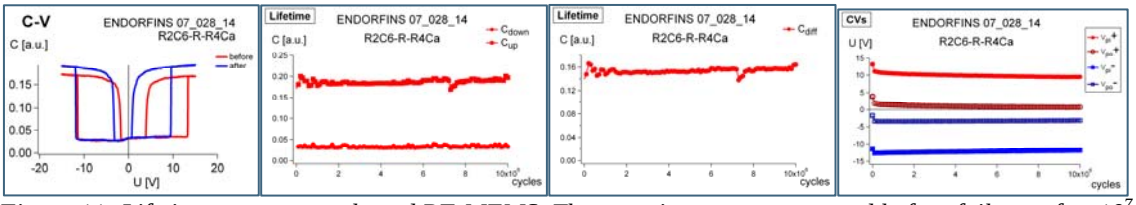

Figure 11: Lifetime test on a packaged RF-MEMS. The experiment was stoppwed before failure, after 10^7 cycles.

Conclusions: First results of lifetime test of the packaged switches show that the packaging step does in general not damage the switches permanently. The bridge deforms during the temperature step, but comes back to its normal position afterwards. In some cases stiction was observed caused by bending of the beams during the packaging temperature step and touching of the beam with the bottom side of the glass cap. Increasing the distance between the beam and the cap, e.g. by increasing the thickness of the BCB layer, will allow avoiding this kind of stiction.

4.4.8 Conclusions from Phase III

The following main findings were obtained:

1. Charging:
    a. a thicker dielectric results in less charging of the interposer dielectric and in a longer lifetime
    b. planarization reduces the effect of charge trapping in the substrate (slot between signal line and ground) on the switch pull-in and pull-out voltages. For this reason it enhances the lifetime. It also increases Vpo which also helps to increase the lifetime
    c. substrate charging cannot be neglected.
2. Temperature induced elastic deformation.
    a. The AlCu bridge is highly sensitive to the temperature. The main problems related to this are that the bridge can deform during packaging, causing stiction to the signal line or to the bottom of the cap. It can also deform during functioning, due to RF power associated heating.
    b. This problem should be solved by design. A cantilever type bridge will for example be much less sensitive to this effect than a clamped-clamped beam.
3. 0-level packaging
    a. The 0-level packaging process has to be optimised for a certain switch/substrate combination by playing with substrate and cap temperature and bonding pressure and time
    b. We demonstrated that 0-level packaging of the switches is possible without affecting their lifetime.

5 General conclusions and recommendations

- Whisker formation can occur in the metal used for the bottom electrode and can be detrimental to the reliability of the devices. It will increase the roughness of the bottom electrode and affect the roughness of the dielectric. It can cause local high electrical fields or even damage in the dielectric. It should be checked on uniform films through roughness measurements (AFM) before and after an anneal step. The temperature of the anneal step should be the same as the maximal temperature seen by the device during the processing. The tests should also be done with dielectric on top of the metal.

- One of the most important findings of ENDORFINS is the presence and influence of substrate charging on the actuation and reliability of the (RF-)MEMS devices. The substrate first of all highly affects the pull-in voltage because it influences the field distribution between actuation electrode and MEMS armature. Secondly, charging clearly occurs in the substrate. It even often dominates the charging taking place in the dielectric interposer. This explains why the lifetimes of MEMS devices using different dielectrics but the same type of substrate are often comparable.

- We found a new failure mechanism: stiction of the beams to the bottom of the 0-level cap due to thermal expansion. The thermal expansion problem of the bridge has to be taken into account in the design phase. This design should be such that this expansion has minimal effect on the shape and position of the bridge. Simple experiments checking the shape of the bridge in function of temperature are recommended.

- We clearly showed that measuring the lifetime of capacitive RF-MEMS switches by monitoring only the up and down state capacitance, as is commonly done all over the world, is NOT the correct measurement methodology. It only gives the correct information on lifetime when there is only one uniform charging mechanism and when all relevant parameters are given (test frequency, duty cycle, environment). It is mandatory to check the deformation of the CV curves during testing, i.e. the shift of the pull-in and pull-out voltages (both positive and negative).

- Finally, although the design was not optimal (it had to allow for a very broad processing range with many different test structures) the finally obtained lifetimes are very good: ~10^8 at 100Hz switching, 50% duty cycle. They can still be improved through design optimization for the chosen process.