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D O C U M E N T

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HEAVY ION SINGLE EVENT EFFECTS IN UCC1806 PWMs

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1 SUMMARY

ESA contractor X uses the BiCMOS circuit UCC1806 in a design where the Single Event Effect (SEE) behaviour, in its particular implementation, is unknown.

The UCC1806 is a Low Power, Dual Output, Current Mode, Pulse Width Modulator (PWM) controller. This circuit is used in several critical applications, within running ESA projects.

In order to radiation SEE evaluate the UCC1806, a test campaign was organised at the European Heavy ion Irradiation Facility (HIF) at the University Catholique de Louvain, Louvain-la- Neuve, Belgium, March 9, 2004. Unitrode and Texas Instruments PWM's were tested for occurrences of hard- or soft failures. Two different test set-ups were used. Both are DC/DC converter applications run in a closed loop mode, and one of them simulating the biasing conditions of contractor X application.

Main conclusions can be summarised to:

Hard errors

No Single Event Latch-up (SEL) or hard errors were observed in any of the tests up to a Linear Energy Transfer (LET) test level of 68 MeV/(mg/cm^2).

Soft errors (as being characterised for contractor X application)

Soft errors are observed with more or less criticality depending on implementation and application. Three types of soft error were observed:

1) Single Event Upset (SEU) causing a single-pulse PWM dropout. The consequence on the output voltage of the DC/DC converter is minor, since a correctly designed output-capacitor will reduce the voltage drop transient to be in the order of ~ 100mV. The criticality is **minor**.

2) SEU causing a ~5ms interruption of the PWM control, but re-starts automatically after the dead period defined by the implementation of the contractor X design. This SEU behaviour causes for a normal design a **total discharge** of the output voltage capacitors, and the DC/DC voltages will drop to ~0V in an unpredictable way (unless a low resistive pull-down exists). The criticality is **minor or major** depending on the user application.

3) When biasing the UCC1806 current measurement ($V_{PIN4} – V_{PIN3}$) with voltage levels >500 mV, an SEU transient behaviour on the DC/DC converter output voltages is observed of what is assumed to be induced and determined by the control loop (i.e. the analogue amplifiers/comparator inside the UCC1806). The typical DC/DC converter propagation on the output voltages is a 1-3 ms negative voltage transient. For our ESTEC test converter the transient amplitude is ΔV ~ 1V on the +5V, which is below the normal reset-level of +5V digital circuits. The occurrence rate seems to be 10 times higher compared to the SEU phenomenon described in 2). The criticality is **minor or major** depending on the user application.

2 INTRODUCTION

This report presents the results of an ESTEC initiated SEE test programme carried out on UCC1806 PWMs operated under flight application conditions. Tests were conducted at the European HIF facility at UCL, Belgium, March 2004, on flight lot samples. Both Unitrode and Texas Instruments marked samples were tested.

2.1 SCOPE

- To test and verify one UCC1806 sample using a TERMA test board set-up.
- To test and characterise UCC1806 samples under flight application conditions using an ESTEC test board set-up.
- To test samples both marked Unitrode and Texas Instruments.

2.2 OBJECTIVES

2.2.1 Main

- To prove no hard-failure occurrence under test conditions representative for contractor X implementation of the UCC1806 – up to a LET of 34 MeV/(mg/cm^2).
- To prove no hard-failure occurrence under test conditions in the TERMA implementation of the UCC1806 - up to a LET of 34 MeV/(mg/cm^2) – but with the decoupling capacitors modified and similar to contractor X's implementation.

2.2.2 Secondary

- To characterise as many soft-error phenomenon as possible
- To quantify the soft-error event occurrence
- To propose methods of preventing SEE in DC/DC converter design implementation

2.3 TEST SAMPLES

Two different lot date codes were available for tests of UCC1806. Samples tested carried the following marking:

Unitrode samples	Texas Instrument samples
- 8A9845	- 1A-T 0126C
- UCC1806 J/883B	- 5962-9457501 MEA
- 5962-9457501 MEA	- UCC1806 J/883B
- **U Q** (Unitrode)	- **THA Q** (Texas Instruments)

Table 2.3-1

Both versions used dies with the following identifications – M UICC 92 C1806 UICC – and both were assembled in CERDIP DIL16 packages.

2.4 HEAVY ION TEST FACILITY

Heavy ion testing was carried out at the CYCLONE Cyclotron at University Catholique de Louvain, Belgium (UCL0403) using the Heavy ion Irradiation Facility [1].

Ions available at the HIF together with their main characteristics can be found in the **Table 2.4-1**. Ions marked in bold were used during the UCC1806 tests. By tilting, the UCC1806 under test an effective LET range of 14.1 to 68.0 MeV/(mg/cm^2) could be covered by the two ions used.

Ion Cocktail M/Q=4.94	Energy MeV	Range µm Si	LET MeV(mg/cm²)
$^{10}B^{2+}$	41	80	1.7
$^{15}N^{3+}$	62	64	2.97
$^{20}Ne^{4+}$	78	45	5.85
$^{40}Ar^{8+}$	**150**	**42**	**14.1**
$^{84}Kr^{17+}$	**316**	**43**	**34.0**
$^{132}Xe^{26+}$	459	43	55.9

Table 2.4-1 UCL – HIF Ion Cocktail #1 produced for ESA

2.5 JUSTIFICATION FOR THE UCC1806 SEE TEST CAMPAIGN

ESTEC's concern regarding permanent heavy ion damage in **UCC1806** was based on test results obtained back in 2000 [2]. These tests were carried out by ESTEC/TERMA on various types of PWMs in support of the ROSETTA project.

Within the ROSETTA heavy ion test campaign, their implementation of the **UCC1801** circuit was found to fail. The failure mechanism was concluded to be a Single Event Burnout (SEB) in the output drive transistors, and depended on the energy stored in the decoupling capacitor connected to the power supply pin of the **UCC1801** circuit.

The hard-failure sensitivity of the ROSETTA **UCC1801** application was found being reduced to a zero level by decreasing the decoupling capacitor value to the power supply pin of **UCC1801**.

Given the fact that the **UCC1806** is derived from the same Unitrode circuit family (BicMOS technology), ESTEC expected that there might be a risk of having the same failure mechanism in this circuit. During an ESTEC review, the **UCC1806** was found to be the essential part of a design from contractor X.

In the earlier ESTEC/TERMA test campaign [2], also one UCC1806 implementation was tested. However, that test was not representative for the implementation of the contractor X design, since the decoupling capacitors and the other circuit biasing is not identical.

- The TERMA test board is re-used for the 2004 test campaign, but modified to have the same decoupling capacitance and impedance on the power pins as the contractor X implementation.

- The ESTEC test board is built-up in order to bias the UCC1806 as far as possible in same conditions as the contractor X type DC/DC converter, and with correct decoupling capacitors.

The power supply scheme for contractor X implementation of the UCC1806 chip in the design is as shown in **Figure 2.5-1**.

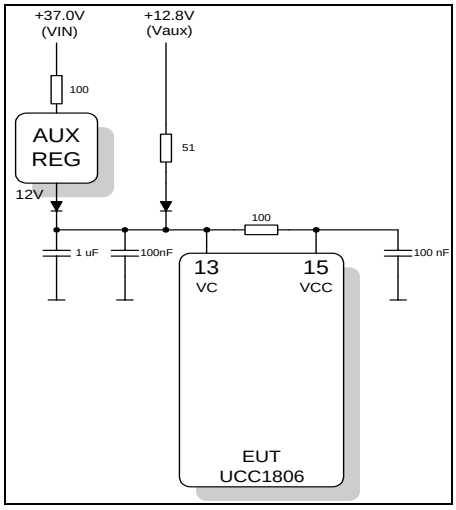


Figure 2.5-1

2.6 TERMA TEST BOARD - DESCRIPTION

The equivalent circuit for the modified TERMA board is given below:

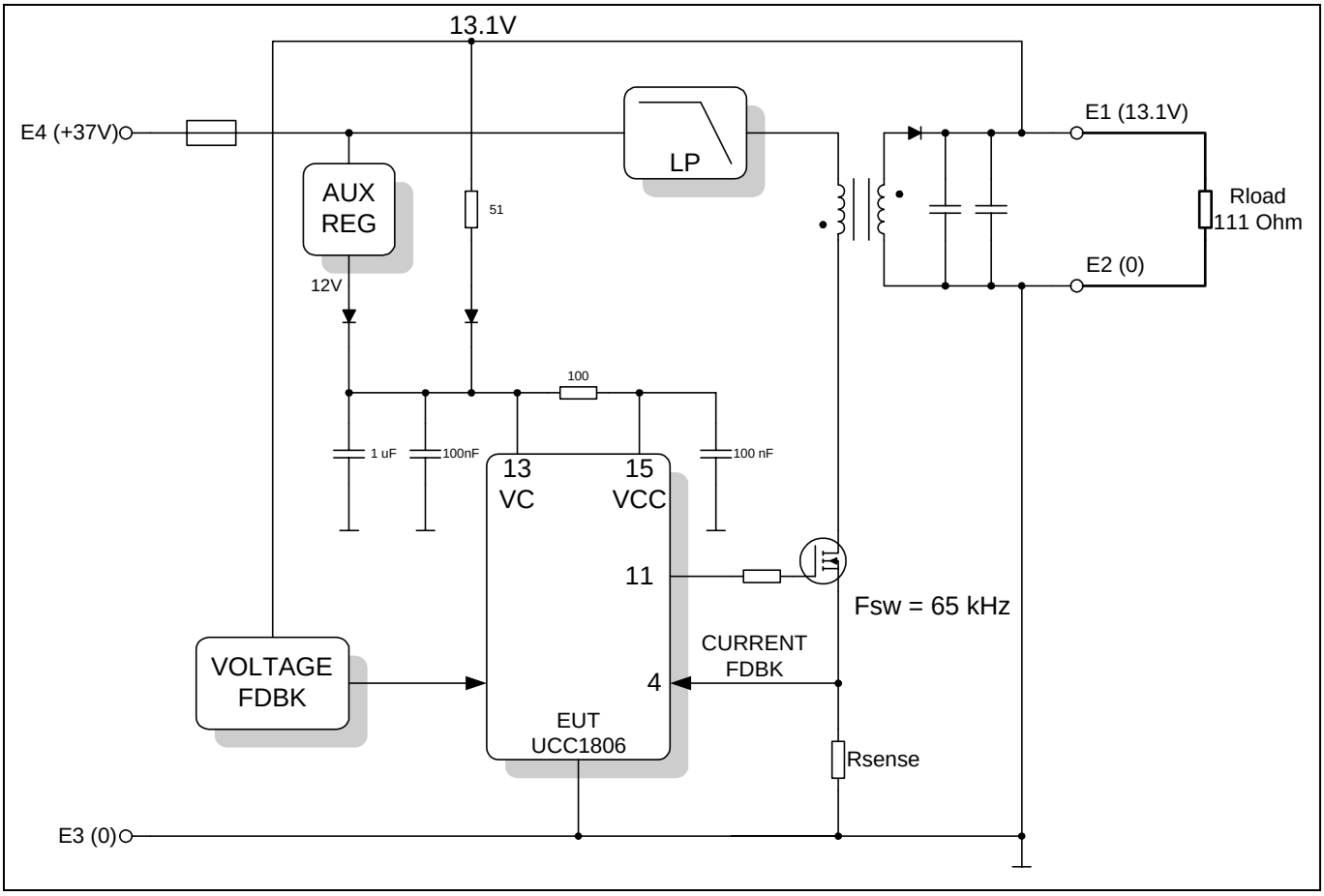


Figure 2.6-1

- The test converter is of Flyback topology, and designed for a low load application < 2W
- After start-up, the 13.1V output will supply the VC via 51 Ohm // (1uF+100nF) and the VCC via an additional 100 Ohm // 100nF.

2.7 ESTEC TEST BOARD - DESCRIPTION

The equivalent circuit for the ESTEC board is given below:

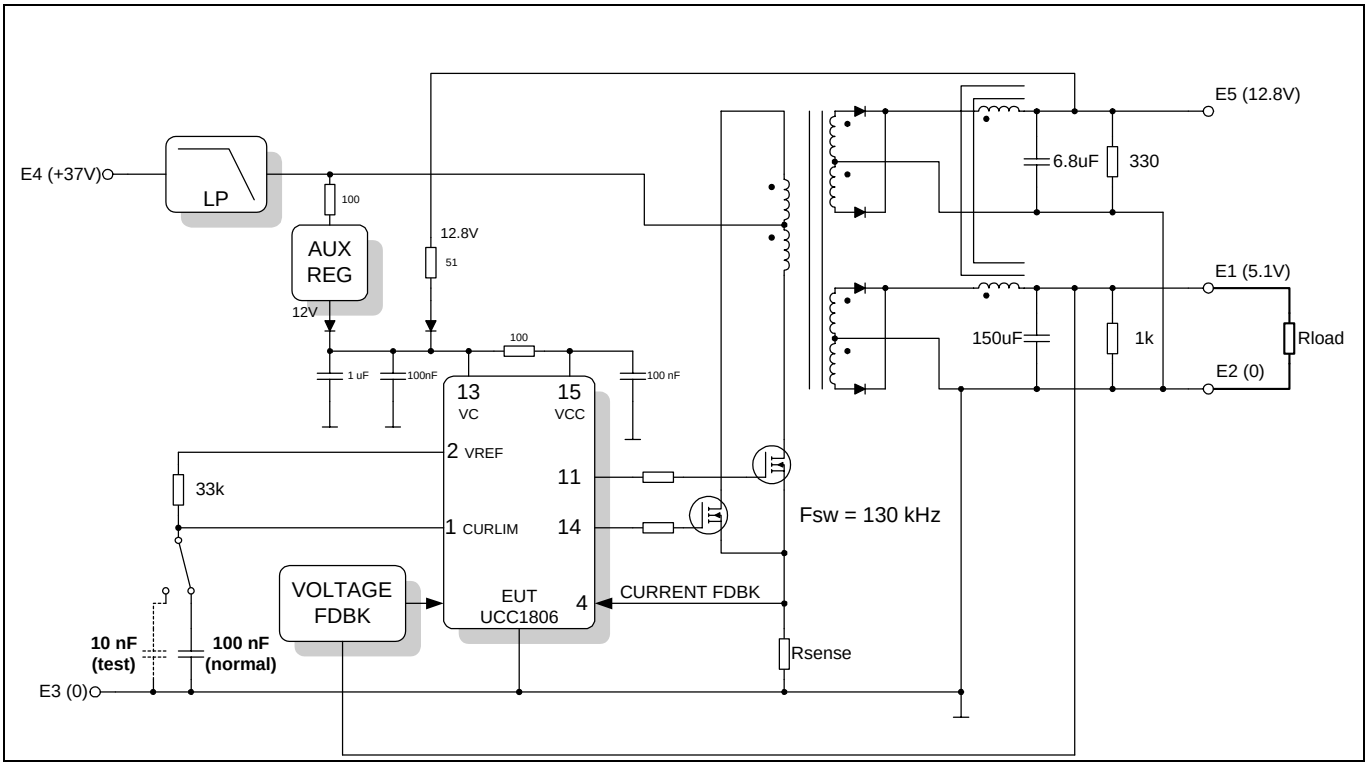


Figure 2.7-1

- The test converter is of Push-Pull topology, and is designed for a load application 0 – 10 W
- The R_{sense} has been scaled to bias the current feedback pin as the contractor X application does for a 25W push-pull converter.
- All other component values and pin level biasing of the UCC1806 has been made to copy contractor X application.
- After start-up, the 12.8V output will supply the VC via 51 Ohm // (1uF+100nF) and the VCC via an additional 100 Ohm // 100nF.

2.8 ESTEC TEST BOARD – LOAD DEFINITION

The R_{sense} value has been scaled up with a factor of 5, to easily simulate different biasing conditions on PIN4.

The default biasing set-up of PIN 4 (current feedback pin) is a level identical to the contractor X case. This load case simulates running a 25W converter for the contractor X application. The default load case is "**LOAD 1**".

In addition to this, for some comparison tests (see 4.4.2) the converter is loaded with a low load, "**LOAD 0**". Taking the R_{sense} scaling into account, the **LOAD 0** corresponds on the PIN 4 biasing simulating a 5W application of the contractor X converter.

LOAD 0 Simulates 5W Application for contractor X

LOAD 1 Simulates 25W Application for contractor X – **The real output load is +5V @ 1A**

LOAD 2 - 4 Increased voltage levels on the current feedback pin. See Figure 2.8-1

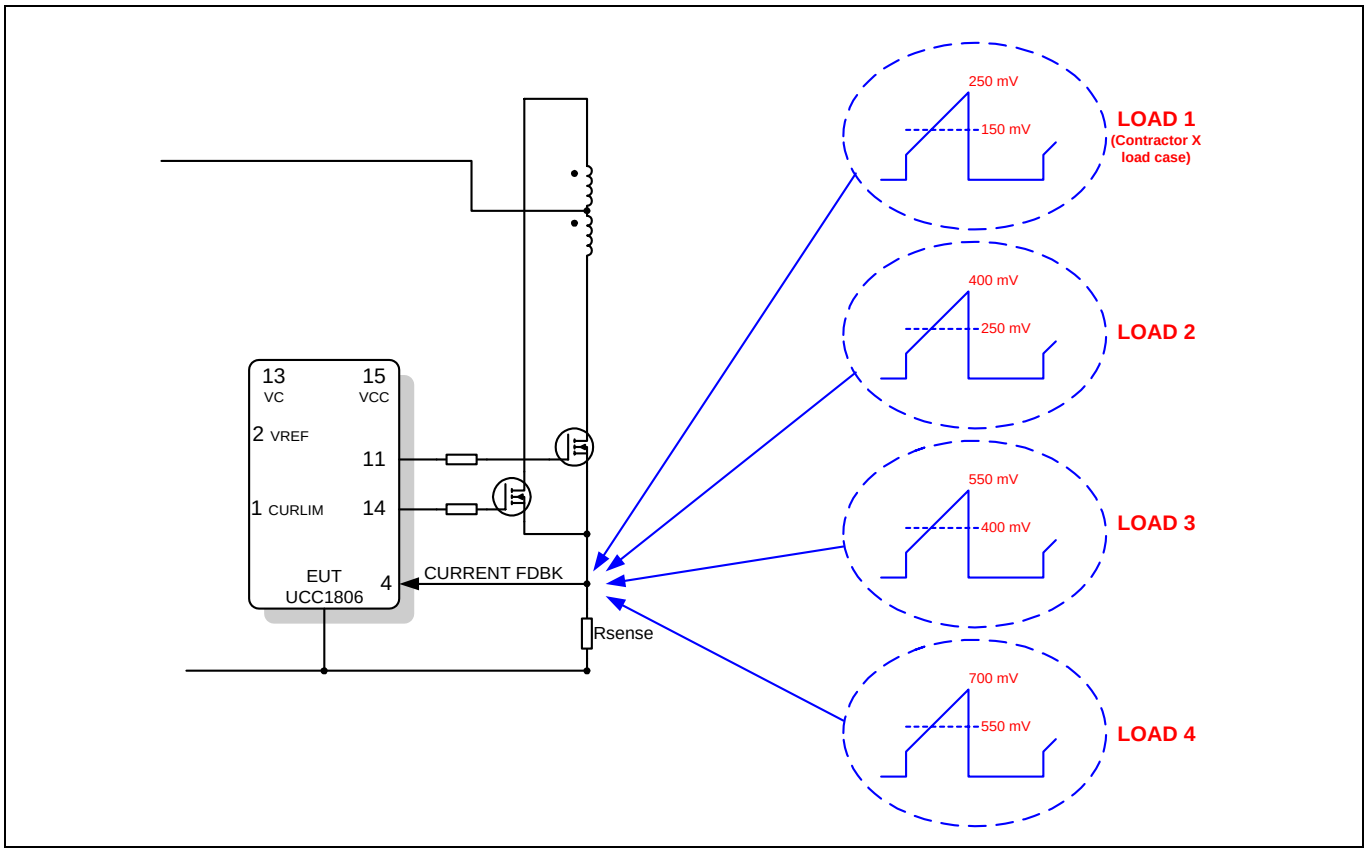


Figure 2.8-1

2.9 EXPECTED SEE TRANSIENTS IN UCC1806

All assumptions on UCC1806 internal design are based on [3].

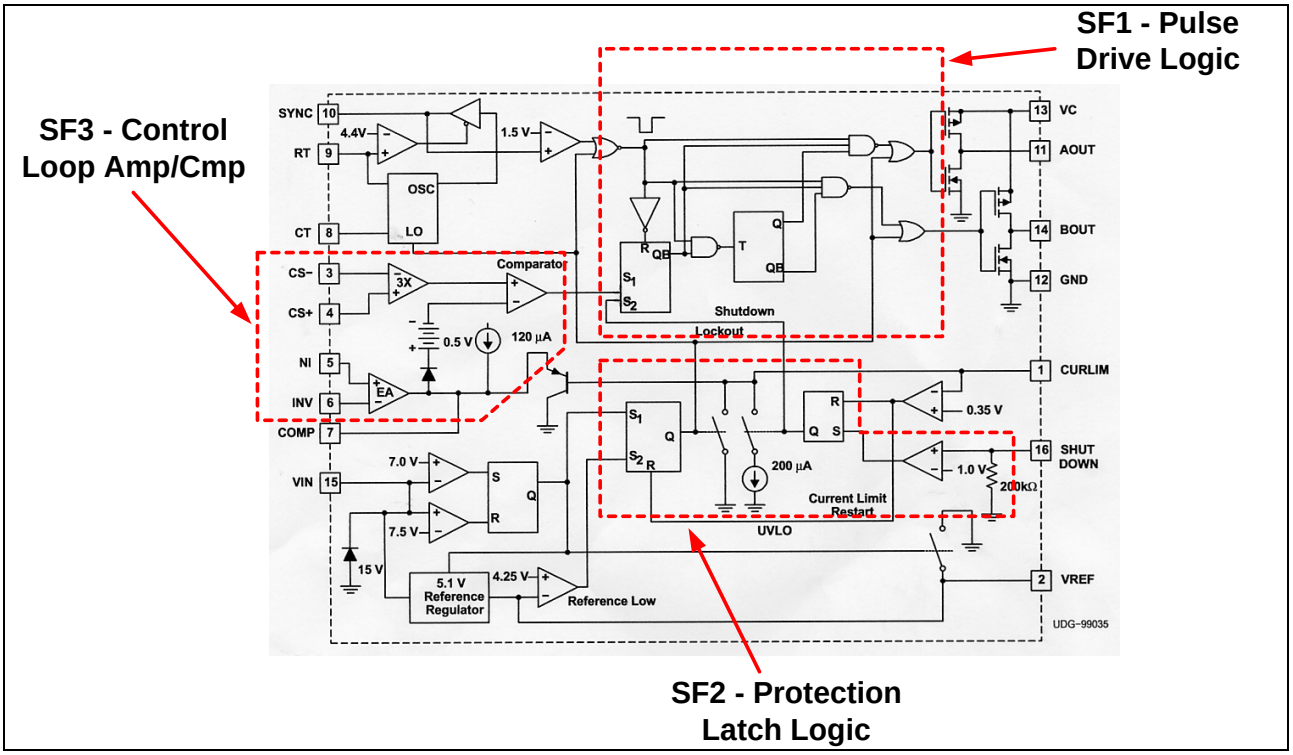


Figure 2.9-1

We expect any presumptive hard failure ("**HF**") to be observed as Single Event Latch-up (SEL) on a power supply pin. We expect any presumptive soft failure being generated from any of three different parts of the circuit

1) "**SF1**" Area - Any SEU 0/1- bit-flip will change the state on one of both the output stages "AOUT" and "BOUT". This means that both A- and B-outputs can be put wrongly into a 0-0 or 1-1 state due to an SEU. The erroneous state will always be restored into a correct state at the next PWM clock-pulse.

2) "**SF2**" Area – Any SEU 0/1- bit-flip will interrupt the output stage into a 0-0 state. The PWM operation is not restored until the PIN1 has been pulled down below the 0.35V limit on the dedicated comparator.

3) "**SF3**" Area – An SEU has the possibility to drive the analogue amplifiers and comparators into stack-high/low on their outputs. The duration of restoring this event sets the criticality. If an operational amplifier is driven into stack-high/low, the restoring time will be in order of magnitude of the slew rate time of the amplifier. Furthermore, the design of the feedback circuit in the voltage/current control loop will affect the restoring behaviour into normal performance of a DC/DC application control loop.

3 TERMA TEST BOARD

3.1 SEE RESULTS OF UCC1806 / UNITRODE #01

LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3
14.1	Ar - 0º	5.0x10^6	#01	1.5	0	Note (1)	Note (2)	0
28.2	Ar - 60º	1.0x10^6	#01	1.5	0	Note (1)	Note (2)	0
34.0	Kr - 0º	1.0x10^6	#01	1.5	0	Note (1)	Note (2)	0
48.1	Kr - 45º	1.0x10^6	#01	1.5	0	Note (1)	Note (2)	0
68.0	Kr - 60º	1.0x10^6	#01	1.5	0	Note (1)	Note (2)	0

Table 3.1-1

Note(1): The effect of 1-clock cycle drop out on the PWM output switching was observed. The characterisation of this event is recorded in detail, but the number of events has not been recorded. See text in paragraph 3.2.1

Note (2): See text in paragraph 3.2.2

3.2 SOFT FAILURE CHARACTERISATION

3.2.1 SF1 TERMA - PWM clock cycle drop-out

As can be seen from Figure 3.2-1, the interrupted UCC1806 switching is restored automatically. Here the case is a “1-clock cycle” interruption. The voltage-drop amplitude is determined by the configured output current and the output capacitance value together with our resistive load.

The TERMA board has in a 120 mA resistive load @ 13.1V, a 30uF output capacitance, and the dropout time is 17us. This yields theoretically resistive discharge of the capacitors: $\Delta V = -70mV$.

The theoretical drop is close to the measured. The rest of the voltage transient is because the voltage control loop has to recover back dynamically.

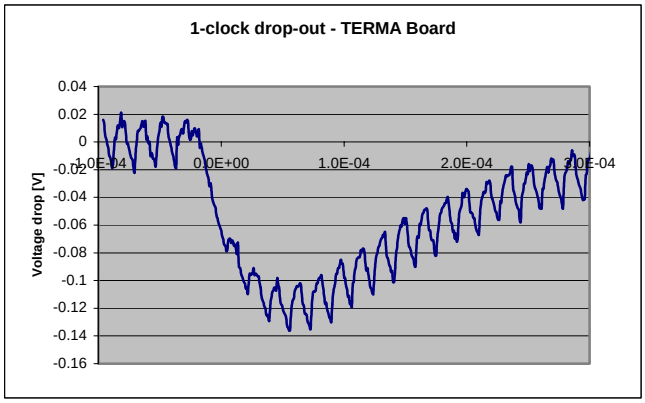


Figure 3.2-1

The number of events was not recorded, since the 1-cycle dropout is not a critical transient. A correctly sized output capacitor vs. load will cover the needed energy to be within specified voltage.

Occasionally, an interruption of the PWM clock was observed, that seems to be a “burst” of single clock interruptions.

This event causes a slightly bigger drop in output voltage, but has the same character and order of magnitude as the single clock interruption. The DC/DC voltage control loop recovers the voltage drop fully within time duration of < 1ms, which is the expected response.

If the multiple PWM clock disturbance is a burst sequence of SEUs, or rather a control loop anomaly, can however not be concluded in this experiment with the TERMA board.

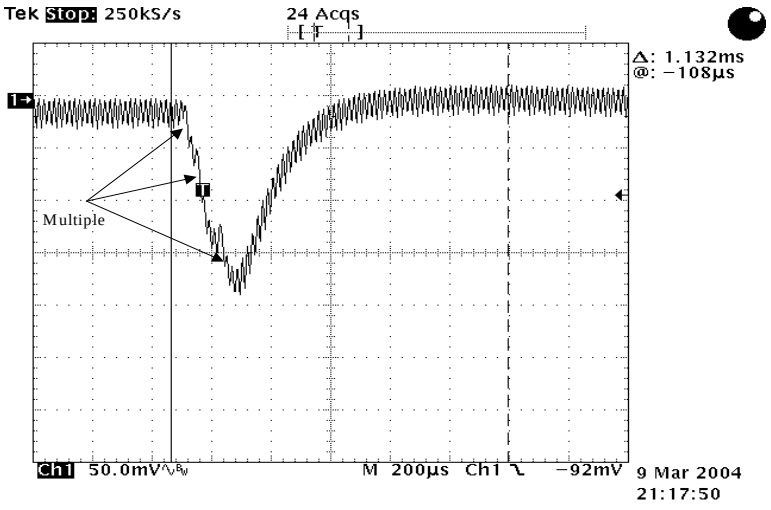
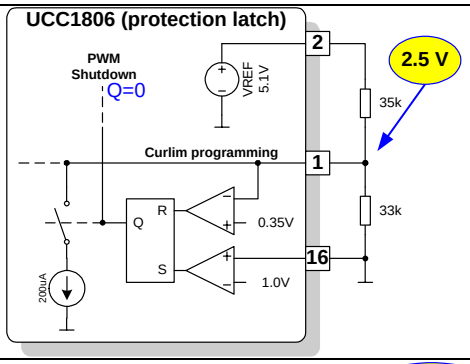
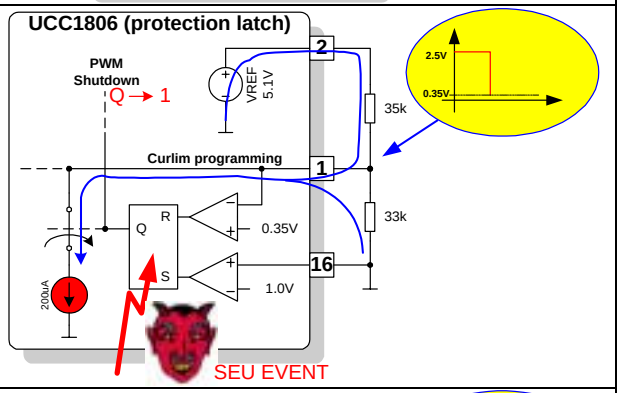
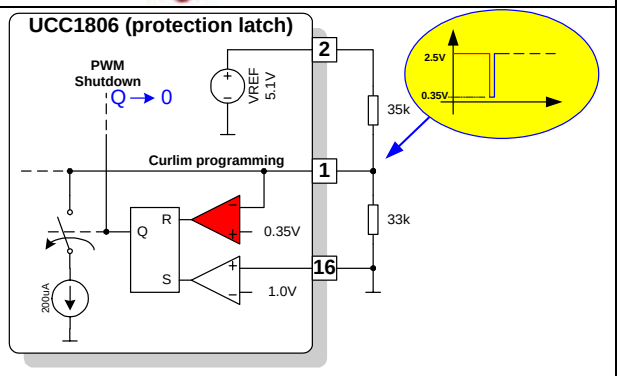


Figure 3.2-2

3.2.2 SF2 TERMA - SEU Latching of PWM clock

This explains the mechanism of SEU in the protection latch, and how it could affect the TERMA application.

The TERMA board is implemented in such a way that a protection-latch SEU inside UCC1806 will be restored instantly or at least within one clock cycle. The implementation of UCC1806 has <u>no capacitance</u> connected to the voltage on PIN1 In its original state, when PWM is operating correctly, the voltage on PIN1 is 2.5 VDC.	
The SEU event, affecting the RS-latch to enter Q = 1. 1) The switch closes immediately. 2) The current source (red) will be pulling down the node on PIN1 due to high source resistance (blue current) 3) When the voltage has fallen down to +0.35V, the RS-latch will be restored (see next picture…).	
When the 0.35V comparator has been activated, the switch opens and the 200 uA current source is interrupted - The node in PIN1 jumps back into normal mode 2.5V. The (pulse) time duration of this reset event is dependant on the delays in the comparator and the RS latch + stray-capacitances on PIN1. If the pull-down on PIN1 coincides with the normal PWM-pulse start, a single PWM-pulse will be lost.	

This means that by observing SEE on the TERMA test board - **we cannot distinguish if an SEU is present in the protection latch (SF2) or in the PWM output switching logic (SF1).**

No further test or set-up was made to separate the two mechanisms on the TERMA board.

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3.2.3 SF3 TERMA – SEU Control loop transient

During the tests of the TERMA board, no SEE was observed on the output voltage that can be assumed caused from a UCC1806 control loop component SEU.

The TERMA test board runs with maximum amplitude of 380 mV on the current feedback pin (PIN4).

4 ESTEC TEST BOARD

4.1 SEE RESULTS OF UCC1806 / UNITRODE #03

LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT HF	SF1	SF2	SF3
14.1	Ar - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	6	0
14.1	Ar - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
19.9	Ar - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
19.9	Ar - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
28.2	Ar - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	21	0
28.2	Ar - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	16	0
34.0	Kr - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	16	0
34.0	Kr - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	21	0
48.1	Kr - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	23	0
48.1	Kr - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	18	0
68.0	Kr - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	24	0
68.0	Kr - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	26	0

Table 4.1-1

Note (3): The effect of 1-clock cycle drop out on the PWM output switching was not recorded.

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4.2 SEE RESULTS OF UCC1806 / TEXAS INSTRUMENTS S/N #TI4

LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3 Note (5)
14.1	Ar - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	6	0
14.1	Ar - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	11	0
19.9	Ar - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	15	0
19.9	Ar - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	9	0
28.2	Ar - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	21	0
28.2	Ar - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	15	0
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	10	0
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	18	0
48.1	Kr - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	22	0
48.1	Kr - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	24	0
68.0	Kr - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	18	0
68.0	Kr - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	21	0
EXTENDED TESTS / PIN4 VOLTAGE BIASING SESITIVITY								
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	19	0
68.0	Kr - 60º	5.0x10^5	#TI4	LOAD1	0	Note (4)	20	0
34.0	Kr - 0º	5.0x10^5	#TI4	LOAD2	0	Note (4)	13	1
68.0	Kr - 60º	5.0x10^5	#TI4	LOAD2	0	Note (4)	13	0
34.0	Kr - 0º	5.0x10^5	#TI4	**LOAD3**	0	Note (4)	5	**~100**
68.0	Kr - 60º	5.0x10^5	#TI4	**LOAD3**	0	Note (4)	21	**~120**
34.0	Kr - 0º	1.0x10^6	#TI4	**LOAD4**	0	Note (4)	18	**~200**
68.0	Kr - 60º	5.0x10^5	#TI4	**LOAD4**	0	Note (4)	19	**~150**

Table 4.2-1

Note (4): The effect of 1-clock cycle drop out on the PWM output switching was not recorded.

Note (5): Trigger detection level for the negative transients was set to –0.5V

4.3 SEE RESULTS OF UCC1806 - SF2 SUMMARY

Figure 4.3-1 summarises the SF2 results of Table 4.1-1 and Table 4.2-1.

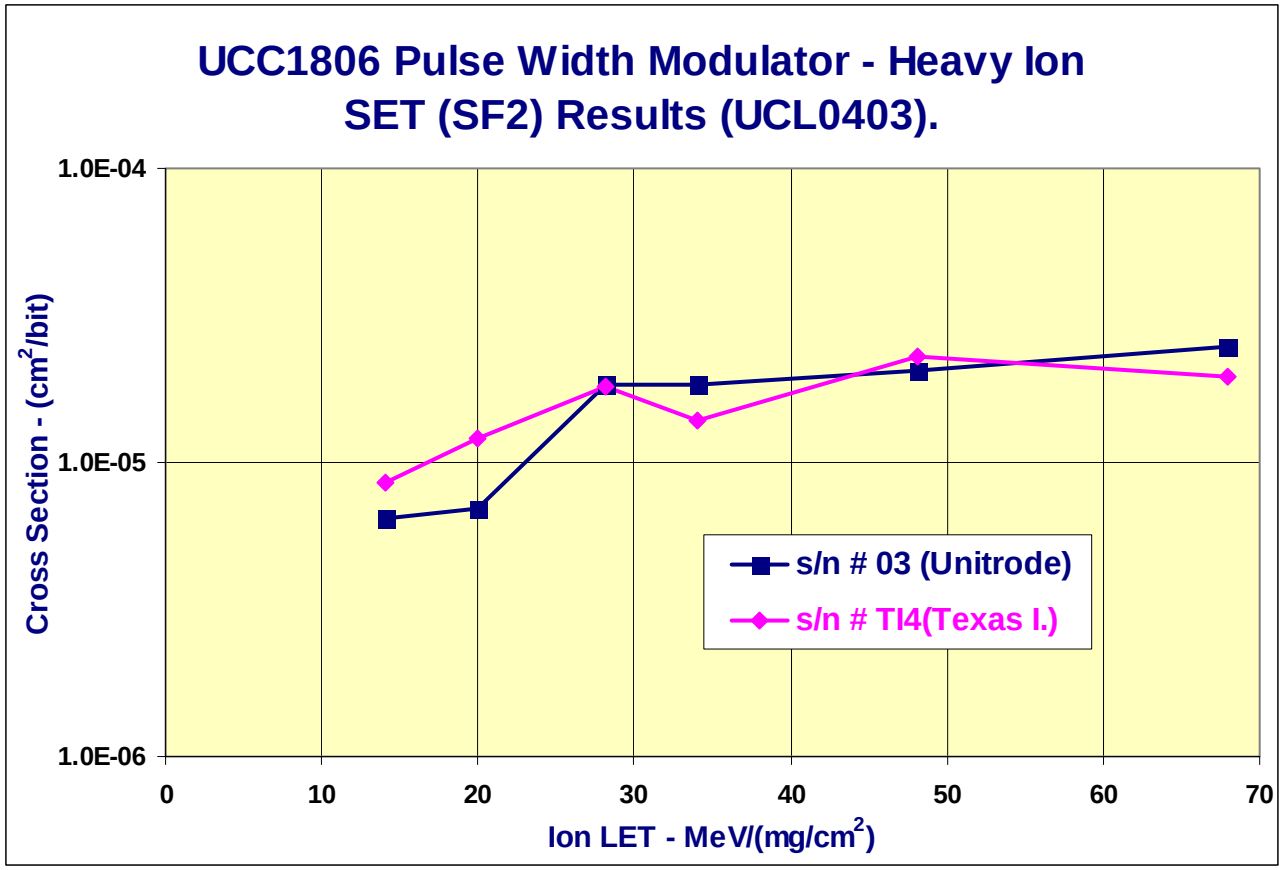


Figure 4.3-1

4.4 SOFT FAILURE CHARACTERISATION

4.4.1 SF1 ESTEC - PWM clock cycle drop-out

The occurrence 1-clock soft failures on PWM outputs are previously proven during tests with the TERMA test board. Since the low-voltage dropouts are non-critical, the events have not been recorded in the test sessions.

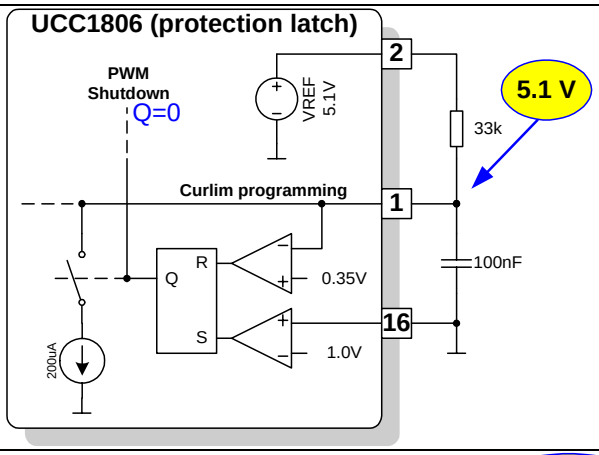
The SF1 event resistive discharge drop value of a on a +5V output @ 1A with C_{out} = 150uF is in the order of:

- 1-cycle drop-out $\Delta V = -0.05V$

4.4.2 SF2 ESTEC - SEU latching of PWM clock

The ESTEC board is implemented in such a way that a protection-latch SEU inside UCC1806 will be restored with a time delay, which is determined by a 100 nF capacitor and the 33k resistor.

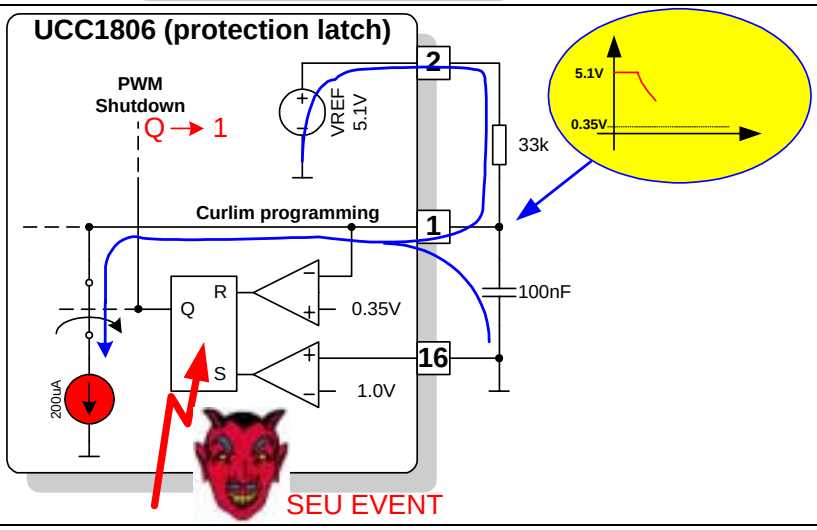
In its original state, when PWM is operating correctly, the voltage on PIN1 is 5.1 VDC.



The SEU affects the RS-latch (Q->1).

A discharge of the 100nF capacitor starts via the 200uA current source (red).

The discharge of the capacitor is an almost linear discharge, but has also a small exponential component due to the 33k pull-up resistor.

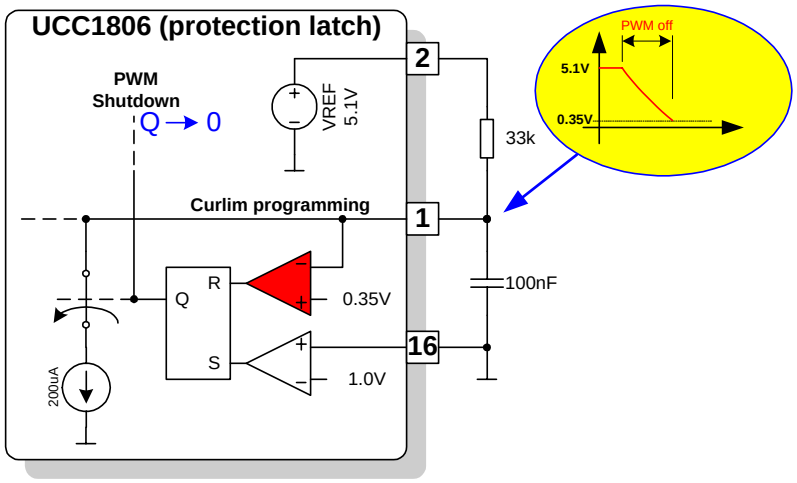


When reaching the +0.35V limit, the comparator is activated, and the RS-latch is restored into Q = 0. During the whole discharge of the 100nF capacitor, the PWM clocking is interrupted.

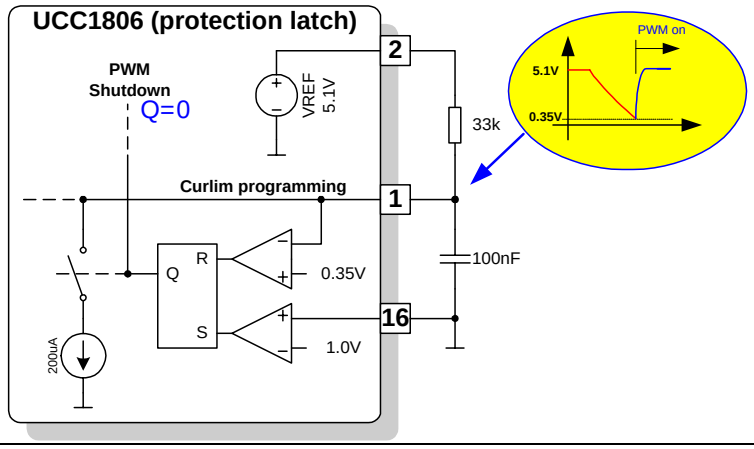
Assuming tolerances:

- VREF 5.1V +/- 1%
- CURR 200 uA +/- 5%
- CAP 100nF +/- 10%
- RES 33.0k +/- 2%
- CMP 0.35V +/- 20mV

The theoretical WCA interval (Monte-Carlo analysis) of the PWM interruption time is 3 - 7 ms.



After restoring the RS-latch, the PWM is operating normally.



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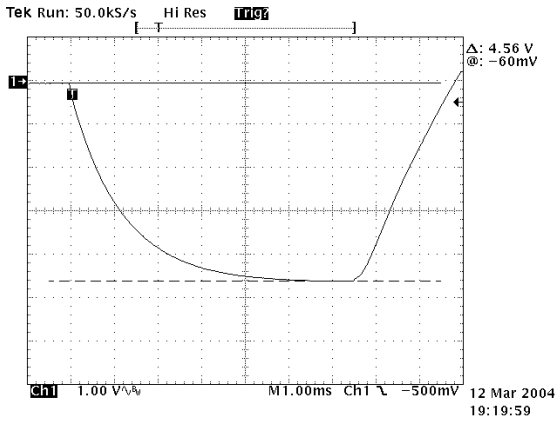
The following graphs illustrate the **+5V output voltage** during the SEU interruption of the PWM clock

Experimental data:

- Sample: Texas Instruments s/n #TI4
- LOAD1 **(+5V @ 1A load)**
- LET 34 MeV/(mg/cm^2)

The dropout time duration (i.e. PWM clock interruption) is ca 6.5 ms.

The result is a **–4.6V drop** on the +5V output voltage. **This is the typical scenario on contractor X application.**



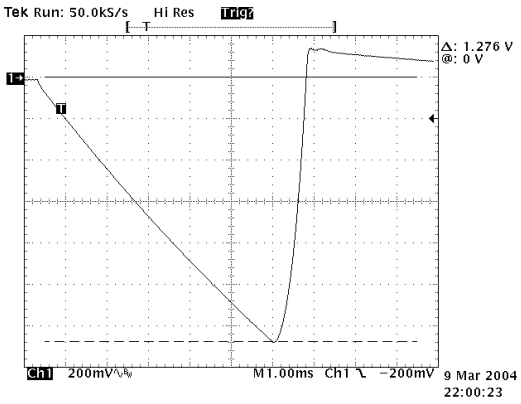
The contractor X application discharges all outputs close to 0V for a typical SF2 event!

Experimental data:

- Sample: Texas Instruments s/n #TI4
- LOAD0
- LET 34 MeV/(mg/cm^2)

The result is a **–1.3V drop** on the +5V voltage.

The time duration is now ca 5.6 ms. (therefore it seems also to be load dependent – due to different biasing of the UCC1806)

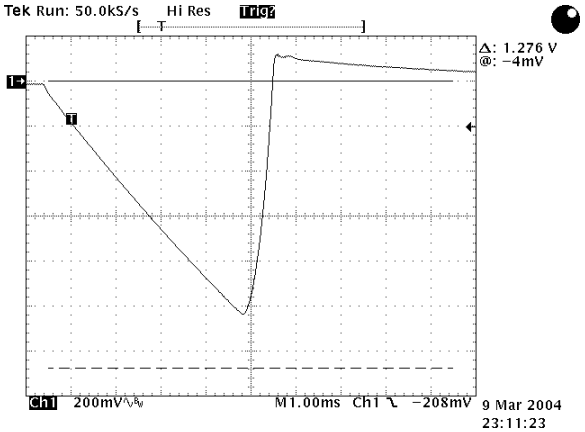


Experimental data:

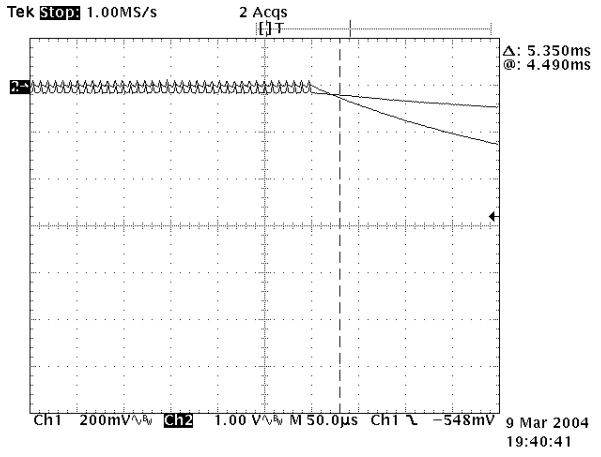
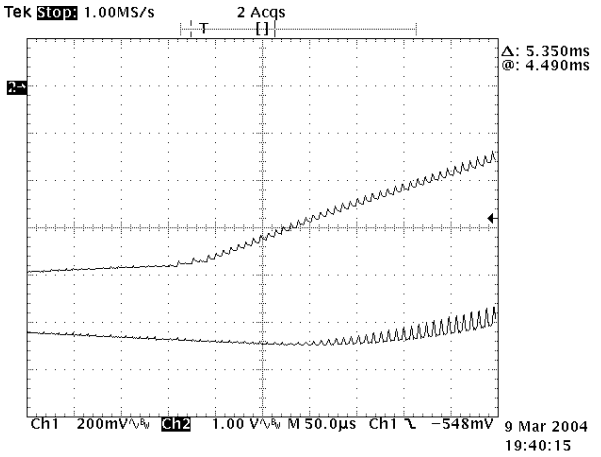
- Sample: Unitrode s/n #03
- LOAD0
- LET 34 MeV/(mg/cm^2)

The time duration is ca 4.5 ms. The difference in dropout time is assumed to be due to UCC1806 parameter tolerances differences.

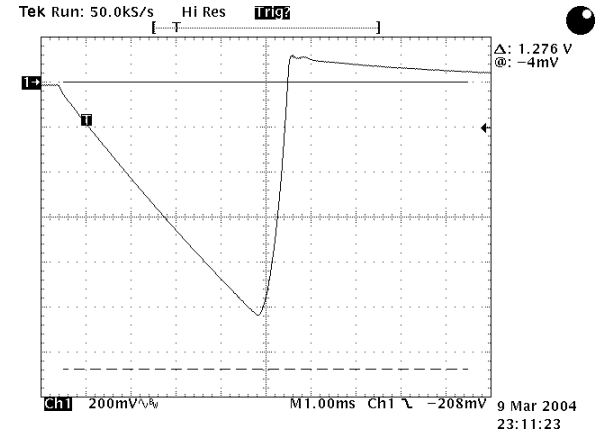
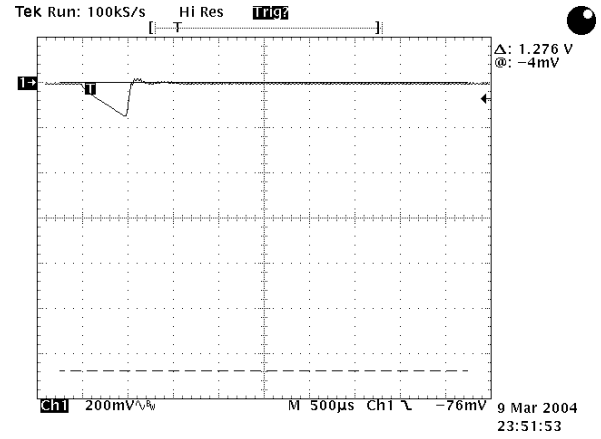
The result is a **–1.0V drop** on the +5V voltage.



To be sure that the voltage drop behaviour really is due to a SF2-SEU interruption of the PWM clock, and not a control loop anomaly – the time scale was stretched to show the PWM operating the sequence ON / OFF / ON.

PWM clock stopped	**PWM clock restarts**
	

To further prove that this is really the protection latch SEU as been assumed, the 100nF capacitor was changed in to a 10nF capacitor on PIN1. This should change the PWM clock OFF-time to a 1/10 of the previous value.

- **UNITRODE s/n #03 & PIN1 = 100nF**	- **UNITRODE s/n #03 & PIN1 = 10nF**
	

The PWM interruption decreases to 0.5 ms, compared to the previous 5 ms - **QED**.

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4.4.3 SF3 ESTEC - SEU Control loop transient

The following SEE has been recorded during test. All explanations are however for this time being assumptions

Increasing the biasing voltage level on PIN 4 by using the increased level load case LOAD2 – LOAD4, yields a new SEU phenomenon on the output voltage.

The output voltage reveals a transient behaviour, which cannot be explained by any PWM 1-cycle or 2-cycle pulse dropout. The assumption currently being is that the control loop amplifiers are sensitive to the heavy Ions causing an anomaly where the output voltage is regulated into a transient behaviour.

- (ESTEC Assumption) The voltage decrease time duration is in the order of 100 – 200 us, and could correspond to the slew rate effect in the SEU affected error amplifiers.

- (ESTEC Assumption) The recovery time of the voltage transient (ca 1ms) is corresponding to the DC/DC converter control loop bandwidth.

When trigging the oscilloscope on a negative –0.5V level from nominal voltage (typically a critical RESET-level), the typical transients behaviour is as shown in Figure 4.4-1.

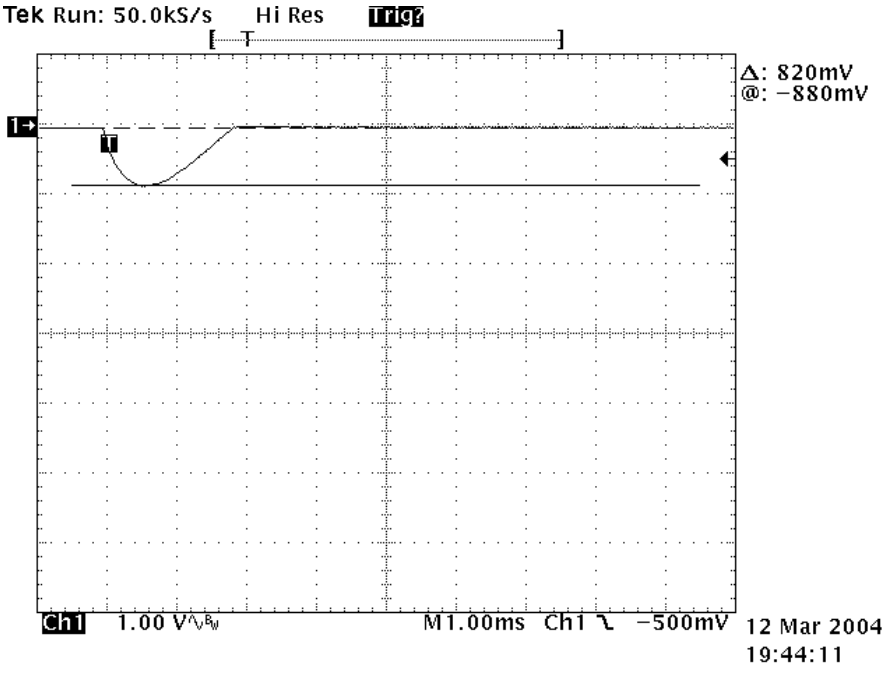


Figure 4.4-1

5 CONCLUSIONS

5.1 RESULTS

Hard errors

No Single Event Latch-up (SEL) or hard errors were observed in any of the tests up to a Linear Energy Transfer (LET) test level of 68 MeV/(mg/cm^2).

Soft errors (as being characterised for contractor X application)

Soft errors are observed with more or less criticality depending on implementation and application. Three types of soft error were observed:

1) Single Event Upset (SEU) causing a single-pulse PWM dropout. The consequence on the output voltage of the DC/DC converter is minor, since a correctly designed output-capacitor will reduce the voltage drop transient to be in the order of ~ 100mV. The criticality is **minor**.

2) SEU causing a ~5ms interruption of the PWM control, but re-starts automatically after the dead period defined by the implementation of the contractor X design. This SEU behaviour causes for a normal design a **total discharge** of the output voltage capacitors, and the DC/DC voltages will drop to ~0V in an unpredictable way (unless a low resistive pull-down exists). The criticality is **minor or major** depending on the user application.

3) When biasing the UCC1806 current measurement ($V_{PIN4} – V_{PIN3}$) with voltage levels >500 mV, an SEU transient behaviour on the DC/DC converter output voltages is observed of what is assumed to be induced and determined by the control loop (i.e. the analogue amplifiers/comparator inside the UCC1806). The typical DC/DC converter propagation on the output voltages is a 1-3 ms negative voltage transient. For our ESTEC test converter the transient amplitude is ΔV ~ 1V on the +5V, which is below the normal reset-level of +5V digital circuits. The occurrence rate seems to be 10 times higher compared to the SEU phenomenon described in 2). The criticality is **minor or major** depending on the user application.

5.2 METHODS OF PREVENTING SEE IN UCC1806 DESIGNS

5.2.1 Single pulse errors

The 1-clock pulse errors causing an unwanted 0-0 or 1-1 configuration of the push-pull driver stage cannot be avoided. The design has to guarantee that:

(1) A 1-pulse dropout (i.e. 0-0 configuration) or doubled (i.e. 1-1 configuration) shall not cause critical output voltage-drop transients or over-voltage transients in the DC/DC converter. Critical levels are for example power-reset level for computers, or over-voltage latch thresholds.

(2) A 1-pulse SEU malfunction must never cause a transformer flux imbalance such that the DC/DC converter transformer goes into saturation. A worst-case design of the transformer core area must always guarantee this margin and safe operation of the DC/DC converter.

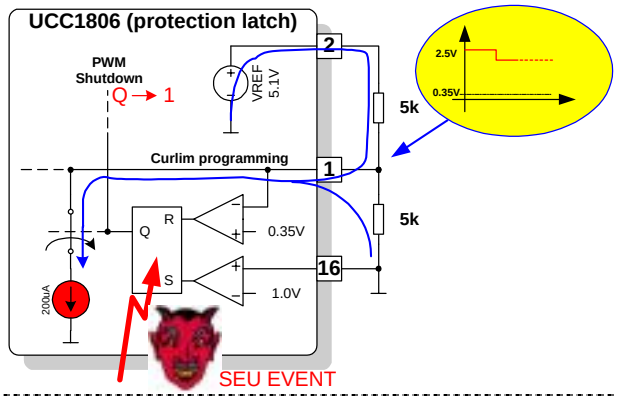
5.2.2 Protection latch errors stopping the PWM clock

The UCC1806 protection RS-latches will be activated by SEU. However, the consequences of the SEU can be controlled depending on PIN1 is biasing. The following recommendations is an outcome from our testing:

(4) Resistor values on PIN1 must always be big enough to force PIN1 < 0.35V for the RS-latch SEU.

Here is an example where the low resistor values (**5k**) results in a PIN1 voltage ≈ 2.0V after the SEU. The RS-Latch will never be restored until you power-cycle the VC and VCC power pins of the UCC1806.

For a data-handling system DC/DC with essential functions, the power cycling is not possible since the converter is fed by an uninterruptible primary power. Any “latching configuration” as this is forbidden.



(5) If a long delay is wanted for autonomous re-start events (i.e. several ms), the PIN1 biasing should be a RC-link similar to the contractor X design shown the report. Take note however, that **discharging of DC/DC output voltages achieving a proper power cycling of FPGAs etc. may require a considerably long delay period!**

(6) If a re-start delay is not wanted, filter capacitance shouldn’t at all be attached on the PIN1 - or be very small.

5.2.3 Control loop induced anomalies

The SEE that seem to be control-loop related were only observed for voltages on PIN4 > 500mV.

(7) **Until further SEU tests campaigns have been done on the UCC1806**, a recommendation must be that the differential voltage between PIN4 and PIN3 should be biased $\mathbf{V_{PIN4} - V_{PIN3} < 500mV}$.

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6 ABBREVIATIONS

Abbreviation	Description
CERDIP	CERamic Dual-In-Line Package
DIL	Dual-In-Line
ESA	European Space Agency
HF	Hard Failure
HIF	Heavy ion Irradiation Facility
LET	Linear Energy Transfer
PWM	Pulse Width Controller
QED	Quod Erat Demonstrandum
S/N	Serial Number
SEE	Single Event Effect
SEL	Single Event Latch-up
SEU	Single Event Upset
SF	Soft Failure

7 REFERENCES

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Proc. NSREC 1996, Workshop Record, pp. 78-83.
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[2] SEE Verification Test of Various Designs Using UCC1801/1805/1806 for ROSETTA
R. Harboe Sørensen /H. Jensen
4th D/TOS-QCA Final Presentation Day
30 January 2001

[3] UCC1806/2806/3806 LOW POWER, DUAL-OUTPUT, CURRENT –MODE PWM CONTROLLER
Manufacturers datasheet, TEXAS INSTRUMENT
SLUS272C
Feb 2000, Revised June 2003