PROJECT
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TITLE
SEE Test on Actel RT54SX32-S FPGA using Frequency Count Test Method

EUROPEAN SPACE AGENCY
CONTRACT REPORT

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SUMMARY

This report presents the results from Heavy Ion test of Actel FPGA RT54SX-S manufactured by Matsushita (MEC) in a 0.25µm technology. The device has earlier been tested using a "Virtual golden chip" method [1]. In this report new SEE data is presented that have been taken with a new test method, using frequency counters.

In the earlier test campaign [1] no SEU in the R- register cells was observed under static conditions up to LET of 64.5 MeV·cm^2/mg. Irradiation with heavy ions under 5 MHz dynamic condition resulted in errors that had the same signature as if they were proper SEU. When lowering the FPGA operating frequency by a factor of 4 to 1.25 MHz no errors could be observed. The errors observed in 5 MHz dynamic mode are very likely due to transient effects which are clocked through to the output. The LET threshold for this effect is likely between 28 and 34 MeV·cm^2/mg.

With this new test method, using frequency counters, one of the two earlier tested samples have been tested with a test frequency up to 100 MHz. Irradiation with heavy ions under 100 MHz dynamic condition resulted in increased number of errors. This is well in line what we would expect for upset from transient events in the circuit that need to be clocked into registers to be detected.

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Changes between issues are marked with a left-bar.

Issue	Date	Paragraphs affected	Change information
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1. INTRODUCTION

This report presents the results from Heavy Ion test of Actel FPGA RT54SX-S manufactured by Matsushita (MEC) in a 0.25µm technology. The device has earlier been tested using a "Virtual golden chip" method [1]. A new test method has been developed using frequency counters. The benefit is the possibility to test with higher frequency. SEE data for test frequency up to 100 MHz is presented in this report. A summary of the results from the preceding tests and also some additional test results are also presented.

The Actel SX-s family has register cells (R-cell) that are SEU hardened through hardwired TMR. No SEU in the registers is expected. At static test conditions no SEU have been detected, but testing in dynamic condition a few errors have been recorded. We suspect that heavy ion induced transients on the inputs to the R-cell can be transferred into the register when it occur in conjunction with clocking of the register. This would mean that increased clock frequency also increase the probability for heavy ion induced transients (SET) to be recorded into a register. This is a phenomenon you may expect with shrinking technologies.

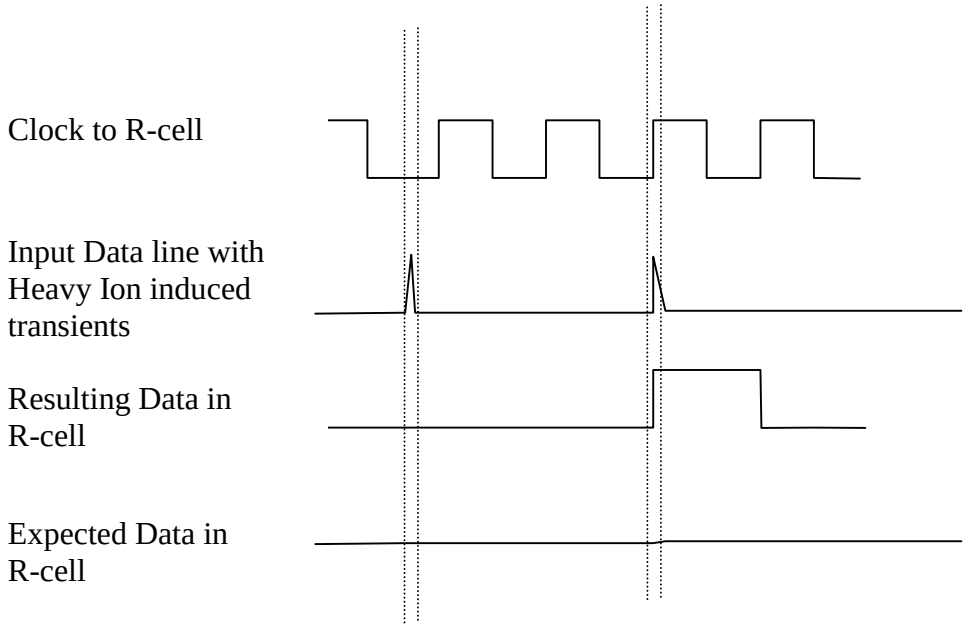

Figure 1.1 Principal for how a heavy ion induced transient on a data line may be recorded when the transient occur in conjunction with clocking of the register (R-cell).

1.1 SEE Results with "Virtual Golden Chip" Method

SEE results for RT54SX32-S have been reported [1] using static test conditions and dynamic up to a frequency up to 5 MHz. This test system uses a "Virtual Golden Chip" method to test for SEU. A summary of these test results and also some additional test results are presented here.

No SEU in the R- register cells was observed under static conditions up to LET of 64.5 MeV·cm^2/mg.
Irradiation with heavy ions under 5 MHz dynamic condition resulted in errors that had the same signature as if they were proper SEU. When lowering the FPGA operating frequency by a factor of 4 to 1.25 MHz no errors could be observed. The errors observed in 5 MHz dynamic mode are very likely due to transient effects which are clocked through to the output. The LET threshold for this effect is likely between 28 and 34 MeV·cm^2/mg.

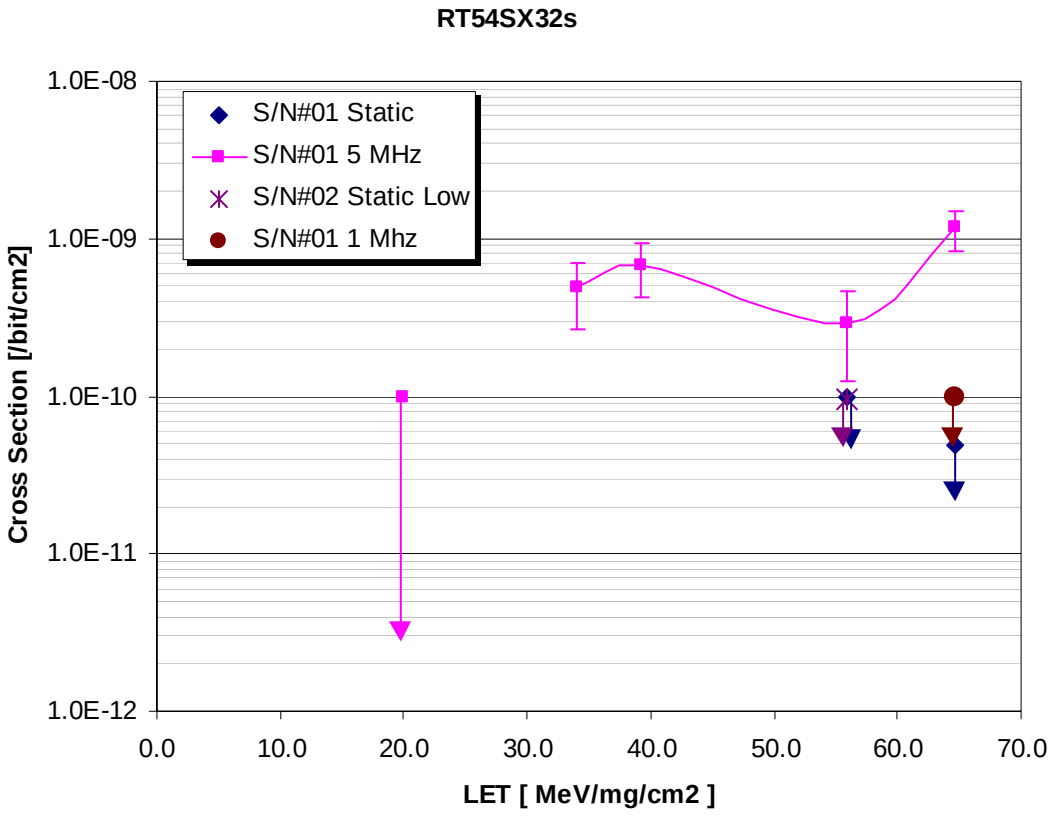

Figure 1.1.1 Upset cross section as a function of LET value for RT54SX32-S. Errors have only been detected in the 5 MHz dynamic test mode. The data points with arrows indicate fluence for test run without errors. The error bars are the standard deviation indicating counting statistics for each test run.

At the first test campaign that was performed [1] no SEE data were taken for ions between 19 and 34 MeV/mg/cm^2. At a later test campaign some more test runs were performed with the same test equipment as in the first campaign.

One device was tested in 5 MHz dynamic condition with 2.7 Volt to the array supply. The results are presented in Table 1.1.1. No errors were recorded.

Table 1.1.1 Summary of data for all performed test runs at RT54SX32S.

Test Run	Fluence	Mean Flux	Ion	Tilt	LET_{eff}	Number of Errors			Cross Section	Test Mode
#	Ions/cm^2	Ions/cm^2•s		degree	MeV•mg/cm^2	Sum	0-1*	1-0*	cm^2/bit	
42	1.0E+07	10000	Ar	0°	14.1	0	0	0	<9.8E-10	5 MHz Dynamic
43	1.0E+07	7000	Ar	45°	19.9	0	0	0	<9.8E-11	5 MHz Dynamic

44	1.0E+07	7000	Ar	60°	28.2	0	0	0	<9.8E-11	5 MHz Dynamic

*0-1 is number of errors when logic one was read but logic low was expected. 1-0 is the reverse case.

2. RT54SX-S DETAILS

The architecture of Actel's RT54SX-S devices is an enhanced version of Actel's SX-A device architecture. The RT54SX-S devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility. The RT54SX-S family incorporates up to four layers of metal interconnects.

To achieve good SEU requirements each register cell (R-Cell) in the RT54SX-S are build up with Triple Module Redundancy (TMR) (Figure 2.1)
The R-cells in SX-S consist of three master and three slave latches gated by opposite edges of the clock. The feedback path of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching.
With this solution the latches is continuously corrected and theoretically the only possibility for a SEU in a R- register is to have two latches hit by two ions within the recovery time of the transient created by the ions.

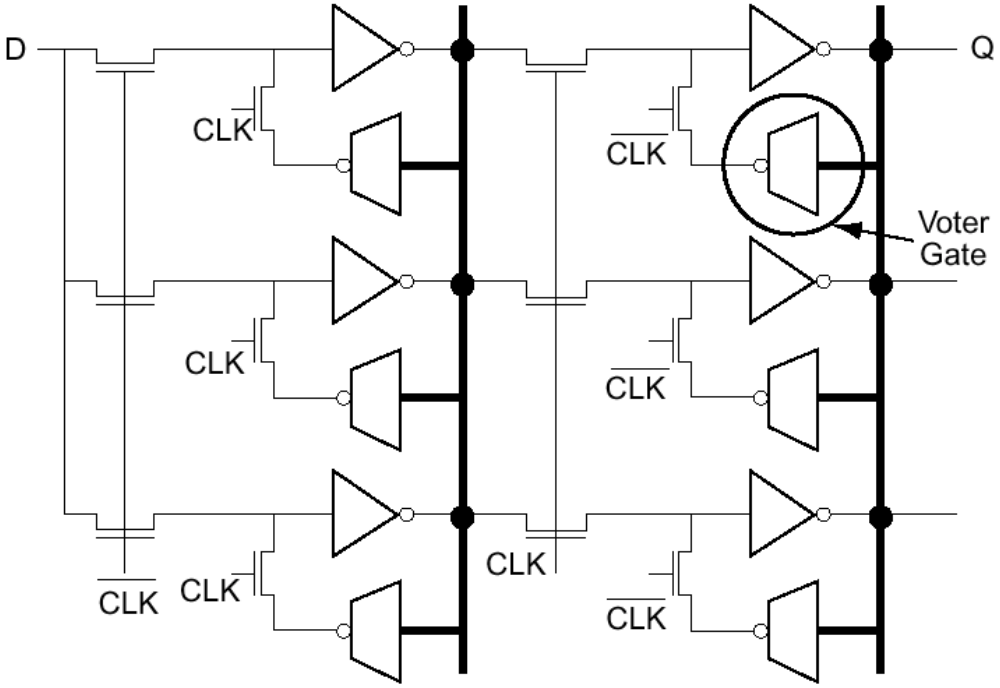

Figure 2.1 Schematic picture of R-Cell in RT54SX-S with tripled master and slave latches and voted feedback.

3. TEST SAMPLES

Two RT54SX32-S devices from the same wafer lot were used as test samples, both in 256 pin ceramic flat package. The devices were serialised as S/N 01 and S/N 02.

Delidded samples were used for SEE tests. The chip surface was covered with polymide coating measured to be about 10 µm thick. The coat was not removed before irradiation tests.

These are the same samples as used in the earlier test [1].

When mounting the test boards at UCL one of the samples (S/N 01) was destroyed due to over voltage stress.

ACTEL PART #	:	RT54SX32S-CQ256BPE60
WAFER LOT #	:	T25JSP03A
DATE CODE	:	0043

Marking / *Top side*	Marking / *Bottom Side*
ESD-logo QML	T25JSP03A
Actel Logo	004
RT54SX32S	USA
CQ256B 0043	

4. TEST TECHNIQUES

4.1 The "Frequency Count" Test Method

The principal of the SEE test is to clock toggling data into the DUT and measure the frequency out from the DUT with high-resolution frequency counters. The DUT is filled with long shift registers. The expected data out from the DUT is the same as was clocked in (just delayed by the length of the shift register). If an upset occurs in a register this will be detected as one less toggle at the output (Fig 4.1.1 & 4.1.2).

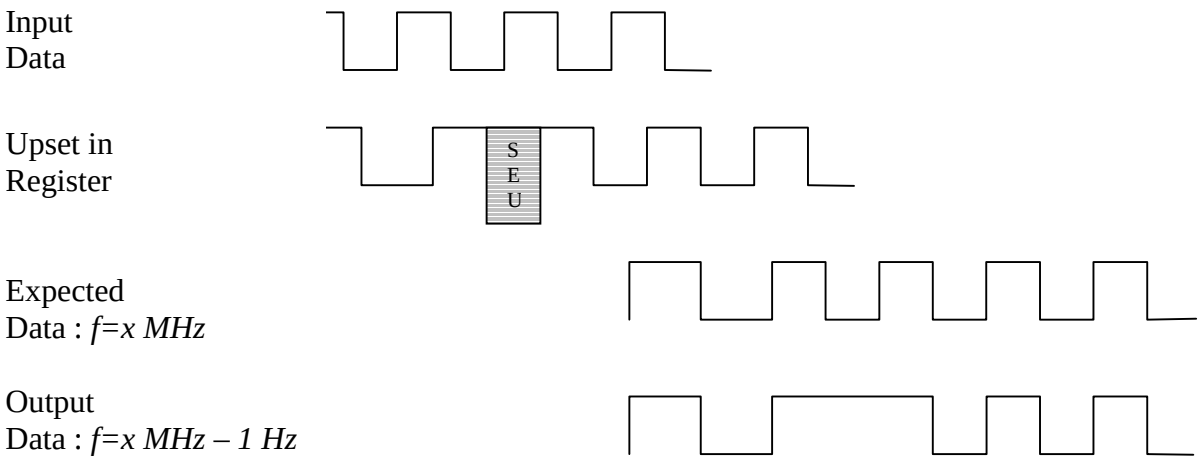

Figure 4.1.1 Principal drawing explaining how an upset will be detected with a high-resolution frequency counter.

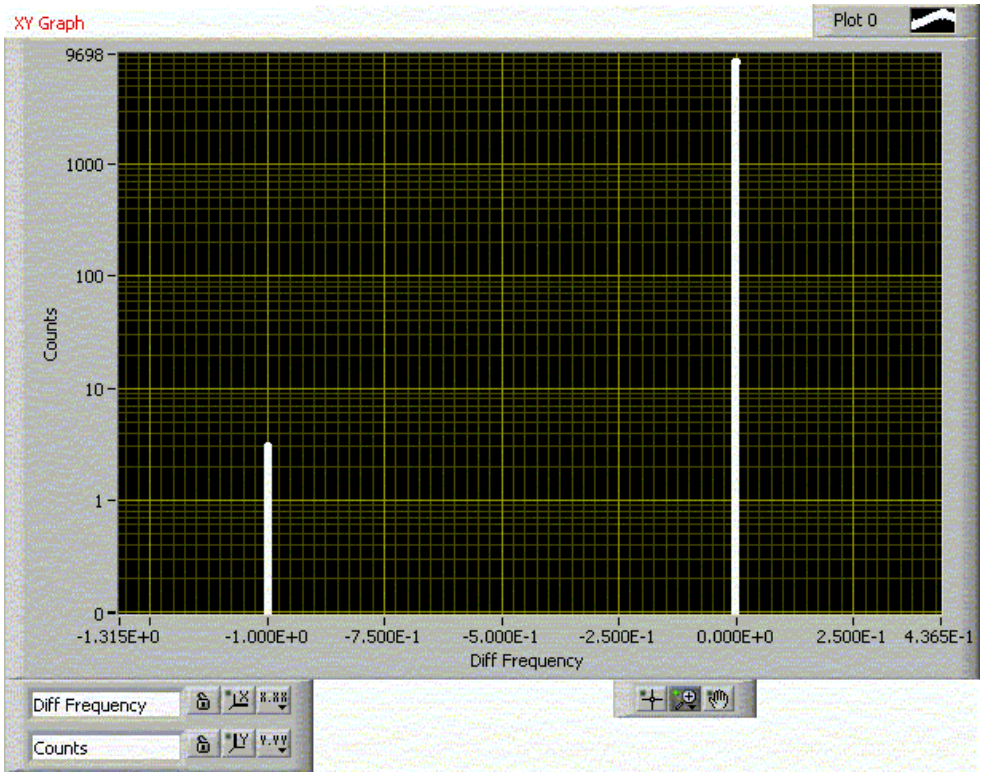

Figure 4.1.2 Histogram with near 10000 measured frequencies where 3 differ with one hertz from expected frequency. This is equivalent with 3 detected SEUs.

4.2 Test Boards

The test system consist of two boards, one Signal/Power board and one DUT board housing two Devices Under Test (DUT). The DUT board is the same that was used in the first SEE tests [1]. The Signal/Power board deliver power to the DUTs and the signals from outside of the test chamber to the DUTs. All outputs from the DUT are driven with LVDS out from the test chamber to frequency counters. The Data and Clock signals to the DUTs come directly from a data generator outside the test chamber through SMA cables.

Outside the test chamber four high-resolution frequency counters, connected to board housing LVDS receivers, recorded data from the DUT. All data from the counters are transferred to PC through the GPIB-interface. Fluke frequency counters were used, three PM6680B and one PM6681. All counters used an integration/sampling time of one second.

4.3 DUT Test Program Layout

The same DUTs and design have been used as in the earlier “Virtual golden chip” test [1]. The DUTs are programmed with eight parallel shift registers, each register consist of “128 bit” of TMR R-cells. This design use up 95% of available register cells in the FPGA.

With four frequency counters, only four of the eight shift registers could be tested in each test run. This means that 512 bits were tested in each test run.

The two devices were programmed at Actel/USA with the Saab Ericsson DUT design, using the “Sculpture programmer”. The used Actel programming S/W was at the time not a released and qualified S/W.

4.4 Test Conditions

All test runs were performed with:

V_{CCA} = 2.5 V
V_{CCI} = 3.3 V

The DUT was mounted in a test socket on the test board. To increase the thermal dissipation, a small copper block was attached on the bottom side of the DUT. Copper wires connected the copper block to the frame of test chamber.

During the tests, the measured case temperature of the DUT varied between 45 and 57°C.

5. SEE RESULTS

5.1 Test with ^{252}Cf

Tests with ^{252}Cf have been performed. Due to the fact that the this device type had a 10 µm coating layer on top of the four metal layers and the low penetration depth of the fission fragments from ^{252}Cf, no single event effects were expected and have not been detected.

5.2 Test with Heavy Ions

Single Event Effects tests have been performed at the Heavy Ion Facility in UCL, Belgium. The results are presented in Table 5.2.1.

Table 5.2.1 Summary of data for all performed test runs for RT54SX32-S

Test Run	Fluence	Ion	Tilt	LET_{eff}	Freq.	Tested R-cells	Number of Errors	SEU Cross Section
#	Ions/cm^2		degree	MeV·mg/cm^2	MHz		#	cm^2/bit
3	1.0E+06	Kr	45°	48.1	100	512	34	1.3E-8
6	1.0E+06	Kr	45°	48.1	75	512	10	3.9E-9
7	1.0E+06	Kr	45°	48.1	25	512	0	<3.9E-10
8	1.0E+06	Kr	45°	48.1	50	512	2	7.8E-10
9	1.0E+06	Kr	45°	48.1	90	512	5	2.0E-9
10	1.0E+06	Kr	45°	48.1	100	512	26	1.0E-8
11	1.0E+06	Kr	45°	48.1	80	512	5	2.0E-9
12	1.0E+06	Kr	45°	48.1	60	512	4	1.6E-9
13	1.0E+06	Kr	0°	34.1	100	512	22	8.6E-9
14	1.0E+06	Kr	0°	34.1	75	512	1	3.9E-10
15	1.0E+06	Kr	0°	34.1	50	512	2	7.8E-10
16	1.0E+06	Kr	0°	34.1	90	512	6	2.3E-9
17	1.0E+06	Kr	0°	34.1	80	512	3	1.2E-9
19	1.0E+07	Kr	0°	34.1	5	512	0	<2.0E-10
20	4.2E+06	Kr	0°	34.1	10	512	0	<4.6E-10

Figure 5.2.1 and 5.2.2 present the recorded cross sections dependence on test frequency, using linear and logarithmic scaling for the cross section.

The result indicates that the recorded cross section increases with increasing test frequency and with increasing LET value.

Some divergences from these relations exist for some test runs. This is probably an artefact due to poor statistics.

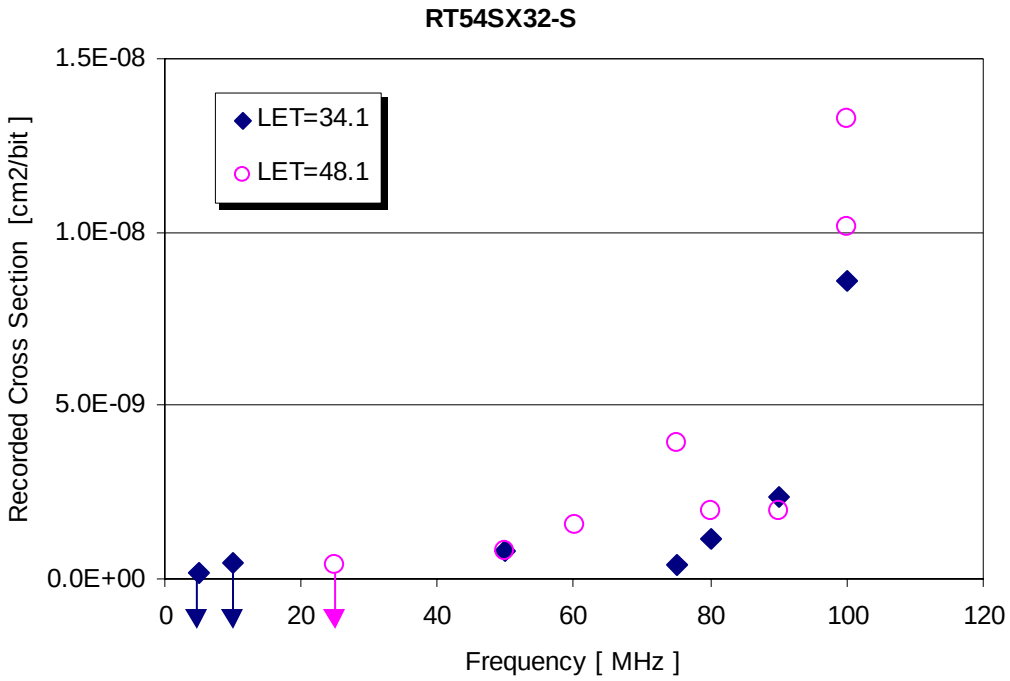

Figure 5.2.1 Recorded upset cross sections for RT54SX32-S with 0° and 45° tilted krypton beam. The Arrows indicate tests with no recorded upsets.

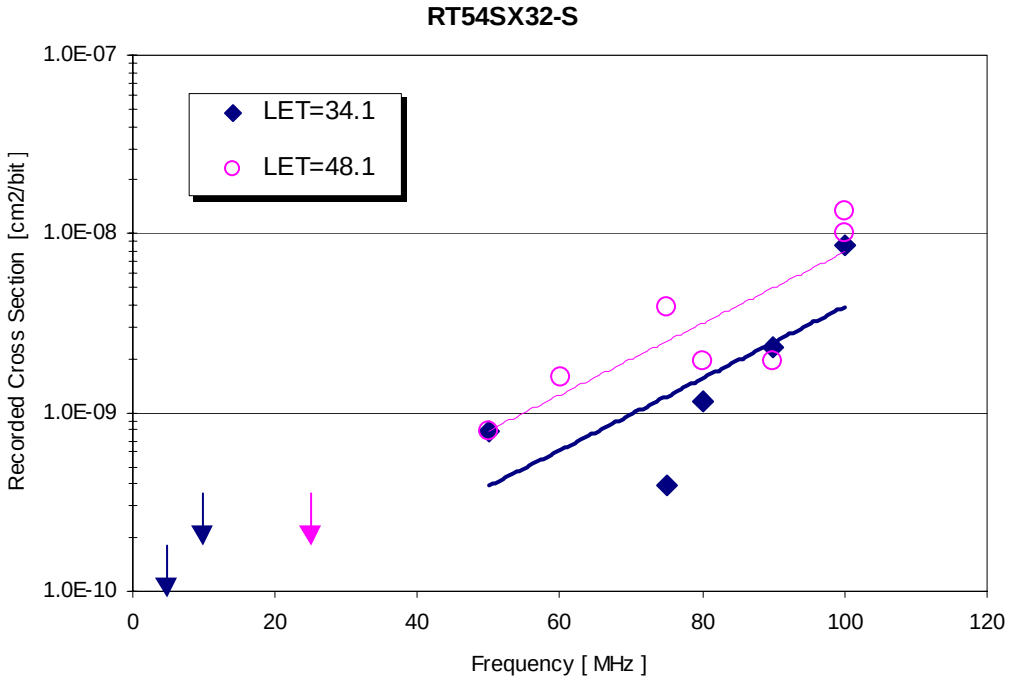

Figure 5.2.2 Recorded test data on logarithmic scale. The lines are exponential regression lines for each LET value. The Arrows indicate tests with no recorded upsets.

6. DISCUSSION

6.1 Linear frequency dependence

With the assumption that the time during a clock period where the register is sensitive for transient effects is constant between all test runs, we would expect a linear dependence between recorded upsets and test frequency. With twice the frequency, twice as many upsets would be recorded.

The result indicates that the recorded cross section rather increase exponential with the test frequency. This result is not in line with the theorem. The reason could be poor statistics or that the sensitive time window may change between the test runs. The chip temperature, that is hard to control in vacuum, may also be a parameter that affects the sensitive time window.

6.2 Comparison with “Virtual Golden Chip” test

Comparison between the results in figure 1.1.1 and 5.1.1 for LET = 34 MeV·cm^2/mg indicates that the frequency count test method records a lower cross section. The tests were performed on the same DUT, but the “Virtual Golden Chip” test did not have any copper mounted on the DUT to increase the thermal dissipation. This means that the relation between chip temperature and frequency differ between the two tests.

6.3 Origin of recorded upsets

In the introduction we suggest that the transients occur on the data line into the register and are clocked into the register. We have no proof that this is the case.
The assumption is that the transient is very short in time (< 0,5 ns) and that when it occurs in conjunction with a transition of the clock signal, the register cell may read an erroneous value. If this transient occurs on the data line, local clock driver or somewhere else is impossible to say.

The time for fully discharge all charge produced from an ion hitting the device is much longer compared to the transient itself. Maybe the register is inhibited to update its content during this period.

This report gives no answers on the origin of the upsets. It has been shown that upsets may occur and that the upset rate increases with increased test frequency.

7. CONCLUSION

At high LET values and when testing RT54SX32-S with high frequencies increased number of upsets has been recorded. At static test conditions no upsets was recorded [1]. This indicates that heavy ion induced transients may be clocked into the registers in the SX-S devices. The SEU hardened registers can't overcome this phenomenon.

The design that has been tested in these tests was developed to test the SEU hardness of the register cells. With the new test method we have been able to test for transient effects inside the chip, but the design was not developed with this purpose. E.g. no combinatorial logic has been included in the design.
The tested design only uses one of the three available global clocks. The other global clocks and also non-global clock nets could show a different result.
By using other kinds of test patterns in the heavy ion tests more knowledge of the transient effects may be achieved.

The recorded error rates for RT54SX32-S are very low, but with shrinking technologies in the future you may expect lower LET thresholds for SET induced errors. This will remarkably increase the error rates in space applications and SET induced errors will be an issue for FPGAs and ASICs.

8. REFERENCES

[1] ESA_QCA0110S_C, "Radiation Pre-Evaluation of Actel FPGA RT54SX32-S", Saab Ericsson Space (D-P-REP-1086-SE), 27 Sept 2001.