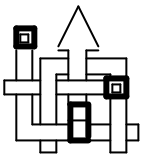

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Work Order 14924/00/NL/ND

Radiation Effects Study of Components Operated at Cryogenic Temperatures and Future Generations Semiconductor Devices

Final Report

Deliverable D6

C. Claeys , A. Mercha and E. Simoen

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Abstract

This report constitutes Deliverable D6 of Work Order 114924/00/NL/NB on "Radiation Effects Study of Components Operated at Cryogenic Temperatures and Future Generations Semiconductor Devices". It is the Final Report and summarizes the main results that have been obtained during the execution of the Work Order. The report contains two parts, one related to Activity I on Cryogenic Radiation Effects, and one dealing with Activity II on Radiation Effects in Advanced Semiconductor Materials and Devices. In case that the results have already been described in detail in one of the Deliverables, only the main results and conclusions are given. Important conclusions are i) the feasibility of cryogenic gamma and proton irradiations at liquid helium temperatures has been successfully demonstrated, ii) the circuits envisaged to be used for HERSCHEL are sufficiently radiation hard but may suffer from statistical spread iii) for total dose testing it is important to be able to perform irradiations at cryogenic temperatures, iv) the IMEC 0.13 µm CMOS technology is radiation hard to at least 100 krad(Si), v) for scaled down technologies it is important to get a good physical insight into the length dependence of the performance degradation after irradiation, v) it is for future technologies essential to study more in detail effects such as radiation-induced leakage current (RILC) and the linear kink effect (LKE). The report concludes by giving an outlook for future activities in this field.

INTRODUCTION

This report constitutes Deliverable D6, associated with Work Order 14924/00/NL/ND on "Radiation Effects Study of Components Operated at Cryogenic Temperatures and Future Generation Semiconductor Devices". It should also be considered as the Final Report of this Work Order, which consisted of two Activities: Activity 1 related to Cryogenic Radiation Effects, and Activity 2 dealing with Radiation Effects in Advanced Semiconductor Materials and Devices. Each Activity was scheduled to run for 24 months. The project started on February 15, 2001 and ended on February 14, 2003. Compared to the original time schedule outlined in the proposal, there was no delay in the completion of all the activities.

For each of the two Activities, the main results and conclusions are only briefly discussed as reference is made to the different Deliverables. These Deliverables report extensively on all the different experiments and the obtained results. Activity 1 is related to the experimental study of low-temperature radiation effects in cryogenic electronics, i.e., electronic devices to be operated at liquid helium temperatures and intended for space missions such as e.g. the HERSCHEL mission to be launched in 2007. The goals were to investigate where in Europe cryogenic irradiations could be performed, to set up an experimental cryogenic irradiation facility, and to validate it by testing HERSCHEL components and basic test structures, both processed in the AMIS 0.7 µm technology. The output is a Cryogenic Irradiation Manual for both gamma and proton irradiations at liquid helium temperature, outlining the procedures to follow, taking into account practical aspects and safety issues.

For the second Activity on Radiation Effects in Advanced Materials and Devices, the focus was on the evaluation of the IMEC's high performance CMOS technologies, including both bulk and SOI 0.13 µm technologies. Both gamma and proton irradiation rounds have been performed. Beside a general study of the radiation performance of the technology, dedicated process modules such as the isolation technology and the nitridation of the gate oxide were investigated in more detail, as these processes will gain in importance for

future scaled down technologies. This part of the report is more extended than the first part, as some interesting observations related to some peculiar phenomena have been noted. In-depth discussions of the physical aspects involved can be found in the different Deliverables as will be indicated.

The Final Report includes a general conclusion and an outlook for possible future activities. For completeness a list of all the generated documents and the resulting publications and conference contributions is given in the Appendix.

ACTIVITY I: CRYOGENIC RADIATION EFFECTS

The Activities were related to the experimental study of cryogenic gamma- and proton irradiations and contained three main Work Packages:

- Cryogenic Irradiation facility Assessment/Installation
- Cryogenic Irradiation Testing
- Update Cryogenic Irradiation Manual

The tasks performed and the results obtained during the execution of the work are briefly summarized. Reference will be made to the different Deliverables for more detailed information.

I.1 Cryogenic Irradiation Facility Assessment/Installation

The aim of this work package was first to investigate where in Europe it would be possible to perform cryogenic irradiations, i.e., at temperatures in the liquid helium range, and to gain information on the different practical and safety aspects that have to be taken into account when setting up a cryogenic irradiation facility. In addition, an irradiation test plan had to be generated for the experimental study of both components envisaged to be used for the HERSCHEL mission and basic test structures fabricated in the AMIS 0.7µm CMOS technology.

As outlined in Deliverable D1 (P35288-IM-RP-0001) there are not many places in Europe where it is possible to perform cryogenic irradiations. Especially when the option is required to bias the devices during irradiation and to be able to monitor in-situ the electrical device performance. For proton irradiations, PSI in Zurich is an option. Because of the practical problems and the fact that for experimental research a lot of unexpected difficulties may be encountered, it was decided to investigate the possibility to set up an experimental cryogenic irradiation facility relatively close by. As discussed in the report, it was decided to perform the gamma irradiations at ESTEC and the proton irradiations at Louvan-La-Neuve (LLN). The most time consuming

issue before being able to start the experimental work was the fact that a dedicated flow cryostat had to be ordered.

I.2 Cryogenic Irradiation Testing

In June 2002 the first cryogenic gamma irradiations were successfully executed at the ESTEC site. The used test plan is described in a Technical Note (P35288-IM-TN-0002). The outcomes of the experimental validation of the cryogenic irradiation facility are (full details in Deliverable D1):

- For safety reasons, it is absolutely necessary that besides the operators of the radiation facility at least two and better three experimenters are available during the tests. Some manipulations can just not be done single-handedly. Next, given the complexity of the experiments, they need to be well prepared. The performed γ-irradiations have helped to establish some rules of conduct and an operation manual and has pointed out some weak points which require further improvements.
- Special attention has to given to the mounting, interconnection and testing procedures.

The cryogenic proton irradiations were successfully performed in August 2002 and in October 2002 in Louvain-La-Neuve. The used irradiation plan is described in a technical Note (P35288-IM-TN-0004). It should be mentioned that it is important to pay special attention to the screening of the sensitive parts of the electronics (PXI,…) from the back-ground irradiation, present in the room. Some soft-ware errors occurred during one of the exposures.

The cryogenic irradiations of the HERSCHEL devices and the relevant test structures, processed by AMIS in a 0.7 µm CMOS technology, are in detail described in Deliverable D2 (P35288-IM-RP-0003). The most important conclusions of the cryogenic irradiations of the test devices, performed at a gamma dose rate of 5 krad/hour, are:

1) The tested n- and p-MOSFETs are quite radiation hard at least until an equivalent total dose of 15 krad for gamma and proton exposures at liquid helium temperature. The most sensitive part to radiation-induced ionisation effects is the gate. The hole trapping in the oxide and the generation of interface states will impact the threshold voltage, while the latter has also a strong influence on the transconductance of the devices. However, in the liquid temperature range both hole trapping and interface states generation are nearly completely eliminated so that no significant shift in threshold voltage and/or transconductance has been observed. Typical curves are shown in Fig. 1 for a p-MOSFET.

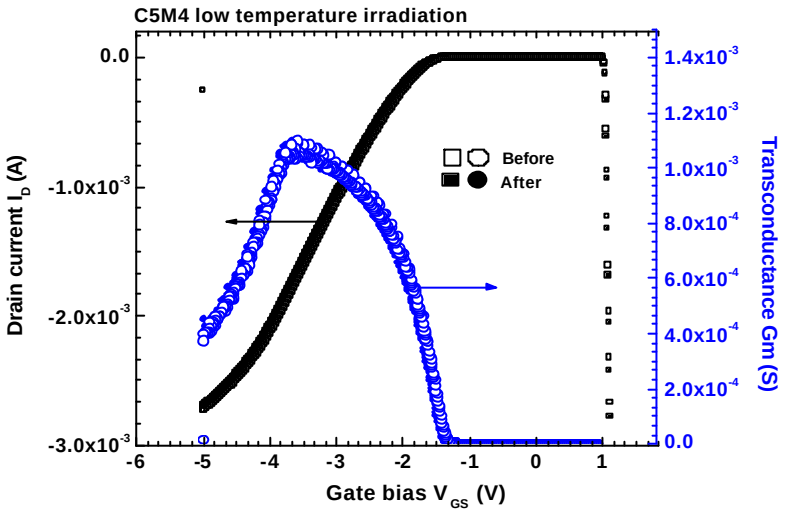


Figure 1: Drain current and transconductance versus gate voltage V_{GS} from 0 V to –5 V with -10 mV steps for a drain bias of -2.5 V at 7 K.

2) Small variations (< 90 mV) have been observed in the threshold voltage for low temperature gamma irradiation. This is illustrated in Fig. 2 by the higher drain current after irradiation for the n-MOSFET.

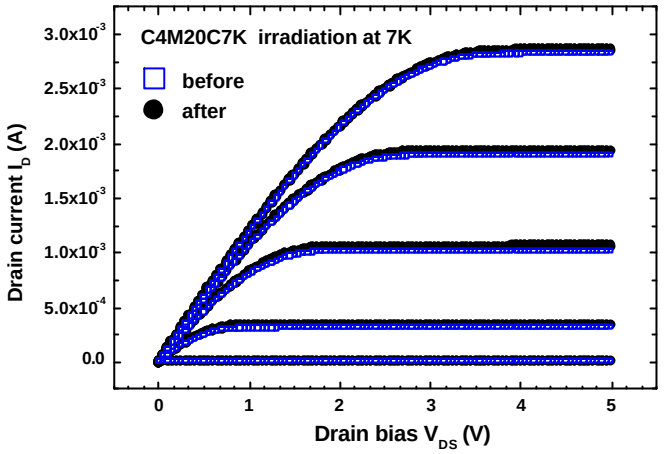


Figure 2: Drain current versus drain voltage V_{DS} from 0 V to +5 V with 10 mV steps for different gate biases from 1 to 5 V with 1 V steps at 7 K.

3) The subthreshold hump measured in the subthreshold regime, seen before irradiation, is for both n and p-MOSFETs at low temperature suppressed after gamma irradiation.

4) The ESD protection diode is not operational at low temperature and definitely useless after irradiation.

The 0.7 µm AMIS CMOS technology is probably suitable for low temperature applications but some points need to be improved or refined for a better reliability. Therefore the activity should continue and investigate the subthreshold currents variations and define a more reliable ESD protection device for low temperature application in a harsh environment.

The PACS CRE electronics and several of its building blocs have been tested before and after low temperature irradiations. The investigations of the readout circuitry performance after low temperature irradiations pointed out that:

1) Low temperature ^{60}Co gamma irradiations showed small radiation induced variations, which could be explained by the V_T shifts observed in

component radiation tests. The PACS CRE Circuit kept on working within the specifications of the PACS.

- The test results on the proton irradiation tests in LLN are inconsistent. Initial tests with proton radiation of the PACS CRE showed on top of temporary radiation effects, a failure of the digital logic on the circuit from 10kRad on. In a second more thorough test round these results could not be repeated. The same temporary effects were observed, but they disappeared after the radiation was disabled; only a small shift in the characteristics remained. Neither of the tested devices showed any malfunction at a total dose of 15 krad(Si), even at double dose most circuits were undamaged. The reason for this contradictory is not clear as both times the flux and energy was the same as well as the biasing conditions. However, an in-depth study of these devices was not within the scope of this Work Order.

In general, it can be stated that the cryogenic gamma and proton irradiations have successfully been performed, which was the final goal of this Work Order. These facilities (ESTEC for ^{60}Co and LLN for protons) can in the future be used for radiation hardness testing of cryogenic devices and circuits.

I.3 Update Cryogenic Irradiation Manual

An important output of Activity 1 is the generation of a Cryogenic Irradiation Manual. At the end of the previous Work Order some general guidelines were defined, but no experimental results were available. The main goal of this Work Order was to define a working procedure for cryogenic gamma- and proton irradiations, based on practical aspects and safety issues. Detailed information on the Cryogenic Irradiation Manual is given in Deliverable D3 (P35288-IM-RP-0005). To illustrate the achievements of this important milestone, some pictures of the gamma- and the proton cryogenic irradiation facilities at ESTEC and LLN, respectively, are given in Fig. 3-6. They are showing the used JANIS flow cryostat, the set-up at the gamma

source, a picture of a mounted sample, and the cryostat at 4.2 K before the start of a 60 MeV proton irradiation.

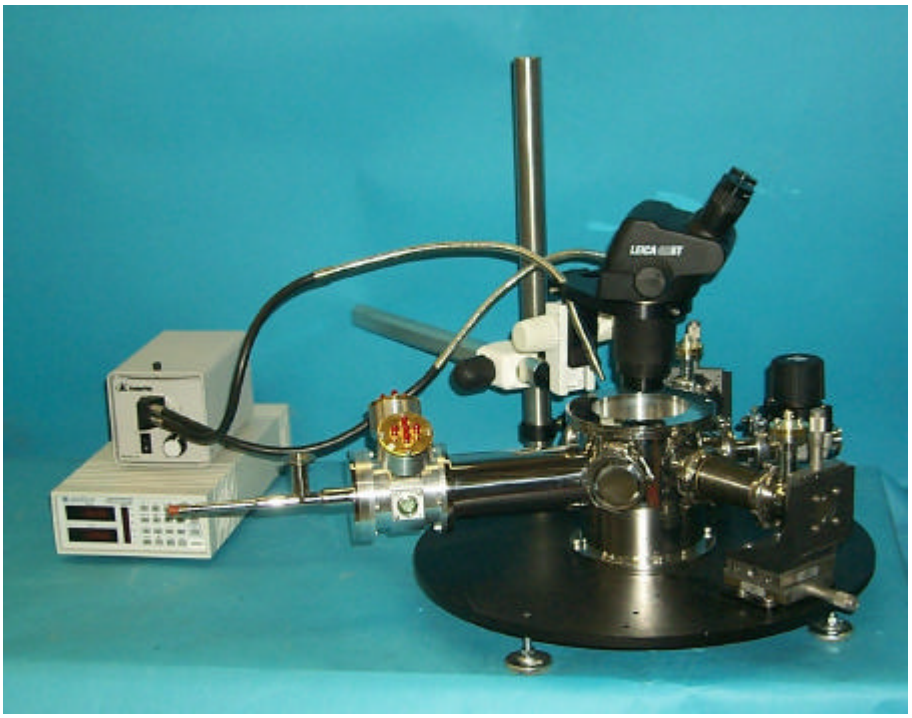


Figure 3: Picture of the Janis cryostat that is used for the cryogenic irradiation.

Figure 4: Picture of the set-up at the γ-source.

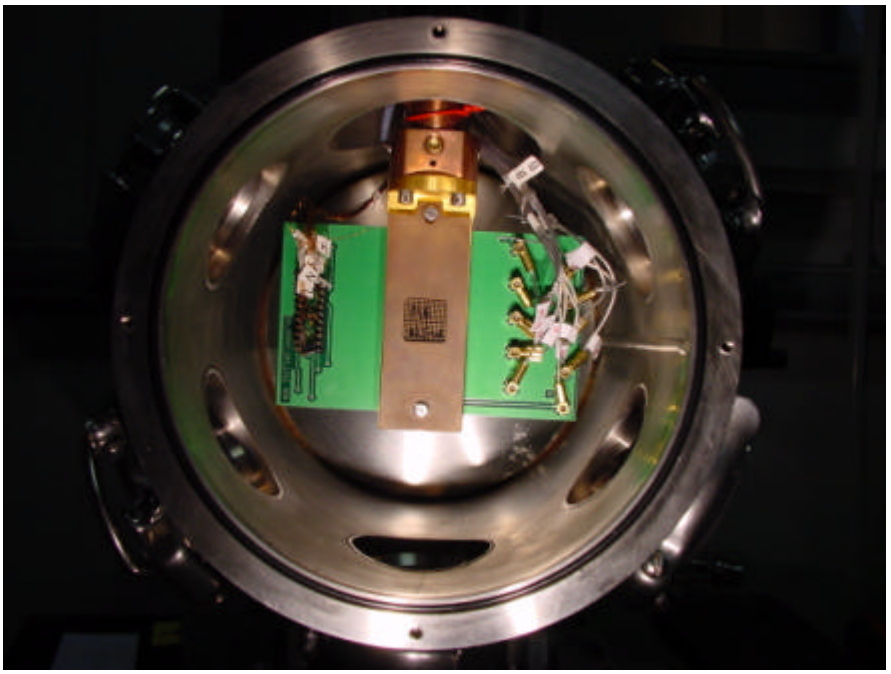


Figure 5: Picture of a mounted sample.

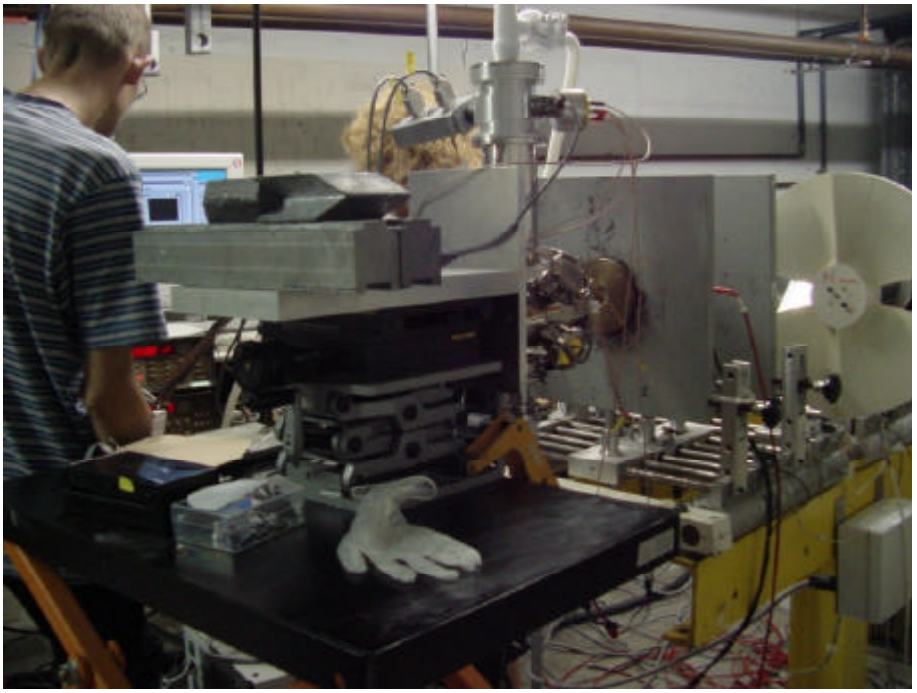


Figure 6: Cryostat at 4.2 K before the start of a 60 MeV proton irradiation.

The following general guidelines for the cryogenic radiation testing can be given:

- Cryogenic radiation testing is needed, as there is a difference in the radiation response between room temperature and 4.2 K irradiations. This was already stated after the literature study and room temperature tests performed in the previous Work Order and is confirmed by the present results. It was for example found that out of the 3 PACS circuits tested at 4.2 K two failed to work after a 60 MeV proton fluence of ~$7x10^{10}$ p/cm^2. The failure threshold was significantly higher at room temperature (about twice as high), although the statistics of the experiments is of course rather poor. There is also as yet no clear explanation available on the failure mechanism and on the different behaviour observed during different proton testing rounds. On the other hand, no failure was found after cryogenic γ-irradiations of circuits and test structures (transistors). This leads to the two following guidelines.

- It is clear that the circuit behaviour under proton or γ-exposure is different. This holds both for room temperature and cryogenic irradiations. In other words, γ-irradiations cannot replace proton testing for the PACS circuits studied and, therefore, a limited proton testing is required. This is even more valid for cryogenic operation, where no valuable conclusions can be drawn from γ-irradiations alone. Another factor seems to be the widely different behaviour of nominally identical circuits coming from the same wafer. This leads to the conclusion that for a meaningful proton testing at 4.2 K, a sufficiently large set of samples should be considered. Two factors which can contribute to the statistical variation are, on the one hand, the operation conditions (biasing) of the circuits at 4.2 K and, secondly, the statistics of the proton irradiation itself, where extreme damage events can occur in certain parts of the chip.

- One possible explanation for the different behaviour observed during our proton and γ-ray irradiations could be the dose rate, which was about 10 times higher for the case of the 60 MeV protons. It has been reported that there is a favourable effect of low dose rates at cryogenic temperatures, i.e., 90 K, which could explain the better performance after the γ-exposures.

- It is not straightforward to extrapolate single device behaviour to predict circuit response. On the other hand, the parameter shifts observed on a transistor level are useful to explain moderate changes in circuit response. For diagnostics of device failure, it is recommended to study the building blocks of the circuit (analog, digital part, amplifier,…) under realistic operation conditions. At the same time, it seems necessary to investigate the hardness of the field oxide (parasitic transistors) at 4.2 K, as the degradation of that oxide is suspected to be the origin of part of the circuit problems. It should also be noted that the device studies indicated a possible failure of the ESD protection of the transistors and by extension of the circuits. This could be an additional source of device failure/malfunctioning.

- From a practical viewpoint, it has become clear that the most delicate part is the device mounting and exchange. Most time was lost during this part of the experiment. Sometimes, the signal was lost during an irradiation, due to the wiring (no contact, shorts,…). This is particularly of concern during the proton testing, which is expensive. In order to make efficient use of the beam time (which continues during mounting, testing and cooling phase), one should prepare the experiments very carefully. It is recommended to perform a dry run of the experiments beforehand, using the same circuits and testing conditions, cooling included.

I.4 Conclusion

Activity I has resulted into a practical set-up for both gamma and proton cryogenic irradiations and the facilities have successfully been tested. A Cryogenic Irradiation Manual has been generated, taking into account several practical aspects and safety issues. There are only a limited number of facilities in the world allowing to perform irradiations at liquid helium under standard operating conditions and offering in-situ monitoring of the circuit performance.

ACTIVITY II: RADIATION EFECTS IN ADVANCED SEMICONDUCTOR MATERIAL AND DEVICES

This Activity has the emphasis on the radiation hardness assessment of some of the deep submicron CMOS technologies available at IMEC. It is important to remark that these technologies are standard technologies, which were not at all optimised from a radiation hardness viewpoint. Therefore this exercise should be considered as typical in the case that a COTS approach is used for space applications. For this Activity 24 months were foreseen, allowing the execution of two irradiation rounds. The first round contained both each gamma's and protons, while only protons were used for the second round. The Activity contained two main Work Packages:

- Radiation Studies of High Performance Deep Submicron CMOS
- Summary and Guidelines

The experimental results obtained during the execution of the Work Packages are briefly summarized. Reference will be made to the different Deliverables for more information.

II.1 Radiation Studies of High Performance Deep Submicron CMOS

One of the roadblocks on the way to scaling a CMOS technology is the gate leakage current that drastically increases as the gate oxide thickness reaches the tunneling limit. To go beyond this physical limit, nitrided (NO) or reoxidised nitrided oxides (RNO) are being used to increase the dielectric constant, allowing a thicker layer to exhibit the same capacitance as a thinner oxide and also to reduce the gate leakage current. Using NO or RNO annealed oxides brings certain advantages with respect to gate oxide reliability and boron penetration. It has also been reported that a higher radiation tolerance can be achieved under certain processing conditions, although this has not been verified thoroughly for thin gate oxides (2 nm).

On the other hand, the presence of N atoms close to the interface has some substantial drawbacks: it introduces fixed oxide charges, which can reduce the mobility and transconductance at low to intermediate gate voltage V_G. Furthermore, beyond 0.25 µm feature sizes the CMOS technologies use Shallow Trench Isolation (STI) instead of LOCal Oxidation of Silicon isolation (LOCOS). STI can lead to appreciable device degradation due to a parasitic sidewall MOSFET leakage path.

In this Activity, in line with the Commercial-Off-The-Shelf (COTS) philosophy, it was decided to focus on the radiation damage in the 0.13 µm CMOS technology, which was IMEC 's workhorse technology during the last two years. Also microelectronics industry has been moving towards this level of scaling. We investigate the impact of 60 MeV proton and gamma irradiations on the behavior of NO and RNO MOSFETs fabricated in IMEC's 0.13 µm CMOS technology with STI based isolation. Device parameters such as the threshold voltage V_T, the transconductance g_m and the series resistance R_s have been studied as a function of the device length and width.

The radiation testing has been done employing two different irradiation rounds, with in the first round both gamma's and 60 MeV protons and in the second one only protons. An overview of the irradiation testing performed during the two rounds is summarised in Table I. Beside irradiations at Louvain-La-Neuve, limited irradiation testing has also been performed at Demokritos in Athens, Greece. The results obtained after the execution of the first gamma and protons irradiation round are described in detail in deliverable D4 (P35288-IM-RP-0001), while the second irradiation round is in-depth discussed in Deliverable D5 (P35288-IM-RP-0004). Here only the most important results and conclusions will be summarized.

II.1.1 Results Obtained from the First Round of Radiation Testing

This section of the report gives a brief overview of the results and conclusions coming from the first gamma and proton irradiation round. It should be considered as a type of summary of the extensive information reported in deliverable D4 (P35288-IM-RP-0001).

Table I: Overview of the different irradiation experiments for Activity 2.

Date	Location	Particle	Dose/fluence
First Irradiation Testing Round			
27/06/01	LLN	60 MeV protons	10^{11} & $5x\ 10^{11}$ cm^{-2}
26/09/01	LLN	^{60}Co	13.5 & 100 krad(Si)
	Demokritos	7.5 MeV protons	$2.7x10^{12}$ & $2.7x\ 10^{13}$ cm^{-2}
Second Irradiation Testing Round			
21-22/08/02	LLN	60 MeV protons	$5x10^{10}$ & $5x10^{11}$ cm^{-2}
01/10/02	LLN	65 MeV protons	10^{11} cm^{-2}

II.1.1.1 Technological and Irradiation Details

The relevant technological details of the devices, fabricated in a 0.13 μm CMOS technology using an STI isolation scheme, 2 nm gate oxide, 150 nm polysilicon gate and 80 nm nitride spacers, used for the first irradiation round are summarized in Table II.

Table II: relevant technological details for wafer 7 (W7 NO) and wafer 9 (W9 RNO)

	Wafer 9 RNO and Wafer 7 NO
Gate oxide thickness	NO or RNO 2nm
Gate oxidation	Wet 850°C
Isolation	STI
P-well implantation	200 keV & 35 keV
N-well implantation	380 keV & 160 keV
N-LDD	5 keV
N-HDD	50keV
N-Halo	65 keV
P-LDD	6 keV
P-HDD	6keV
P-Halo	120 keV
Nitride spacer	80nm
Silicidation	Ti/Co (8/12 nm)

Both 2nm NO annealed (W7 NO) and 2 nm reoxidised NO (W9 RNO) gate dielectrics have been studied. L-arrays serve to study the short channel effects, while W-arrays provide insight in the impact of the STI on the transistor performance. Both packaged and unpackaged pieces have been characterized.

Unbiased and biased (V_G=1.5V) 60 MeV proton irradiations were performed on 27 June 2001 at the Cyclone cyclotron facility (Louvain-la-Neuve) for two fluences typical for space applications, i.e., 10^{11} and 5.10^{11} cm^{-2}. For packaged transistors, the irradiation was performed through the lid of the package. The flux was 3.10^8 $p/cm^{-2}s$. On 26 September 2001 also gamma irradiations were performed at the Louvain-la- Neuve ^{60}Co source for a total dose of 100 krad(Si) and 13.5 krad(Si), respectively. In this case the dose rate is 5 krad(Si)/hr. These conditions have been chosen to be approximately equivalent to the total dose after 10^{11} and 5.10^{11} p/cm^{-2} of 60 MeV protons. In that way, from this set of experimental results, it should be possible to separate the role of ionization damage from displacement damage.

II.1.1.2 Pre-Irradiation Test Results

Pre-irradiation characterization has been performed for the mounted and non-mounted devices, both for p and n-MOSFETs, L-arrays and W-arrays, NO and RNO annealed gate oxides. This allowed studying the narrow and short channel effects and the impact of the STI isolation scheme. Typical for these devices is a reverse short channel effect (RSCE), whereby the threshold voltage is first increasing with decreasing length before starting to decrease as expected. This effect, illustrated in Fig. 7, is similar for NO and RNO gate oxides and can be explained by the non uniform lateral doping.

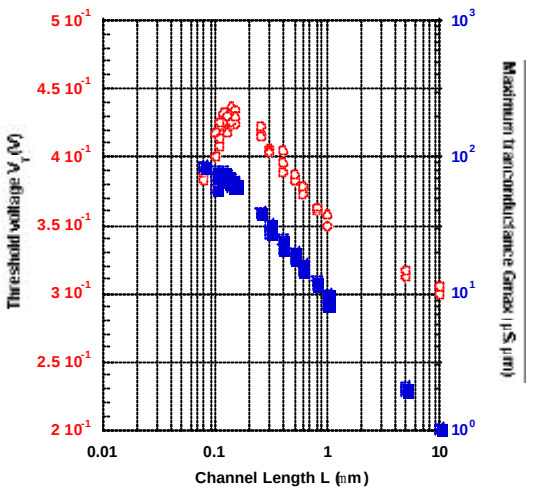
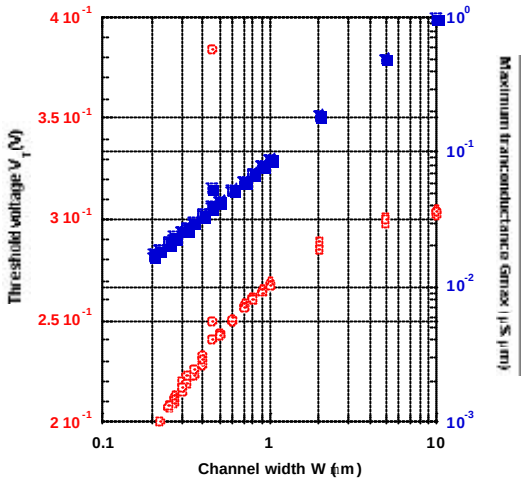
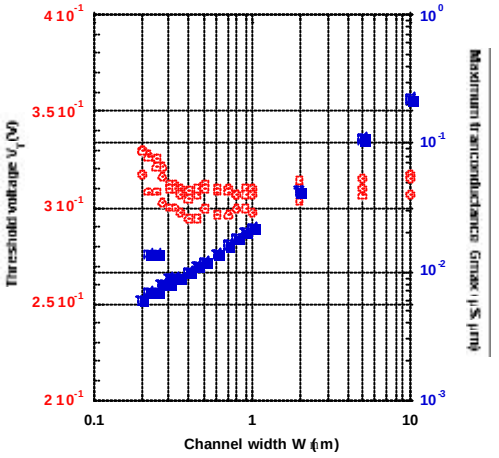


Figure 7: Threshold voltage (circles) and maximal transconductance (closed squares) versus the mask channel length for RNO n-MOSFETs samples 91, 92 and 93.

It is known that for narrow width devices the threshold voltage may decrease for decreasing channel widt due to the so-called Inverse Narrow Channel Effect (INCE). However, whereas for LOCOS isolation NCE (increase of V_T with decreasing channel width) is observed for n-channel devices, it is for p-channels in the case of STI. The V_T behavior and the maximum transconductance as a function of the channel width are illustrated in Fig. 8 for STI devices processed in the IMEC's 0.13 µm technology. For STI devices, the fringing field from the gate region beyond the channel edges helps to support the depletion charge in the channel making the depletion region deep, thus increasing the surface potential and help starting the inversion layer (lower V_T). For p-MOSFETs, a normal Narrow Channel Effect (NCE) may be explained by the same positive charges at the channel edges that contribute to an increase of V_T but can also be caused by boron segregation into the STI due to stress effects as the channel width decreases.



(a)



(b)

Figure 8: Threshold voltage (circles) and maximum transconductance (closed squares) versus the mask channel width for RNO n-MOSFETs (a) and p-MOSFETs (b) samples 91, 92 and 93.

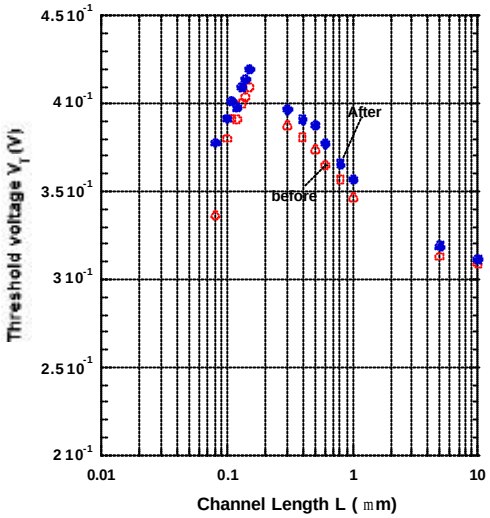
II.1.1.3 Post Proton-Irradiation Results

For devices, which have been proton irradiated under bias, the main variations are related to the short channel n-MOSFETs showing an increase of V_T and G_{max} which is most pronounced for RNO at a fluence of 5. 10^{11}p/cm^2. These changes are illustrated in Fig. 9. Comparing NO with RNO, it was observed that for low 60 MeV fluences (10^{11} p/cm^2), RNO is more resistant to degradation. The situation reverses after 5 10^{11} p/cm^2: for NO n-MOSFETs, the amount of change does not particularly increase with fluence Φ (or

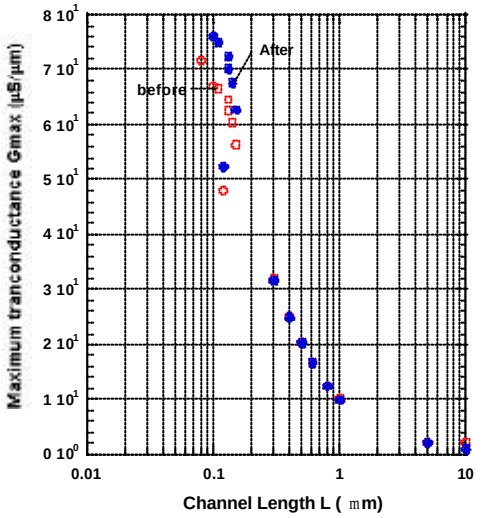
saturates already for low Φ); the only difference being that also the long channel devices are affected, showing the same trend. For RNO, a cross-over in the degradation of the parameters is seen, whereby the long transistors show opposite behaviour compared with the short ones. In addition, RNO n-MOSFETs exhibit a larger parameter shift, i.e., are more sensitive for higher proton fluences.

For unbiased irradiations, the degradation of the parameters is scattered and no consistent length-dependence has been observed. It seems that NO and RNO behave as mirror images at the two proton fluences studied. Comparing the scale of the variations, it happens to be larger for the NO n-MOSFETs in this case.The maximum change for unbiased devices is also larger than for the biased irradiations, which may come as a surprise. One important observation, however, is that the change in V_T and G_{max} is correlated, irrespective of device length, gate oxide or proton fluence. To some extent, the same has been observed before for the 0.18 μm n-MOSFETs, after unbiased 60 MeV proton irradiation. There, a different parameter shift could be obtained, which was a function of the device length – in general, more aggrevated for shorter lengths.

There was also not a clear proportionality with the proton fluence, but rather a rebound behaviour was found in some cases. A strong difference, however, is that for the 0.18 μm transistors, a clear degradation of the substhreshold characteristics was observed after irradiation. This could be related to the use of PELOX isolation compared with STI. Overall, the 0.13 μm technology is extremely hard from a viewpoint of ionisation damage in the gate and isolation dielectrics. A length-dependent degradation may result from a change in the lateral doping profile (HALO and LDD) in the channel region.



(a)



(b)

Figure 9: Threshold voltage (a) and maximum transconductance (b) versus channel length before and after a 60MeV proton irradiation.

The proton irradiations allow to make the following conclusions related to the observed behavior and the physical interpretation:

- Electrical parameter variations induced by irradiation are mainly related to RNO and NO n-MOSFETs L-arrays. In fact there is no clear variation for both W-arrays and p-MOSFETs. This remark implies first that the STI isolation scheme is radiation hard but also that charge eventually trapped in the nitride spacers may not be responsible for the observed variations in the transconductance and

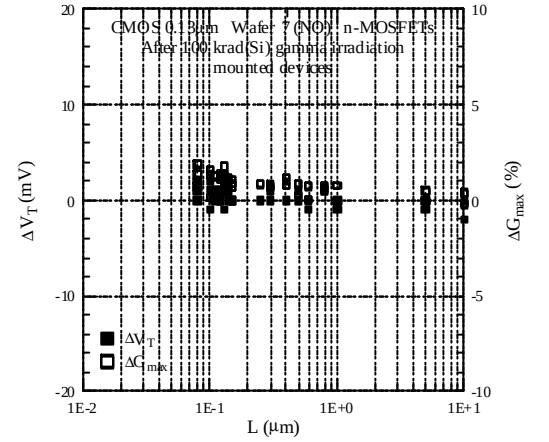
threshold voltage. The gamma irradiation at an equivalent dose (13.5 krads(Si)) on the same technology, which is reported in the following section, confirms this hypothesis. For a quantitatively similar amount of hole and electron pairs susceptible to be trapped in the oxides there is no significant definitive variation of the electrical parameters.

- A kind of rebound is found for the transconductance and also for the threshold voltage, suggesting a length-dependence of the radiation damage. The observed dependence of the variations of the electrical parameters and the fact that the transition occurs for the same length as the threshold voltage suggest that the parameter variations may be related to the non-homogenous channel doping. This can be caused either by the displacement damage component or by some hydrogen passivation mechanism, whereby the hydrogen is released by the ionisation occurring in the gate dielectric. The expected displacement damage at a fluence of 10^{11} p/cm^{-2} is, however, very low (about 10^{12} cm^{-3} radiation defects have been found in diodes irradiated at the same time). This is confirmed by the C-V and the body factor analyses, showing no clear change in the substrate doping density. The hydrogen passivation mechanism is expected to be operative for the n-MOSFETs and less probably for the p-channel devices. However, a similar amount of ionization should occur for 10^{11} p/cm^2 and for 13.5 krad(Si) gamma's. In the next part, a full description of the experimental data after gamma irradiation is presented.

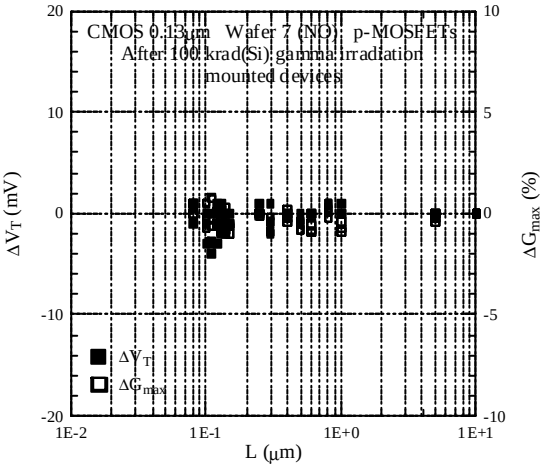
II.1.1.4 Post Gamma-Irradiation Results

Figure 10 shows the threshold voltage shift (ΔV_T) and the maximum transconductance degradation (ΔG_{max}) after 100 krad(Si) gamma irradiation of mounted n- and p-MOS devices with NO and RNO gate dielectrics. For all the devices studied, very small shifts of the threshold voltage (generally below 4mV) were registered. However, these appeared to be somewhat higher in the case of the shortest ($L<0.25$ μm) transistors and, statistically

speaking, ΔV_T values seem to be more positive in the case of n-channel devices and more negative for their p-channel counterparts. Very small changes of G_{max} (generally below 2%) were also registered for all the devices studied. As for the ΔV_T results, these appeared to be somewhat higher in the case of the shortest ($L<0.25\,\mu m$) transistors and, statistically speaking, ΔG_{max} values were positive in the case of the n-channel transistors and negative for the p-channel devices.



(a)



(b)

Figure 10: Threshold voltage shift and maximum transconductance degradation vs. channel length after 100 krad(Si) gamma irradiation for (a) mounted n-MOSFETs and (b) mounted p-MOSFETs with NO gate dielectric.

The V_T and G_{max} values extracted for n-MOS devices with a RNO gate oxide before and after a low dose gamma irradiation (13.5 krad(Si)) show no

clear trends for the device degradation. The V_T and G_{max} values after irradiation tend to be slightly lower in the case of the shortest devices (L<0.3µm) and higher in the case of the longest ones (L≥0.3µm). Also in the case of the p-MOS transistors the V_T and G_{max} values were found to be always lower after gamma irradiation. Unfortunately, in the case of the longest (L≥0.25µm) p-MOS devices, high gate leakage currents were already present before irradiation. In this way, the fact that no reverse short channel shape was observed for the V_T values could be associated with their gate weakness.

The interface trap density after irradiation has been investigated by using both gated diode measurements and low frequency noise studies. Gated diode measurements do not show a clear change that could allow to privilege one hypothesis about the origin of the strong variation observed for the n-MOSFETs. Noise measurements performed before and after gamma irradiation (illustrated in Fig. 11), in the ohmic regime (small V_{DS}) are in agreement with both C-V and gated diode measurements which indicates that after some time, the devices recover to their initial electrical characteristics.

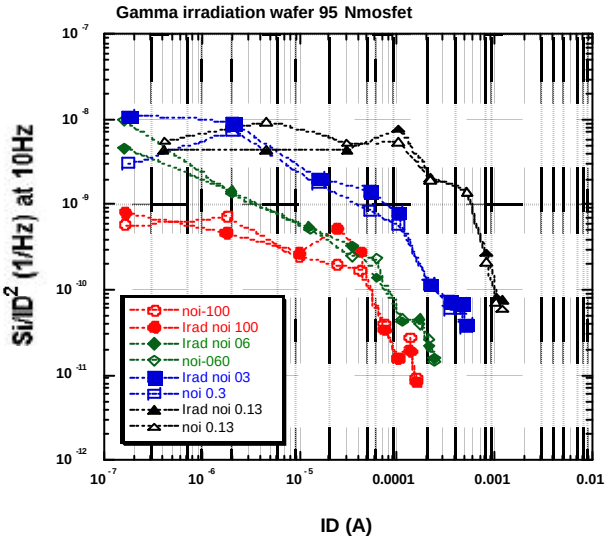


Figure 11: Normalized noise power spectral density $S_I(f)$ versus the drain current before and after 100 krad(Si) gamma irradiation for different channel lengths L=1, 0.6, 0.3, 0.13 µm.

In fact, complementary measurements like high frequency C-V, gated diode and low frequency noise have been performed 10 days after the irradiation, whereas the I-V measurements have been done less than 4 hours after the exposure.

II.1.1.5 Conclusions from the First Gamma- and Proton Irradiation Testing Round

From this initial study we can conclude that the 0.13 µm IMEC technology can withstand a high proton fluence or gamma irradiation dose at least in the range of interest for space applications.

Shallow trench isolation allows to eliminate the radiation-induced leakage current often measured for the other isolation schemes. Therefore, no variation has been observed for the subthreshold regime. This STI makes the W-arrays quite insensitive to radiation damage. Moreover, it should be remarked that partially depleted 0.13 µm Silicon-on-Insulator (SOI) transistors irradiated at the same time did show evidence of radiation-induced edge leakage. This will be reported more in detail in the next section.

The gamma irradiation, operated at nearly the same total ionisation dose as for the proton irradiation, did not show noticeable variation for most of the devices. Only the RNO n-MOSFETs showed a change but it was also observed that this variation was very unstable and disappeared after a few days of room temperature (unbiased) annealing. This was not the case for the proton-induced changes, which remained stable several weeks after the irradiation.

For the proton irradiation we observed interesting variations for the n-MOSFETs L-arrays. For the mounted devices irradiated under bias the main variation is related to an increase of the transconductance for the short channels. But for the unmounted ones the variations are more complex. A kind of rebound is found for the transconductance and also for the threshold voltage, suggesting a length-dependence of the radiation damage.

The dependence with L of the variations of the electrical parameters suggests that they are related to the non homogenous channel doping. This

points out that the contribution of the substrate degradation to the device performance (doping neutralization or deactivation) may dominate an eventual degradation of the isolation trenches and spacers.

The lateral non-uniform doping can be schematically pictured as a Gaussian shaped “pile up” near the drain and the source. Recent analysis of the effective channel doping extracted from the curves of $I_D(V_G)$ versus substrate bias showed that this effective value did not change significantly after proton irradiation. But the sensitivity to small variations near the drain and source of this effective doping parameter is not high. So, to gain better insight on the probable importance of the doping profile near the drain and source, numerical simulations could be performed to investigate qualitatively the physical mechanisms that can induce the measured variations

II.1.2 Results Obtained from the Second Round of Radiation Testing

This section of the report gives a brief overview of the results and conclusions coming from the second gamma and proton irradiation round. It should be considered as a type of summary of the extensive information reported in deliverable D5 (P35288-IM-RP-0004).

II.1.2.1 Technological and Irradiation Details

The Commercial-Off-The-Shelf (COTS) approach currently pursued by the space electronics community goes hand in hand with technology scaling. In other words, due to the reduction of the gate dielectric thickness an implicit hardening has been achieved which brings commercial microelectronic components within the range of space applications, without the need for expensive technology hardening. At the same time, it has become clear that for the sub 100 nm era, SOI is entering mainstream technology, indicating that it is no longer restricted to niche markets and it may be the ultimate solution at the end of the roadmap. Combining these two trends, the question rises whether deep submicron SOI CMOS is suitable for operation in the space radiation environment?

Early studies pointed out that although SOI has many advantages from a radiation-hardness perspective, charging of the buried oxide (BOX) may yield unacceptably high subthreshold leakage in n-channel devices. Although there is a tendency for reducing the BOX thickness, while at the same time, novel high-quality SOI substrates have conquered the market, recent investigations demonstrate still substantial charge trapping, both for SIMOX and UNIBOND materials. Using a thin gate dielectric below the tunnelling limit drastically improves its radiation hardness. However, concern has recently emerged related to some novel degradation phenomena, which are associated with the creation of traps or localized leakage current paths in the gate oxide. This gives rise to so-called Radiation-Induced Leakage Current (RILC) and soft breakdown. Finally, in recent papers, evidence has been advanced that in deep submicron technologies, a length-dependent radiation response may exist, whereby the degradation of the static device parameters, like the threshold voltage V_T, the transconductance g_m and the subthreshold slope S becomes higher for shorter gate lengths L_m. It is, therefore, worthwhile to study the radiation effects in 0.13 µm PD SOI CMOS, which is the subject of the activities performed in association with the second irradiation round.

For the second irradiation round also devices from the standard IMEC's 0.13 µm CMOS technology were used. In addition irradiations have been performed on partially depleted (PD) SOI n-MOSFETs fabricated in a 0.13 µm SOI process, using a Polysilicon Encapsulated Local Oxidation of silicon (PELOX) isolation scheme, a 2.5 nm Nitrided gate Oxide (NO), a 150 nm polysilicon gate and 80 nm nitride spacers. Processing was done on 200 mm UNIBOND wafers, with a Buried Oxide (BOX) thickness of 400 nm and a final film thickness of 100 nm. Wafer splits with (wafer 18) and without (wafer 17) a HALO implantation have been fabricated. The test structures consist of transistor arrays with common gate/common source configuration, separate drain pads and no film contact, which were not biased during the exposures. The gate width W=10 µm. Also W-arrays have been characterized, having a constant device length L_m of 10 µm.

The 60 or 65 MeV proton irradiations were performed at a fluence Φ of 0.5, 1 or 5×10^{11} p/cm^2.

II.1.2.2 Post Proton-Irradiation Results on 0.13 mm PD SOI Devices

Already in 2001 some initial proton irradiation testing has been performed. Both 60 MeV protons at Louvain-La-Neuve (LLN) and 7.5 MeV proton irradiations at Demokritos have been used. However, a more in depth study was executed during the different irradiation rounds in 2002. A 60 MeV proton irradiation testing was done on August 20-21 at LLN. Both chips and mounted devices related to the partially depleted (PD) 0.13 µm SOI technology were irradiated. A similar set of devices was exposed on October 1 irradiated with 65 MeV protons.

The overall conclusion of the initial irradiation testing in 2001 was that the investigated 0.13 µm PD SOI technology is radiation-hard from a viewpoint of space applications. This was validated by the limited damage observed after 7.5 and 60 MeV proton irradiation, implying no peculiar problems related to displacement damage. In addition, total ionizing dose studies up to 100 krad(Si) yielded similar minor device degradation. The main effect is the development of a subthreshold leakage current in the n-channel transistors, which could be related to edge or back-channel leakage. This effect was absent in the p-MOSFETs. In addition, a small increase of the V_T and of g_{mmax} was observed for the n-MOSFETs, which is more pronounced for the shorter device lengths. The origin of the changes was not clear at the start of the second irradiation round, but could have been related to dopant de-activation along the channel. In some cases, as clearly illustrated by Fig. 12., RILC could be observed after 60 MeV proton irradiations, pointing to the creation of neutral bulk oxide traps. Another peculiar, and new phenomenon observed for the first time, is the so-called Linear Kink Effect (LKE) associated with the second peak in the transconductance as shown in Fig. 13.

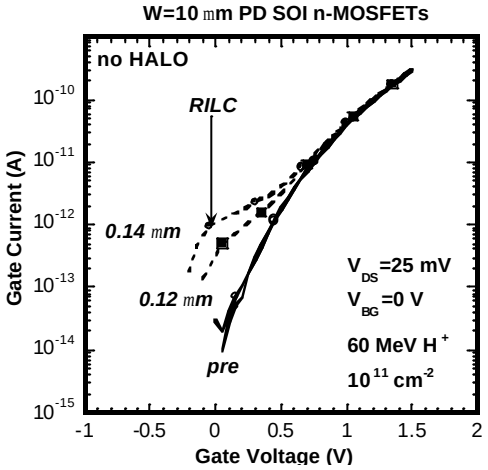


Figure 12: RILC in two 60 MeV proton-irradiated PD SOI n-MOSFETs, belonging to the same array, without HALO implantation. V_{BG}=0 V.

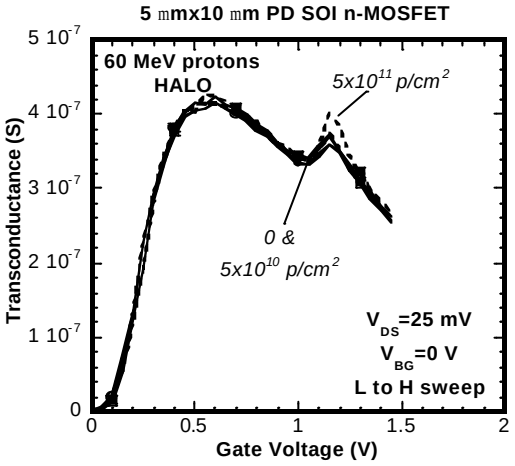


Figure 13: Transconductance at V_{DS}=25 mV before (0) and after 60 MeV proton irradiation, for different fluences, obtained for a W=5 µm, L_m=10 µm PD SOI n-MOSFET with HALO implant. V_{BG}=0 V

The enhanced gate leakage (RILC) for low gate voltage is believed to be associated with trap-assisted-tunneling (TAT) through radiation-induced neutral defect centers created in the ultra-thin oxide. The LKE effect, which has a lot of resemblance with the well-known impact ionisation induced kink in floating body SOI devices, can be explained by a hole generation mechanism related to valence band electron tunnelling. For sufficiently high gate biases (> 1.1 V) electron tunnelling occurs from the silicon valence band to the conduction band in the polysilicon gate (EVB process).

The main conclusions from the 2002 proton irradiation round are:

- The observed degradation in the irradiated mounted n-MOSFETs could be simply explained by a positive charge trapping (about $6 \cdot 10^{11}$ effective charges/cm^2) in the buried oxide, which would be also responsible for the observed back gate threshold voltage shift of about 13-14 Volts.
- These phenomena may be explained also in terms of a lateral isolation parasitic transistor and/or any other radiation-induced degradation mechanism.
- The observed degradation in the irradiated on-wafer n-MOSFETs could be simply explained by a positive charge trapping (about $2.2 \cdot 10^{11}$ effective charges/cm^2) in the buried oxide, which would be also responsible for the observed back gate threshold voltage shift of about 4.5 Volts.
- The analysis of the geometry (W and L) dependence of the hump, as well as of the back gate threshold voltage, could give some answer to the above questions.
- The measurement of a gated diode could give direct knowledge of the back gate threshold voltage (eliminating the MOSFET's possibility of any coupling effect between the two gates).
- Low frequency noise measurements pointed out that there is an excess low frequency noise component associated with the LKE, similar to the well-known excess LF noise associated with the kink effect observed in floating body n-channel SOI devices. This is illustrated in Fig. 14, indicating that proton irradiation enhances the excess LF noise.

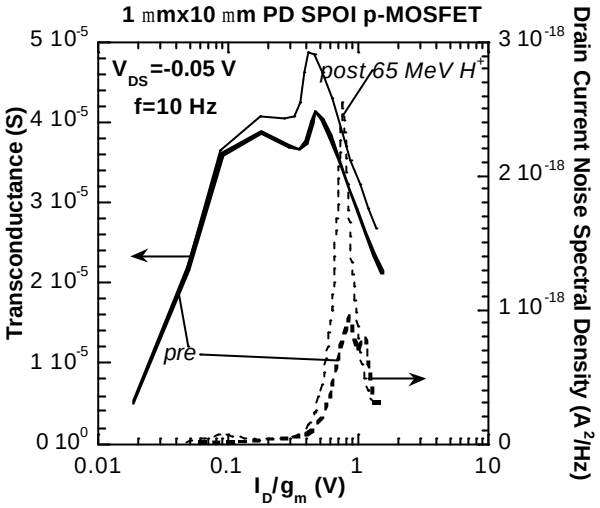


Figure 14: Transconductance and current noise spectral density S_I versus gate overdrive voltage for a 1 µm PD SOI p-MOSFET before and after a 65 MeV proton irradiation.

II.1.2.3 Post Proton-Irradiation Results on 0.13 mm CMOS Devices

In section II.1.1.3 it was pointed out that additional irradiation testing would be helpful to get a better insight into the degrading mechanisms observed for the L-arrays of n-MOSFETs irradiated under or without bias. The goal is to analyse the eventual role of substrate degradation on the extracted variations. For this additional testing 65 MeV protons have been used.

The most important conclusions that can be drawn from this additional irradiation round are:

- The 0.13 µm bulk CMOS technology can withstand a high proton fluence and irradiation dose in the range of interest for space applications.
- The process used in IMEC for shallow trench isolation allows eliminating the radiation-induced leakage current often measured for the other isolation schemes. Therefore, no variation has been observed for the subthreshold regime. For the proton irradiation we observed interesting variations for the n-MOSFETs L-arrays. For the irradiated n-MOSFETs devices the main variation is related to an increase of the transconductance for the short channels. From the data generated during the first and second irradiation round, and in spite of the great diversity of measurement

techniques used, one can not give a clear picture from the physical mechanism responsible for the observed channel length degradation dependence. The same degradation behavior is also reported for SOI deep submicron MOSFETs.

- These fundamental questions do not impede using this technology for space application, but a clear answer could provide a technological solution to improve it. Therefore as we continue to suspect both the impact of ultra thin gate oxides and substrate characteristics to be a possible explanation, it is worthwhile to perform the same complete analysis on the next devices generations with thinner gate oxide thickness. One should also keep in mind that for both SOI and bulk MOSFETs tested during the execution of this Work Order, the test structures had a common gate. Therefore, as for the linear kink effect a reduced gate area in isolated devices can suppress this channel length degradation dependence.
- One could also perform some characterization at higher doses, probably out of the range that interests space engineering. These experiments, which are amplifying the degradation, could help to localize and identify the mechanism responsible for the degradation at lower dose if one supposes that they remain identical.

II.2 Conclusion

Based on the extensive radiation studies performed on the 0.13 µm CMOS technology node, it can be concluded that from a viewpoint of total ionising dose and displacement damage no problems should be expected up to 100 krad(Si). The gate dielectric, the spacers and the STI isolation maintain their integrity throughout the irradiation experiments. This is not true for the BOX of the SOI devices, where hardening measures could be necessary – i.e., by the introduction of electron traps through application of an ion implantation. It is also clear that the bias condition during the irradiation plays an important role in the final amount of degradation. Therefore, the following issues remain open and could be topics for future research:

- A more detailed investigation of the impact of the bias during the irradiation of PD and Fully Depleted SOI n-MOSFETs.
- Although the STI gives no problems at room temperature, it has been observed that at 77 or 4.2 K, a subthreshold hump is observed related to edge conduction along the STI. The question is whether this problem aggravates under ionizing irradiation or not? This is an important issue if these deep submicron technologies are to be used for cryogenic space applications.
- There is still no conclusive evidence or model to explain the "mysterious" length-dependent degradation observed both on SOI and bulk MOSFETs. There are clues that it can be related to the two-dimensional lateral doping profile in the well/body region. Summarizing the observations so far: the effect is clearly visible after high energy proton irradiations, while it is not obvious after γ-irradiations. The largest degradation is found for unbiased irradiations and for device lengths around the peak of the V_T (~0.2 µm). In most cases, an increase of V_T and g_{mmax} is observed, although the opposite 'rebound' behaviour can also be found, depending on the array. Therefore, there seems to be some statistical factor, which could be related to an extreme displacement damage event in the case of protons (similar as for the damage distributions in CCD pixels). There is possibly a correlation with the occasionally observed degradation of the gate current characteristics.
- The occurrence of radiation-induced leakage current (RILC) after low fluences of 60 MeV protons could be a problem for future CMOS technologies and points to the fact that there still exist gate dielectric degradation mechanisms which need taking care of.
- It is also worthwhile to further investigate the impact of irradiation on the new floating body effects, which are related to the gate tunneling current and giving rise to the LKE in SOI transistors. With a further scaling of the gate oxide thickness this problem can only become worse. This is of interest in the first place from a device physics viewpoint.

CONCLUSIONS AND OUTLOOK

In general it can be stated that the two Activities have successfully been completed and within the originally envisaged time schedule. A very strong basis for the execution of the work was the activities performed within the frame of the previous Work Order. The then started literature study and the experimental work finally resulted in a book on "Radiation Effects in Advanced Semiconductor Materials and Devices, C. Claeys and E. Simoen, Springer Verlag, August 2002.

The most important conclusions from the first Activity related to Cryogenic Irradiation Effects are:

- Room temperature radiation testing is not sufficient to obtain a good picture of the device/circuit performance during real space missions such as e.g. HERSCHEL.
- There is a strong difference in the radiation response between room temperature and liquid helium temperature irradiations. Both gamma and proton irradiations have to be performed.
- There might be a large spread in circuit performance after cryogenic irradiations, in agreement with other reports for COTS microelectronics.
- Device response cannot be used to predict the circuit response. The latter correspond with the real situation, while the former one is useful to get insight into the underlying physical mechanisms. A good understanding of these mechanisms is needed to define technological or design modifications for improved radiation hardness.
- Cryogenic proton and gamma irradiations have successfully been executed. This resulted in the generation of a Cryogenic Irradiation Manual, outlining practical aspects and safety issues. This can be considered as a very important achievement and milestone.

The most important conclusions from the second Activity related to Radiation Effects in Advanced Semiconductor Materials and Devices are:

- From a viewpoint of both displacement damage and total ionisation dose the IMEC's 0.13 µm bulk CMOS technology is sufficiently hard up to 100

krad(Si). Good integrity is maintained for the gate dielectric, the spacers and the shallow trench isolation scheme.

- For the BOX of the IMEC's 0.13 µm SOI technology, some hardening measures may be needed.
- Bias during irradiation has a strong impact on the performance degradation.
- There is still no good physical model to explain the observed gate length dependence of the performance degradation after irradiation, especially for protons.
- For future scaled down technologies, RILC should be carefully monitored.

This work clearly demonstrated that the COTS approach looks very promising for deep submicron technologies, but dedicated radiation testing is surely required. Suggestions for future activities in this field include:

- Getting a better physical insight into some of the peculiarities observed during the study of the 0.13 µm CMOS technology. Although they surely do not limit the use of these devices for space applications, such a study would give more insight into possible long term reliability hazards and would point out the importance of some technological parameters.
- Radiation assessment of future technology nodes down to 70 nm. Both room temperature and cryogenic irradiations are envisaged. Special attention has to be given to the use of advanced process modules such as thin gate oxides, isolation, device engineering and salicides.
- The study of the radiation performance of devices with dual gate thickness. These are gaining strong importance for system-on-chip applications. In this case, a thin gate dielectric corresponding with the low power/high performance logic part is combined with a 'thick' (up to 5 nm) high voltage analogue part. Another important feature in the context of analogue applications is the study of the radiation hardness of the capacitor modules (Metal-Insulator-Metal – MIM or Polysilicon-Insulator-Metal) which are nowadays co-integrated on the same wafer. Especially their

performance at lower temperature may cause problems, related to strong capacitor non-linearities.

- Radiation assessment of high-k dielectrics. The low power applications are the driving force to replace the ultra thin SiO_2 gate dielectrics by a high-k dielectrics such as HfO_2, ZrO_2, Al_2O_3…. A large variety of these materials are worldwide under investigation. The present information on their radiation hardness is very scarce and systematic studies will surely be needed.
- Impact of irradiation on the SEU performance of 0.18 µm CMOS technologies. Both technological and design aspects have to be taken into account, whereby the emphasis should be on a more fundamental study of SEU. For that purpose, it is considered to irradiate besides circuits also more simple test structures and basic building blocks, which should enable assessment of the basic parameters and mechanisms.
- SOI is playing a more dominant role in commercial applications. It is therefore important for state of the art SOI technologies (i.e. thin film, fully or partially depleted devices, etc) to investigate the impact of key SOI parameters (substrate quality, buried oxide layer, fabrication technique….) on the radiation hardness of devices with leading edge feature sizes (technology nodes between 130 and 70 nm).

Some of the above mentioned studies are essential for some missions to be launched in the coming years, while other ones (e.g. study of deep submicron technologies) are required to increase the confidence level in the use of COTS devices fabricated in a scaled down technology,

APPENDIX: DOCUMENT CATALOGUE

P35288-IM-PP-0001: Proposal for: Radiation Effects Study of Components Operated at Cryogenic Temperatures and Future Generation Semiconductor Devices

Minutes

P35288-IM-MM-0001: Minutes of the Negotiation meeting held at ESTEC on February 14, 2001

P35288-IM-MM-0002: Minutes of the Midterm Review Meeting held at IMEC on March 22, 2002

Progress Reports

P35288-IM-PR-0001: Progress Report nr. 1

P35288-IM-PR-0002: Progress Report nr. 2

P35288-IM-PR-0003: Progress Report nr. 3

P35288-IM-PR-0004: Progress Report nr. 4

P35288-IM-PR-0005: Progress Report nr. 5

P35288-IM-PR-0006: Progress Report nr. 6

P35288-IM-PR-0007: Progress Report nr. 7

P35288-IM-PR-0008: Progress Report nr. 8

P35288-IM-PR-0009: Progress Report nr. 9

P35288-IM-PR-0010: Progress Report nr. 10

P35288-IM-PR-0011: Progress Report nr. 11

Technical Notes

P35288-IM-TN-0001: Irradiation Plan for the Study of Future Generation Semiconductors - Irradiation Round 1 of Activity 2

P35288-IM-TN-0002: Irradiation Plan for the Study of Future Generation Semiconductors - Gamma Irradiation Round 1 of Activity 2

P35288-IM-TN-0003: Irradiation Plan for the Study of Future Generation Semiconductors - Cryogenic Gamma Irradiation Round 1 of Activity 1

P35288-IM-TN-0004: Irradiation Plan for the Study of Future Generation Semiconductors - Proton Irradiation Plan Activity (Round 1) and Activity 2 (Round 2)

Deliverables

P35288-IM-RP-0001: 60 MeV Proton and Gamma Irradiation Effects on NO and RNO Deep Submicron MOSFETs Fabricated in IMEC's 0.13 µm CMOS Technology
(Deliverable D4)

P35288-IM-RP-0002: Cryogenic Irradiation Facility Assessment/Installation
(Deliverable D1)

P35288-IM-RP-0003: Cryogenic Proton and Gamma Irradiations of Devices and Circuits Processed in a 0.7µm CMOS Technology intended to be used for the HERSCHEL Space Observatory
(Deliverable D2)

P35288-IM-RP-0004: 60 MeV Proton and Gamma Irradiation Effects on Deep Submicron MOSFETs Fabricated in IMEC's 0.13 µm CMOS Technology and in IMEC's 0.13 µm Partially Depleted SOI Technology. – Radiation Round 2.
(Deliverable D5)

P35288-IM-RP-0005: Updated Cryogenic Irradiation Manual.
(Deliverable D3)

P35288-IM-RP-0006: Final Report.
(Deliverable D6)

Publications

"60 MeV proton irradiation effects on NO-annealed and standard-oxide deep submicron MOSFETs", E. Simoen, J. Hermans, A. Mercha, W. Vereecken, C. Vermoere, C. Claeys, E. Augendre, G. Badenes and A. Mohammadzadeh, presented at RADECS 2001, Grenoble (France), Sept. 10-14, 2001.

"Shallow Trench Isolation and Source and Drain Extension Conduction in a 0.13 μm CMOS Technology at Low Temperatures", A. Mercha, J.M. Rafi, E. Simoen, E. Augendra and C. Claeys, presented at WOLTE 5, Grenoble, France, June 19-21, 2002

"Short-Channel Radiation Effect in 60 MeV Proton Irradiated 0.13 μm CMOS Transistors", E. Simoen, A. Mercha, A. Morata, K. Hayama, G. Richardson, J.M. Rafi, E. Augendre, C. Claeys and A. Mohammazadeh, presented at the RADECS 2002 Workshop, Padova (Italy), Sept. 19-20, 2002