SINGLE EVENT EFFECTS RADIATION TEST REPORT

Part Type : AT60142E

4 Mb SRAM

Manufacturer : ATMEL

Report Reference : ESA_QCA0216S_C

Issue : 01

Date : December 17th, 2002

ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

ESTEC Technical Officer: R. Harboe Sorensen

Hirex reference :	HRX/SEE/0073	Issue : 01	Date :	December 17th, 2002
Prepared by :	J.G. LOQUET	[signature]	Date :	December 17th, 2002
Checked by :	F.X GUERRE	[signature]	Date :	December 17th, 2002
Approved by :	J. F. MOUNES	[signature]	Date :	December 17th, 2002

Heavy ion SEE characterization of AT60142E SRAM

TABLE OF CONTENTS

List of Tables:

List of Figures:

1 Abstract

Under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02 covering "Radiation Evaluation of COTS Semiconductor Components: “Radiation evaluation of parts for new VME design", AT60142E SRAM memories were radiation assessed.

Results from these assessments, primarily focusing on the sensitivity of these devices to Single Event Effects (SEE), are reported in this report.

2 INTRODUCTION

This report presents the results of a Single Event Effects (SEE) test program carried out on AT60142E SRAMs, from ATMEL.

Test was conducted on Rad Hard samples delivered by ESA.

These devices were used for heavy ion test at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.

This work was performed for ESA/ESTEC under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02.

3 REFERENCE DOCUMENTS

RD1. AT60142E data sheet
RD2. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD3. The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

4 DEVICE INFORMATION

4.1 AT60142E

Relevant device identification information is presented here after.

Part type:	AT60142E
Manufacturer:	ATMEL
Package:	36-pin flatpack
Quality Level:	Rad Hard
Date Code:	0203
Top Marking:	T AT60142E SAMPLE 0203 1T5926
Die Size:	11.4 mm x 6.2 mm approximately
Die marking	ATMEL NANTES 2001 AT57R00 60142E
Serial number	SN1, SN2 and SN3 (attributed by Hirex)

The AT60142E is a Rad Hard 512K x 8 3.3-Volt very low power CMOS SRAM.

Die identification is provided in Figure 1.

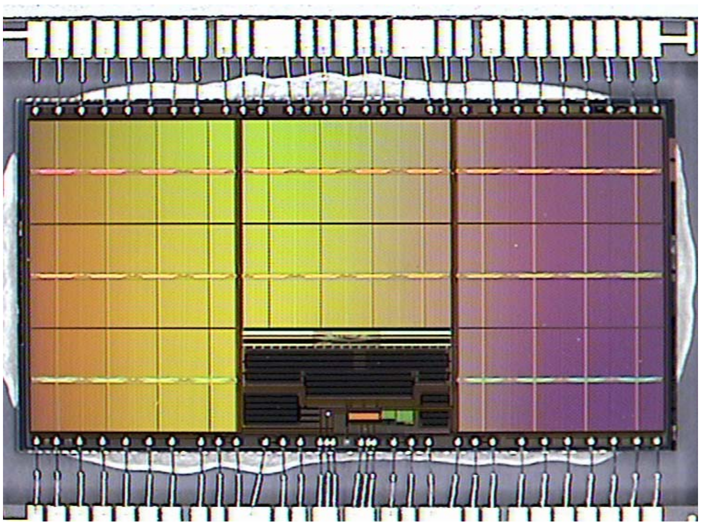

Photo 1

Die, full view

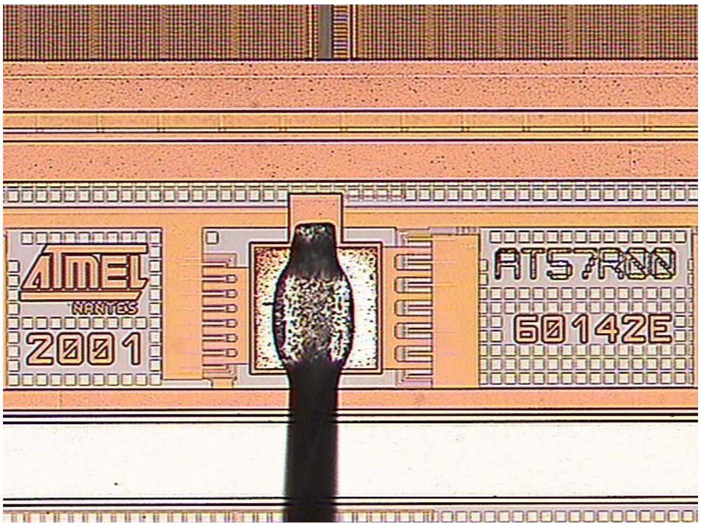

Photo 2

Die marking

Figure 1 - AT60142E die identification

5 Test Definition

5.1 Test Set-up

Hirex test equipment is composed of a modular rack coupled with a generic memory test board:

This modular rack is derived from iTest BILT modular instrumentation system and presents 8 slots for modular instruments.
In addition to the existing power supply modules which cover the SEE test needs for precision measurements, remote control, LU detection, data storage, scope observation, etc, a specific modular board has been designed to provide:

- A high speed communication link with the test board under vacuum (up to 500 ko/s)
- Particle and test time counting

Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board includes programmable logic circuits with a total capacity of 30000 cells and 960 macrocells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Today, the board has a capacity of 80 pin-drivers, using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

5.2 Test Configuration

Two basic configurations were used:

STATIC TEST MODE:

1. Device initialization
2. Write the test pattern in the memory and perform a read to check eventual stuck bits
3. Expose the device to the beam for a given time (typically 10s). At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Read the memory and count the errors
5. Loop with step 2, etc

DYNAMIC TEST MODE:

1. Device initialization
2. Write the test pattern in the memory and make a read to detect eventual stuck bits
3. Expose the device to the beam for a given time and perform continuous read-write operations. At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Loop with step 2, etc

The table here below provides, for each group of 4 bits, the 14 words repetitive pattern.

	It k	It k+1	It k+2	It k+3	It k+4	It k+5	It k+6	It k+7	It k+8	It k+9	It k+10	It k+11	It k+12	It k+13	It k+14
address n	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000
address n+1	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010
address n+2	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101
address n+3	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111
address n+4	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001
address n+5	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110
address n+6	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101
address n+7	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000
address n+8	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010
address n+9	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101
address n+10	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111
address n+11	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001
address n+12	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110
address n+13	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010
address n+14	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000

Table 1 - Test Pattern

Errors which can be detected and counted are the following:

- Any single error in the memory block with identification of the transition (1->0 or 0->1)
- Any word with at least one bit flip with the identification of the word address

DUT power supply module is monitored and each time the current consumption exceeds a programmable threshold, a power reset cycle is done and latch-up error counter is incremented.

In addition the use of fast latch-up detection with a high speed comparator avoids the counting of SEU errors which could be induced by the latch-up condition.

DUT power supply is 3.3V.

6 TEST FACILITIES

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain-La-Neuve (Belgium) under HIREX Engineering responsibility.

6.1 Beam Source

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions was built and installed on the HIF beam line in the experimental hall of Louvain-La-Neuve cyclotron.
CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula:

$$110\ Q^2/M,$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows producing highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

6.2 Beam Set-up

6.2.1 Ion Beam Selection

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.
For each run, information is provided on the beam characteristics in the detailed results table in paragraph 7.

6.2.2 Flux Range

For each run, the averaged flux value is provided in the detailed results table of paragraph 7.

6.2.3 Particle Fluence Levels

Maximum fluence level was set to 1 E6 ions/cm²

6.2.4 Dosimetry

The current UCL Cyclotron dosimetry system and procedures were used.

6.2.5 Accumulated Total Dose

For each run, the computed equivalent cumulated doses received by the DUT sample, are provided in the detailed results table of paragraph 7.

6.2.6 Test Temperature

Tests have been performed at 22 deg. C.

6.3 Available ions

The most commonly used ions at the UCL HIF facility are listed along with some of their features in the table here below:

Ion Specie	Energy	LET	Range
	(MeV)	(MeV.cm²/mg)	µm
10-B	41	1.7	80
20-Ne	78	5.85	45
40-Ar	150	14.1	42
84-Kr	316	34	43

Table 2 – HIF ions

The use of a tilt angle allows intermediate effective LETs.

7 RESULTS

The detailed results per run for each device are presented in Table 3.

The corresponding SEU cross-section per bit vs. Effective LET curve is shown on Figure 2

The device turned out to be quite sensitive to SEU, as upsets were detected with an LET as low as 1.70 MeV.cm²/mg. No functional errors were observed during these runs. However, three Large Errors (LE) occurred during runs 20, 21 and 27 at a LET of 28.2 MeV.cm²/mg . An example of LE is represented on Figure 3, and can be compared to the case where no LE occurred and all upsets are randomly distributed, as seen on Figure 4. Asymptotic cross section per bit appears to be around 3.5E-8/cm².

SEL occurred in these devices at an LET of 28.2 MeV.cm²/mg. Analysis of the runs log files show that these latch-up are observed when a read or a write of the memory is performed.

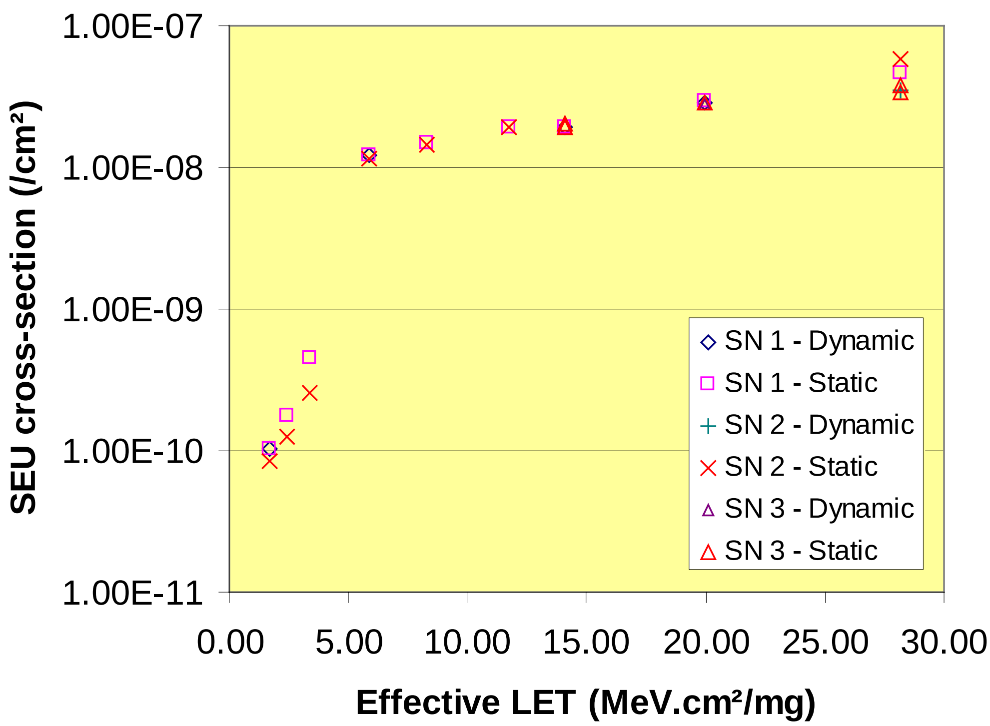

Figure 2 - SEU cross-section per bit vs. effective LET curve for AT60142E

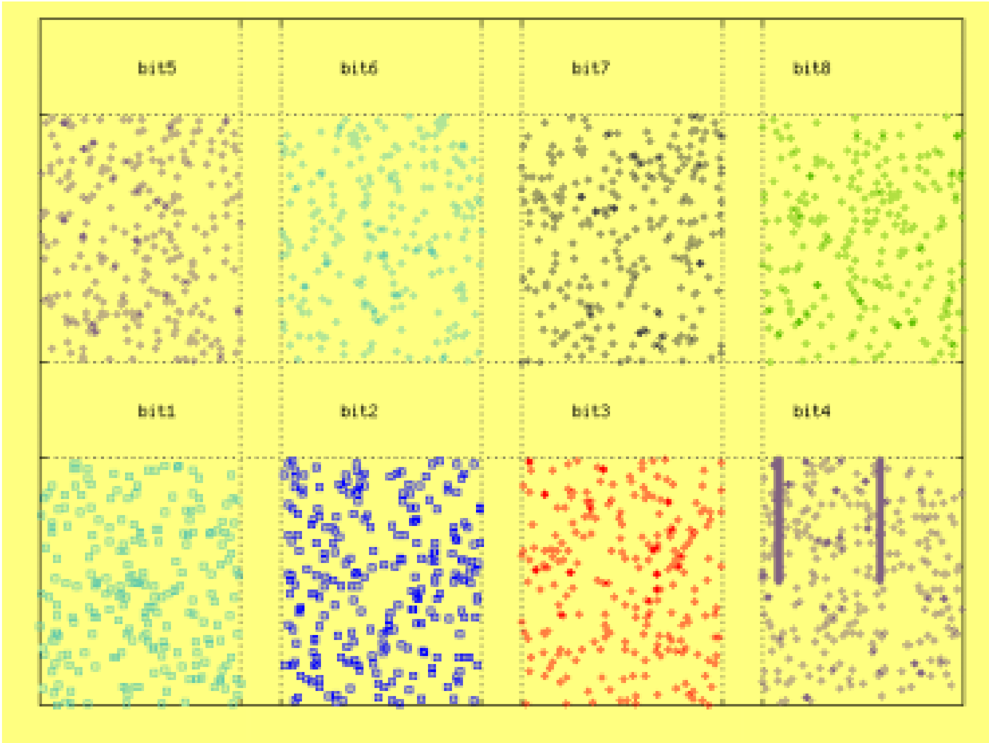

Figure 3 - Example of Large Error. A large row error occurred on bit 4 (Run 21). All other upsets are randomly distributed.

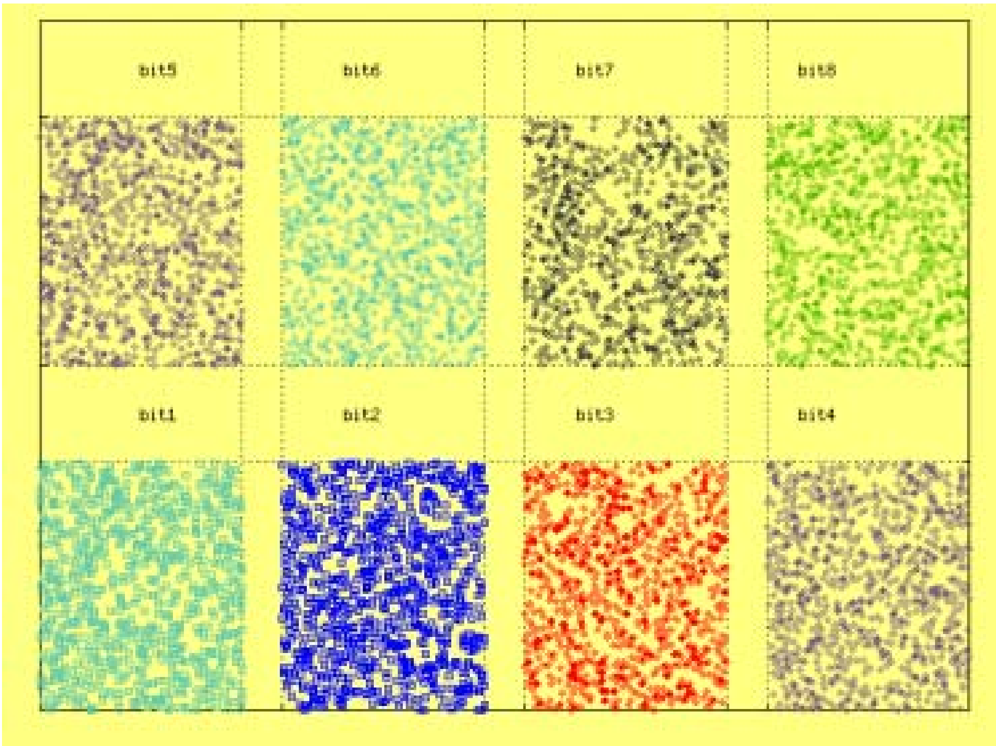

Figure 4 - Distributions of errors in (row, column) coordinates for each bit. In that case (run 25) all errors (each represented by a single symbol) are randomly distributed.

Run #	S/N	Test mode	Ion	LET (MeV.cm²/mg)	Angle (°)	Eff LET (MeV.cm²/mg)	Time (s)	Effective time (s)	Fluence (/cm²)	Flux (/cm²/s)	SEU (Words)	Large Errors	Corrected SEU (Words)	Bits Up (0 to 1)	Bits Down (1 to 0)	Total Bits (Up+Down)	SEU cross-section per bit (/cm²)	SEL
108	1	D	B	1.70	0	1.70	143		1.00E+06	6993	435	0	435	210	225	435	1.04E-10	0
107	1	S	B	1.70	0	1.70	140		1.00E+06	7143	429	0	429	195	234	429	1.02E-10	0
109	1	S	B	1.70	45	2.40	201		1.00E+06	4975	743	0	743	389	354	743	1.77E-10	0
110	1	S	B	1.70	60	3.40	295		1.00E+06	3390	1914	0	1914	999	915	1914	4.56E-10	0
73	1	D	Ne	5.85	0	5.85	159		7.77E+04	489	3999	0	3999	2003	1996	3999	1.23E-08	0
72	1	S	Ne	5.85	0	5.85	291		2.35E+04	81	1210	0	1210	563	647	1210	1.23E-08	0
74	1	S	Ne	5.85	45	8.27	160		1.34E+05	835	8442	0	8442	4328	4119	8447	1.51E-08	0
75	1	S	Ne	5.85	60	11.70	237		1.41E+05	594	11431	0	11431	5794	5644	11438	1.94E-08	0
23	1	D	Ar	14.10	0	14.10	225		9.42E+04	419	7550	0	7550	3855	3695	7550	1.91E-08	0
22	1	S	Ar	14.10	0	14.10	186		9.51E+04	511	7604	0	7604	3874	3733	7607	1.91E-08	0
25	1	D	Ar	14.10	45	19.94	248		6.00E+04	242	7299	0	7299	3684	3615	7299	2.90E-08	0
24	1	S	Ar	14.10	45	19.94	248		6.05E+04	244	7524	0	7524	3921	3604	7525	2.97E-08	0
27	1	D	Ar	14.10	60	28.20	198	131	1.72E+04	131	20300	1	2748	-	-	-	3.81E-08	15
26	1	S	Ar	14.10	60	28.20	341		4.84E+04	142	9309	0	9309	-	-	-	4.59E-08	0
111	2	S	B	1.70	0	1.70	136		1.00E+06	7353	351	0	351	173	178	351	8.37E-11	0
112	2	S	B	1.70	45	2.40	192		1.00E+06	5208	533	0	533	265	268	533	1.27E-10	0
113	2	S	B	1.70	60	3.40	281		1.00E+06	3559	1058	0	1058	569	489	1058	2.52E-10	0
76	2	S	Ne	5.85	0	5.85	138		1.60E+05	1156	7645	0	7645	-	-	-	1.14E-08	0
77	2	S	Ne	5.85	45	8.27	154		1.24E+05	802	7436	0	7436	3679	3761	7440	1.43E-08	0
78	2	S	Ne	5.85	60	11.70	155		8.48E+04	547	6833	0	6833	3539	3297	6836	1.92E-08	0
29	2	D	Ar	14.10	60	28.20	254	211	2.14E+04	101	3145	0	3145	1636	1509	3145	3.51E-08	26
28	2	S	Ar	14.10	60	28.20	392		4.27E+04	109	10510	0	10510	5513	5000	10513	5.87E-08	1
15	3	S	Ar	14.10	0	14.10	158		6.82E+04	431	5849	0	5849	2960	2892	5852	2.05E-08	0
16	3	S	Ar	14.10	0	14.10	78		7.28E+04	933	5904	0	5904	2989	2915	5904	1.93E-08	0
18	3	D	Ar	14.10	45	19.94	108		6.87E+04	636	7939	0	7939	3977	3962	7939	2.76E-08	0
17	3	S	Ar	14.10	45	19.94	97		5.53E+04	571	6643	0	6643	3361	3286	6647	2.86E-08	0
20	3	D	Ar	14.10	60	28.20	41	17	6.81E+03	401	112003	2	1007	-	-	-	3.52E-08	7
19	3	S	Ar	14.10	60	28.20	174	170	7.04E+04	414	11144	0	11144	5859	5294	11154	3.77E-08	4
21	3	S	Ar	14.10	60	28.20	67	37	1.37E+04	371	6971	1	1971	4376	2595	6971	3.43E-08	8

(*) S stands for STATIC TEST MODE; D for DYNAMIC TEST MODE

Table 3 - Heavy ion detailed results per run

8 CONCLUSION

Heavy ion tests were conducted on rad hard samples of AT60142E memories from ATMEL, using the heavy ions available at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.

The device was found to be quite sensitive to SEU. No functional errors was observed. A few Large Errors were detected. Most importantly, SEL occurred at an LET of 28.2 MeV.cm²/mg.