SINGLE EVENT EFFECTS
RADIATION TEST REPORT

Part Type : TC55V8200FT

16 Mb SRAM

Manufacturer : TOSHIBA

Report Reference : ESA_QCA0217S_C

Issue : 01

Date : December 17th, 2002

ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02

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The work described in this report was done under ESA contract.
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Heavy ion SEE characterization of TC55V8200FT SRAM

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1 Abstract

Under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02 covering "Radiation Evaluation of COTS Semiconductor Components: “Radiation evaluation of parts for new VME design“, TC55V8200FT SRAM memories were radiation assessed.

Results from these assessments, primarily focusing on the sensitivity of these devices to Single Event Effects (SEE), are reported in this report.

2 INTRODUCTION

This report presents the results of a Single Event Effects (SEE) test program carried out on TC55V8200FT SRAMs, from TOSHIBA.
Test was conducted on commercial samples delivered by ESA.
These devices were used for heavy ion test at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.
The samples' back were mechanically thinned, and they were irradiated from the backside.
This work was performed for ESA/ESTEC under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02.

3 REFERENCE DOCUMENTS

RD1. TC55V8200FT data sheet
RD2. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD3. The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

4 DEVICE INFORMATION

4.1 TC55V8200FT

Relevant device identification information is presented here after.

Part type:	TC55V8200FT
Manufacturer:	TOSHIBA
Package:	54-TSOP
Quality Level:	Commercial
Date Code:	0229
Top Marking:	TOSHIBA YB7731 0229 KAD TC55V8200FT-12

2097152 word by 8 bit CMOS Static RAM, Silicon gate CMOS, 3V3, LVTTL compatible

4.2 Sample preparation

This device presents a Lead on Chip (LOC) construction as shown in Figure 1. It is therefore required to thin the samples for back side irradiation.
One sample was prepared that way with a thickness target of 50 microns +/- 20 microns.

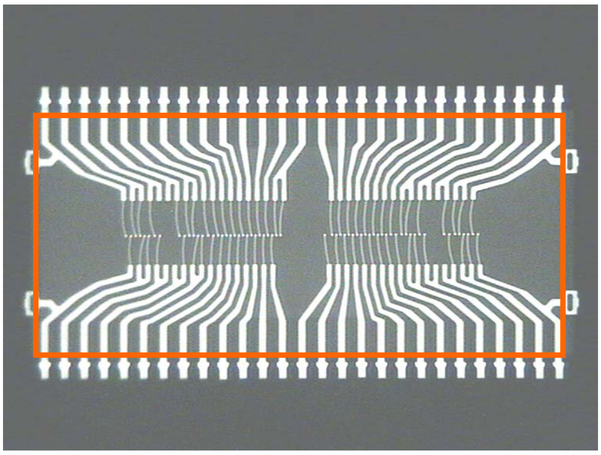

Photo 1 - Package X-ray

One can see the lead frame on the top of the die and the central wires bonding
(Lead On Chip construction)

Die perimeter:

Figure 1 – TC55V8200FT Xray photo

5 Test Definition

5.1 Test Set-up

Hirex test equipment is composed of a modular rack coupled with a generic memory test board:

This modular rack is derived from iTest BILT modular instrumentation system and presents 8 slots for modular instruments.
In addition to the existing power supply modules which cover the SEE test needs for precision measurements, remote control, LU detection, data storage, scope observation, etc, a specific modular board has been designed to provide:

- A high speed communication link with the test board under vacuum (up to 500 ko/s)
- Particle and test time counting

Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board includes programmable logic circuits with a total capacity of 30000 cells and 960 macrocells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Today, the board has a capacity of 80 pin-drivers using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

5.2 Test Configuration

Two basic configurations were used:

STATIC TEST MODE:
1. Device initialization
2. Write the test pattern in the memory and perform a read to check eventual stuck bits
3. Expose the device to the beam for a given time. At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Read the memory and count the errors
5. Loop with step 2, etc

DYNAMIC TEST MODE:
1. Device initialization
2. Write the test pattern in the memory and make a read to detect eventual stuck bits
3. Expose the device to the beam for a given time and perform continuous read-write operations. At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Loop with step 2, etc

The table here below provides, for each group of 4 bits, the 14 words repetitive pattern.

	It k	It k+1	It k+2	It k+3	It k+4	It k+5	It k+6	It k+7	It k+8	It k+9	It k+10	It k+11	It k+12	It k+13	It k+14
address n	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000
address n+1	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010
address n+2	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101
address n+3	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111
address n+4	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001
address n+5	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110
address n+6	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101
address n+7	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000
address n+8	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010
address n+9	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101
address n+10	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111
address n+11	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001
address n+12	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110
address n+13	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010
address n+14	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000

Table 1 – Test pattern

Errors which can be detected and counted are the following:

- Any single error in the memory block with identification of the transition (1->0 or 0->1)
- Any word with at least one bit flip with the identification of the word address

DUT power supply module is monitored and each time the current consumption exceeds a programmable threshold, a power reset cycle is done and latch-up error counter is incremented.

In addition the use of fast latch-up detection with a high speed comparator avoids the counting of SEU errors which could be induced by the latch-up condition.

DUT power supply is 3.3V.

6 TEST FACILITIES

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain-La-Neuve (Belgium) under HIREX Engineering responsibility.

6.1 Beam Source

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions was built and installed on the HIF beam line in the experimental hall of Louvain-La-Neuve cyclotron.
CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula:

$$110\ Q^2/M,$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows producing highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

6.2 Beam Set-up

6.2.1 Ion Beam Selection

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.
For each run, information is provided on the beam characteristics in the detailed results table in paragraph 7.

6.2.2 Flux Range

For each run, the averaged flux value is provided in the detailed results table of paragraph 7.

6.2.3 Particle Fluence Levels

Maximum fluence level was set to 1 E6 ions/cm²

6.2.4 Dosimetry

The current UCL Cyclotron dosimetry system and procedures were used.

6.2.5 Accumulated Total Dose

For each run, the equivalent cumulated dose received by the DUT sample is computed.

6.2.6 Test Temperature

Tests have been performed at 22 deg. C.

6.3 Available ions

The most commonly used ions at the UCL HIF facility are listed along with some of their features in the table here below:

Ion Specie	Energy	LET	Range
	(MeV)	(MeV.cm²/mg)	µm
10-B	41	1.7	80
20-Ne	78	5.85	45
40-Ar	150	14.1	42
84-Kr	316	34	43

Table 2 – HIF ions

The use of a tilt angle allows intermediate effective LETs.

7 RESULTS

The detailed results per run are presented in Table 3.

As expected, this device was improperly tested due to ion penetration limitations in Silicon.

Indeed, a quite high amount of errors were counted with ions featuring a low LET (and therefore a high penetration range), i.e. the 41 MeV B (LET = 1.7, range = 80 µ) , but none were observed with higher LET ions, 78 MeV Ne (LET = 5.85, range = 45 µ) or 150 MeV Ar (LET = 14, range = 42 µ) featuring lower penetration ranges. Moreover, a notable disproportion between the number of errors counted in the 4 MSB and the number counted in the 4 LSB was observed, as one can see on figure 1.
This might also be explained by a penetration problem, and would indicate that the device was not homogeneously thinned. This last point is unclear and a die micro-section and a reverse engineering would be required for clarification.

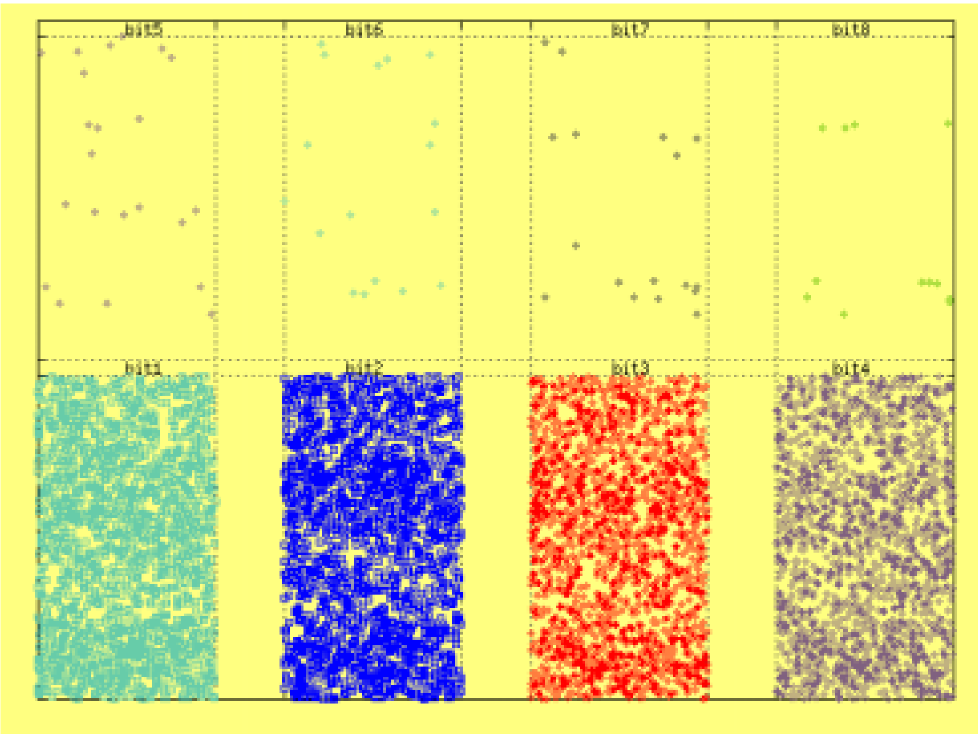

Figure 2 - Distributions of errors in (row, column) coordinates for each bit. In that case (run 92) all errors (each represented by a single symbol) are randomly distributed, but the 4 MSB appear to be much less sensitive to SEU..

Run #	Test mode	S/N	Ion	LET (MeV.cm²/mg)	Angle (°)	Eff LET (MeV.cm²/mg)	Time (s)	Fluence (/cm²)	Flux (/cm²/s)	SEU (words)	Bits up (0 to 1)	Bits down (1 to 0)	Total bits (up + down)	SEU cross-section per bit (/cm²)
38	S	2	Ar	14.10	0	14.10	299	215149	720	0	0	0	0	
39	D	2	Ar	14.10	0	14.10	296	249588	843	0	0	0	0	
89	S	2	Ne	5.85	0	5.85	193	301076	1560	6	3	4	7	1.19E-12
90	D	2	Ne	5.85	0	5.85	177	301221	1702	17	11	6	17	3.36E-12
91	S	2	B	1.70	0	1.70	57	304921	5349	7083	3543	3543	7086	1.38E-09
92	D	2	B	1.70	0	1.70	59	303116	5138	7136	3577	3559	7136	1.40E-09
93	S	2	B	1.70	45	2.40	108	504726	4673	458	211	247	458	5.41E-11

(*) S stands for STATIC TEST MODE; D for DYNAMIC TEST MODE

Table 3 - Heavy ion detailed results per run

8 CONCLUSION

Heavy ion tests were conducted on one commercial sample (thinned for back side irradiations) of TC55V8200FT memory from TOSHIBA, using the heavy ions available at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.

Since this device was tested from the back side using low penetration ions, nothing conclusively can be said. However a noticeable SEU sensitivity to low LET ions point in the direction of a fairly sensitive device type, which can only be confirmed during re-testing with higher penetration ions as available at the JYFL facility, Juvaskyla, Finland. These UCL tests confirm the demand for high penetration ions if back side irradiations have to be carried out.