SINGLE EVENT EFFECTS
RADIATION TEST REPORT

Part Type : TC55V8200FT

16 Mb SRAM

Manufacturer : TOSHIBA

Report Reference : ESA_QCA0217S_C-01

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Heavy ion SEE characterization of TC55V8200FT SRAM

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1 Abstract

Under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02 covering "Radiation Evaluation of COTS Semiconductor Components: “Radiation evaluation of parts for new VME design“, TC55V8200FT SRAM memories were radiation assessed.

Results from these assessments, primarily focusing on the sensitivity of these devices to Single Event Effects (SEE), are reported in this report.

2 INTRODUCTION

This report presents the results of a Single Event Effects (SEE) test program carried out on TC55V8200FT SRAMs, from TOSHIBA.
Test was conducted on commercial samples delivered by ESA.
These devices were used for heavy ion test at the JYFL RADEF facility, at Jyvaskyla, Finland.
The samples' back were mechanically thinned, and they were irradiated from the backside.
This work was performed for ESA/ESTEC under ESA Contract No 13528/99/NL/MV COO-13 dated 11/10/02.

3 REFERENCE DOCUMENTS

RD1. TC55V8200FT data sheet
RD2. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD3. Radiation Effect Facility (RADEF), JYFL, Jyvaslkyla, Finland

4 DEVICE INFORMATION

4.1 TC55V8200FT

Relevant device identification information is presented here after and photos of sample X-ray and die identification are shown in Figure 1.

Part type:	TC55V8200FT
Manufacturer:	TOSHIBA
Package:	54-TSOP
Quality Level:	Commercial
Date Code:	0229
Top Marking:	TOSHIBA YB7731 0229 KAD TC55V8200FT-12
Die Marking:	TC55V8200 TOSHIBA HW016A 822

2097152 word by 8 bit CMOS Static RAM, Silicon gate CMOS, 3V3, LVTTL compatible

4.2 Sample preparation

This device presents a Lead on Chip (LOC) construction as shown in Figure 1. It is therefore required to thin the samples for back side irradiation.

Two samples were prepared that way with a thickness target of 50 microns +/- 20 microns.

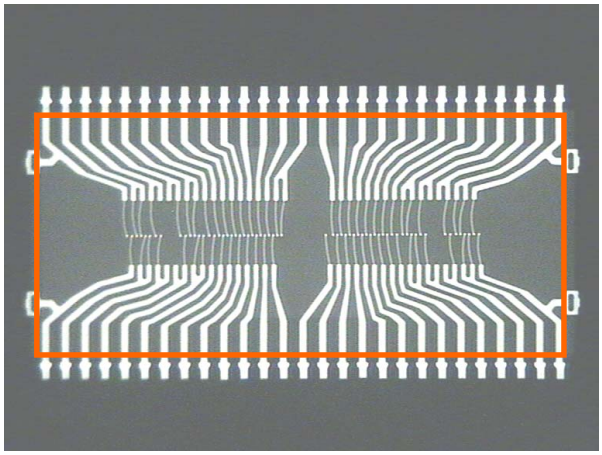

Photo 1 - Package X-ray

One can see the lead frame on the top of the die and the central wires bonding
(Lead On Chip construction)

Die perimeter:

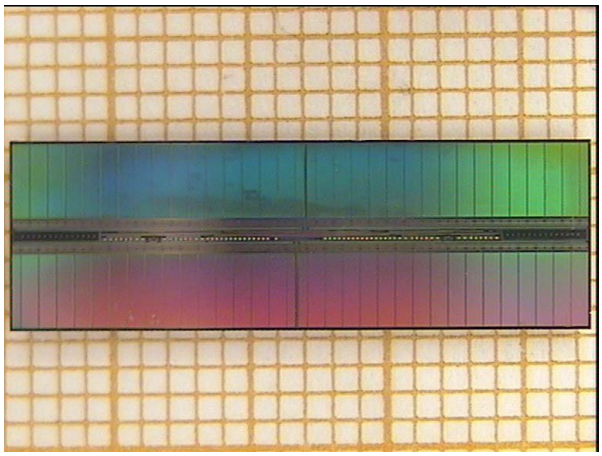

Photo 2 – Die full view

The presence of stripe-shaped blocks is noticeable on the die.

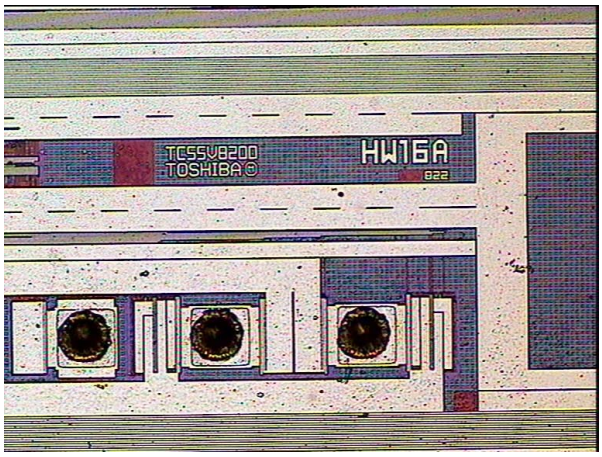

Photo 3 – Die marking

Figure 1 – TC55V8200FT photos

5 Test Definition

5.1 Test Set-up

Hirex test equipment is composed of a modular rack coupled with a generic memory test board:

This modular rack is derived from iTest BILT modular instrumentation system and presents 8 slots for modular instruments.
In addition to the existing power supply modules which cover the SEE test needs for precision measurements, remote control, LU detection, data storage, scope observation, etc, a specific modular board has been designed to provide:

- A high speed communication link with the test board under vacuum (up to 500 ko/s)
- Particle and test time counting

Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board includes programmable logic circuits with a total capacity of 30000 cells and 960 macrocells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Today, the board has a capacity of 80 pin-drivers using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

5.2 Test Configuration

Two basic configurations were used:

STATIC TEST MODE:

1. Device initialization
2. Write the test pattern in the memory and perform a read to check eventual stuck bits
3. Expose the device to the beam for a given time. At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Read the memory and count the errors
5. Loop with step 2, etc

DYNAMIC TEST MODE:

1. Device initialization
2. Write the test pattern in the memory and make a read to detect eventual stuck bits
3. Expose the device to the beam for a given time and perform continuous read-write operations. At each sequence, an offset is done on the test pattern and the number of errors is cumulated.
4. Loop with step 2, etc

The table here below provides, for each group of 4 bits, the 14 words repetitive pattern.

	It k	It k+1	It k+2	It k+3	It k+4	It k+5	It k+6	It k+7	It k+8	It k+9	It k+10	It k+11	It k+12	It k+13	It k+14
address n	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000
address n+1	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010
address n+2	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101
address n+3	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111
address n+4	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001
address n+5	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110
address n+6	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101
address n+7	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000
address n+8	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010
address n+9	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101
address n+10	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111
address n+11	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001
address n+12	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110
address n+13	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010
address n+14	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000

Table 1 – Test pattern

Errors which can be detected and counted are the following:

- Any single error in the memory block with identification of the transition (1->0 or 0->1)
- Any word with at least one bit flip with the identification of the word address

DUT power supply module is monitored and each time the current consumption exceeds a programmable threshold, a power reset cycle is done and latch-up error counter is incremented.

In addition the use of fast latch-up detection with a high speed comparator avoids the counting of SEU errors which could be induced by the latch-up condition.

DUT power supply is 3.3V.

6 JYFL TEST FACILITY

Test at the cyclotron accelerator was performed at University of Jyvaskyla (JYFL) (Finland) under HIREX Engineering responsibility.

The facility includes a special beam line dedicated to irradiation studies of semiconductor components and devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.
The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR's are especially valuable in the study of single event effects (SEE) in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula

$$130\ Q^2/M,$$

where Q is the ion charge state and M is the mass in Atomic Mass Units.

6.1 Test chamber

Irradiation of components is performed in a vacuum chamber with an inside diameter of 75 cm and a height of 81 cm.
The vacuum in the chamber is achieved after 15 minutes of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the X, Y and Z directions. The possibility of rotation around the Y-axis is provided by a round table. The free movement area reserved for the components is 25 cm x 25 cm, which allows one to perform several consecutive irradiations for several different components without breaking the vacuum.
The assembly is equipped with a standard mounting fixture. The adapters required to accommodate the special board configurations and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components.
A CCD camera with a magnifying telescope is located at the other end of the beam line to determine accurate positioning of the components. The coordinates are stored in the computer's memory allowing fast positioning of various targets during the test.

6.2 Beam quality control

For measuring beam uniformity at low intensity, a CsI(Tl) scintillator with a PIN-type photodiode readout is fixed in the mounting fixture. The uniformity is measured automatically before component irradiation and the results can be plotted immediately for more detailed analysis.
A set of four collimated PIN-CsI(Tl) detectors is located in front of the beam entrance. The detectors are operated with step motors and are located at 90 degrees with respect to each other. During the irradiation and uniformity scan they are set to the outer edge of the beam in order to monitor the stability of the homogeneity and flux.
Two beam wobblers and/or a 0.5 microns diffusion Gold foil can be used to achieve good beam homogeneity. The foil is placed 3 m in front of the chamber. The wobbler-coils vibrate the beam horizontally and vertically, the proper sweeping area being attained with the adjustable coil-currents.

6.3 Dosimetry

The flux and intensity dosimeter system contains a Faraday cup, several collimators, a scintillation counter and four PIN-CsI(Tl) detectors. Three collimators of different size and shape are placed 25 cm in front of the device under test. They can be used to limit the beam to the active area to be studied.
At low fluxes a plastic scintillator with a photomultiplier tube is used as an absolute particle counter. It is located behind the vacuum chamber and is used before the irradiation to normalize the count rates of the four PIN-CsI(Tl) detectors.

6.4 Used Ions

	Q+	Z	A	Energy (MeV)	LET (MeV.cm²/mg)	Range (µ)
Si	8	14	30	280	7	133
N	4	7	15	138	2	205

Table 2 - Used ions and features thereof

7 RESULTS

The detailed results per run are presented in Table 3.

The corresponding SEU cross-section per bit vs. Effective LET is plotted on Figure 2.

It is important to note that, although in the case of some runs the SEU were randomly and uniformly distributed in the whole memory as one can see on figure 3, in most cases, the distribution of errors wasn't homogeneous. Globally, a significant discrepancy was observed between the number of SEU that occurred in the 4 MSB and the 4 LSB. Indeed, it seems that at low LET, the 4 LSB are more sensitive than the 4 MSB, and the other way around at higher LET, as can be seen in table 3. An example of MSB/LSB discrepancy is represented on figure 4.

Moreover, when tilting, at low LET as well as high ones, stripe-shaped areas that seem less sensitive to SEU appear, as shown on figure 5. It seems reasonable to exclude penetration problems as a possible explanation for this phenomenon, since the ions used for these runs feature very high ranges in Si (as one can see on table 2). No definite explanation for this observation can be given at the time being, although it can possibly be related to the stripe-shaped blocks noticeable on the die (Figure 1). Reverse engineering on the parts would be useful to understand this phenomenon precisely.

More important is the fact that the occurrences of these stripe-shaped regions for tilted runs correspond to a significant drop of the SEU cross-section, as one can see on Table 3 and Figure 2.

Finally, but most important of all, SEL occurred at LET as low as 8 MeV.cm²/mg.

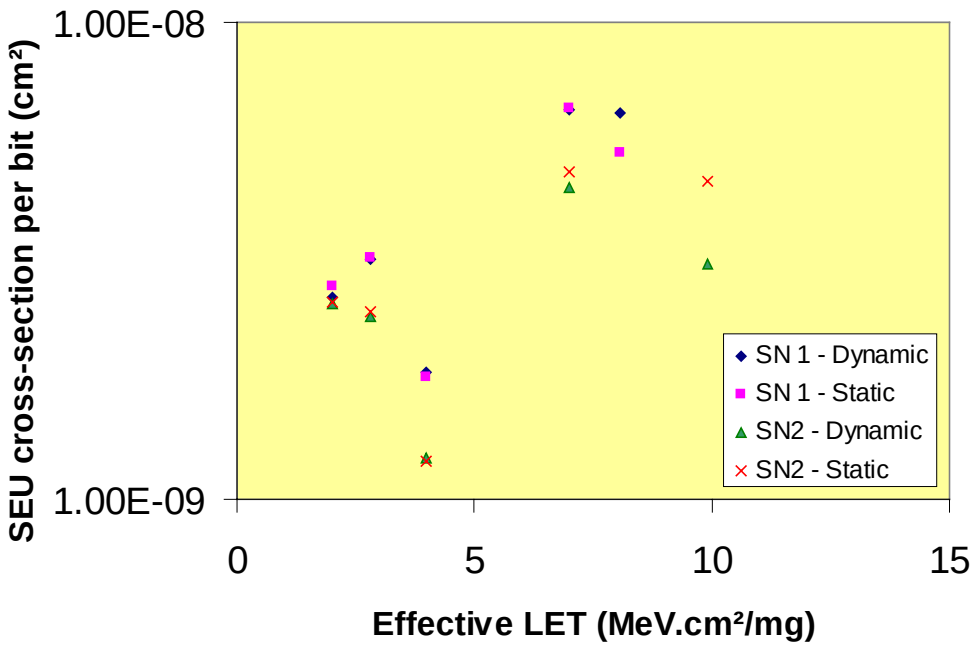

Figure 2 - SEU cross-section per bit vs. Effective LET

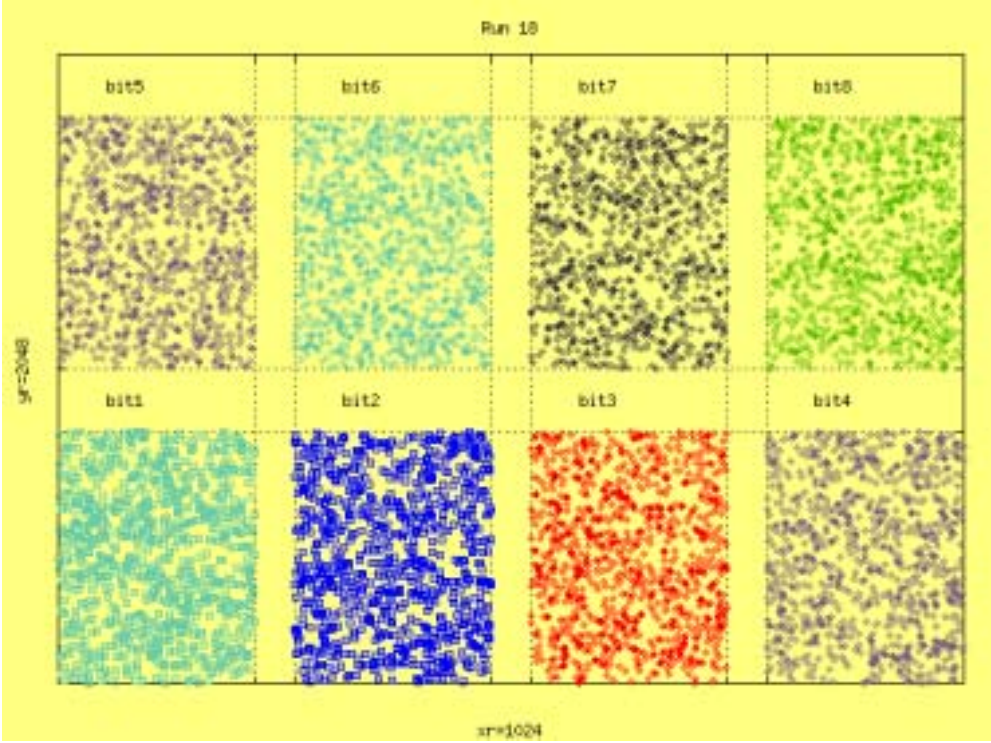

Figure 3 - Distributions of errors in (row, column) coordinates for each bit. In this case, all SEU are randomly distributed in the memory, and about the same number of SEU occured for each bit.

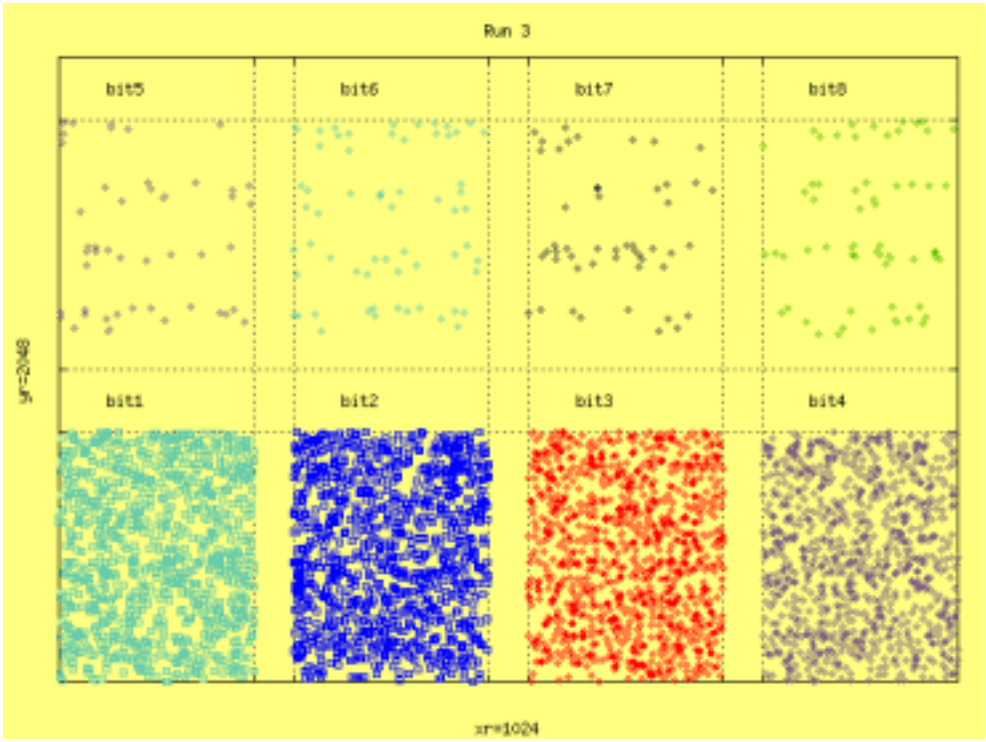

Figure 4 - Distributions of errors in (row, column) coordinates for each bit. In this case, all errors (each represented by a single symbol) are randomly distributed, but the 4 MSB appear to be much less sensitive to SEU.

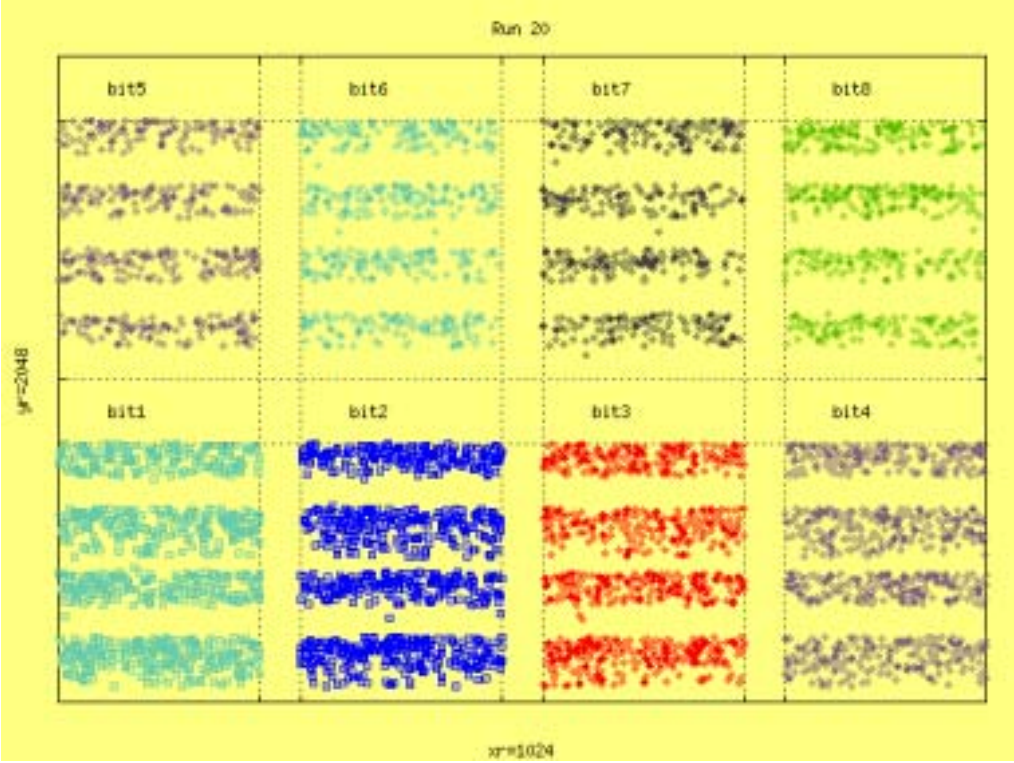

Figure 5 - Distributions of errors in (row, column) coordinates for each bit. In this case, stripe-shaped areas of the memory seam less sensitive to SEU than the rest of it.

Run	S/N	Test Condition	Ion	LET (MeV.cm²/mg)	Angle (°)	Eff. LET (MeV.cm²/mg)	JYFL Time (s)	Bilt Time (s)	Fluence (/cm²)	Eff. Fluence (/cm²)	Flux (/cm²/s)	SEU Words	SEL	0 to 1 transitions	1 to 0 transitions	0 to 1 + 1 to 0	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	SEU cross-section per bit (cm²)
10	1	D	N	2	0	2	196	203	1.65E+05	1.71E+05	842	7585	0	3832	3754	7586	550	546	553	527	1356	1313	1346	1395	2.65E-09
12	1	D	N	2	45	3	211	218	1.39E+05	1.44E+05	659	7675	0	3762	3914	7676	709	720	811	722	1179	1209	1126	1200	3.19E-09
14	1	D	N	2	60	4	258	258	1.36E+05	1.36E+05	527	4218	0	2116	2124	4240	302	286	297	276	783	757	790	749	1.85E-09
6	1	D	Si	7	0	7	130	130	7.22E+04	7.22E+04	555	7943	0	3934	4009	7943	1104	1137	1023	1156	855	928	849	891	6.56E-09
8	1	D	Si	7	30	8	172	163	8.24E+04	7.81E+04	479	8441	3	4218	4304	8522	1286	1333	1308	1321	829	840	847	757	6.44E-09
9	1	S	N	2	0	2	205	202	1.80E+05	1.77E+05	878	8325	0	4119	4239	8358	628	588	572	599	1506	1519	1491	1456	2.80E-09
11	1	S	N	2	45	3	261	263	1.58E+05	1.59E+05	605	8590	0	4366	4241	8607	833	791	807	847	1335	1364	1284	1346	3.22E-09
13	1	S	N	2	60	4	266	269	1.29E+05	1.30E+05	485	3964	0	1984	1997	3981	267	303	295	294	660	739	690	733	1.81E-09
5	1	S	Si	7	0	7	130	134	7.11E+04	7.33E+04	547	8120	0	4107	4015	8122	1195	1129	1109	1091	929	888	875	906	6.60E-09
7	1	S	Si	7	30	8	176	155	9.64E+04	8.49E+04	548	7574	3	3762	3815	7577	1180	1180	1116	1138	730	718	770	745	5.32E-09
16	2	D	N	2	0	2	95	117	1.44E+05	1.77E+05	1516	7630	0	3817	3813	7630	655	700	703	655	1324	1187	1199	1207	2.56E-09
18	2	D	N	2	45	3	165	173	1.78E+05	1.87E+05	1079	7556	0	3775	3783	7558	946	885	990	938	939	994	914	952	2.41E-09
20	2	D	N	2	60	4	286	293	2.56E+05	2.62E+05	895	5376	0	2726	2668	5394	830	872	883	812	510	506	490	491	1.22E-09
2	2	D	Si	7	0	7	165	165	1.12E+05	1.12E+05	679	8470	0	4235	4285	8520	1529	1504	1493	1465	670	622	615	622	4.51E-09
4	2	D	Si	7	45	10	90	61	4.77E+04	3.23E+04	530	1683	3	838	850	1688	420	413	400	370	19	28	19	19	3.11E-09
15	2	S	N	2	0	2	134	136	1.73E+05	1.76E+05	1291	7609	0	3852	3758	7610	663	645	641	656	1270	1299	1233	1203	2.58E-09
17	2	S	N	2	45	3	165	166	1.70E+05	1.71E+05	1030	7102	0	3500	3604	7104	839	875	925	924	887	901	867	886	2.48E-09
19	2	S	N	2	60	4	351	355	2.81E+05	2.84E+05	801	5741	0	2870	2891	5761	925	895	869	880	517	551	542	582	1.20E-09
1	2	S	Si	7	0	7	158	158	9.35E+04	9.35E+04	592	7644	0	3851	3810	7661	1332	1374	1355	1372	534	542	563	589	4.87E-09
3	2	S	Si	7	45	10	178	132	7.22E+04	5.35E+04	406	4155	7	2061	2117	4178	946	1041	1014	955	48	62	50	62	4.63E-09

(*) S stands for STATIC TEST MODE; D for DYNAMIC TEST MODE

Table 3 - Heavy ion detailed results per run

8 CONCLUSION

Heavy ion tests were conducted on two commercial samples (thinned for back side irradiations) of TC55V8200FT memory from TOSHIBA, using the heavy ions available at RADEF facility at JYFL, Jyvaskyla, Finland.

Numerous SEU were observed on the device for LET as low as 2 MeV.cm²/mg. SEL were observed at LET as low as 8 MeV.cm²/mg.