SINGLE EVENT EFFECTS
RADIATION TEST REPORT

Part Type : IRFY140

100V N-Channel Power MOSFET Transistor

Manufacturer : International Rectifier

Report Reference : ESA_QCA0402S_C

Issue : 01

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Heavy ion SEE characterization of IRFY140 100V N-Channel Power MOSFET Transistor

TABLE OF CONTENTS

1 ABSTRACT **3**
2 INTRODUCTION **4**
3 REFERENCE DOCUMENTS **4**
4 DEVICE INFORMATION **4**
4.1 IRFY140 4
4.2 SAMPLE PREPARATION 4
5 TEST DEFINITION **6**
5.1 TEST SET-UP 6
5.1.1 Single Event burnout (SEB) 6
5.1.2 Single Event Gate Rupture (SEGR) 7
5.2 TEST CONDITIONS 7
6 BNL TEST FACILITY **8**
6.1 DOSIMETRY 8
6.2 USED IONS 8
6.3 BEAM SET-UP 8
7 RESULTS **8**
8 CONCLUSION **10**

List of Tables:

Table 1 – BNL ions selection 8
Table 2 - Heavy ion detailed results per run 9

List of Figures:

Figure 1 – IRFY140 photos 5
Figure 2 – Test set-up, motherboard 6
Figure 3 – Equivalent circuit for SEB including the parasitic capacitor of the MOSFET. 7

1 Abstract

Under ESA Contract No 13528/99/NL/MV COO-16 dated 05/01/04 covering "Radiation Evaluation of COTS Semiconductor Components: "Radiation evaluation of parts for the ATV project', IRFY140 100V N-Channel Power MOSFET Transistor, was radiation assessed.

Heavy ion radiation results, focusing on Single Event Effects (SEE), are reported in this report.

2 INTRODUCTION

This report presents the results of a Single Event Effects (SEE) test program carried out on IRFY140 100V N-Channel Power MOSFET Transistor, from International Rectifier.
Test was conducted on Hi-Rel samples delivered by ESA.
These devices were used for heavy ion test at the Brookhaven National LaboratoryJ (BNL) facility, at Long Island, New York, USA – January 17/18, 2004.
This work was performed for ESA/ESTEC under ESA Contract No 13528/99/NL/MV COO-16 dated 05/01/04.

3 REFERENCE DOCUMENTS

RD1. IRFY140 data sheet
RD2. ATV/MMS/PR/FX/329.03 EADS fax dated 30/07/03
RD3. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD4. Brookhaven National Laboratory, SEU Test Facility, User Guide, revised January, 1997

4 DEVICE INFORMATION

4.1 IRFY140

IRFY140 is a 100V N-Channel MOSFET Transistor.

Relevant device identification information is presented here after and photos of sample die identification are shown in Figure 1.

Part type:	IRFY140
Manufacturer:	International Rectifier
Package:	TO-257A
Quality Level:	Hi-Rel
Date Code:	9730
Top Marking:	IR BeO 94-569 MA5000AKG01S
S/Ns	3, 5, 16, 142

4.2 Sample preparation

The 4 samples delivered were delidded mechanically.

Photo 1 – Top marking

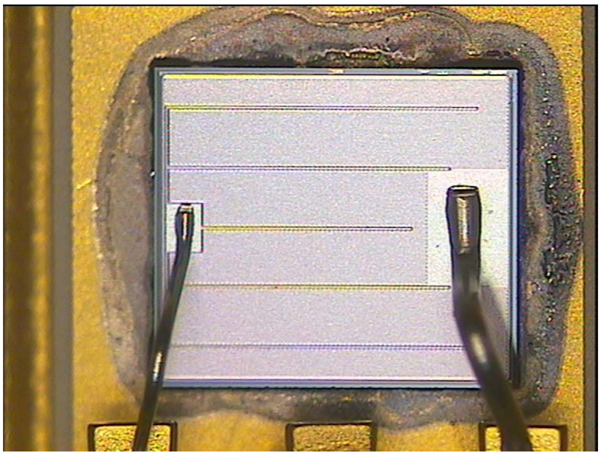

Photo 2 – Die full view

Die dimensions:
4.3mm x 4.8 mm

Figure 1 – IRFY140 photos

5 Test Definition

5.1 Test Set-up

The motherboard test set-up (see Figure 2) can accept up to 5 transistors, each DUT being mounted on a specific Device Interface Board (to fit with the DUT package).
To prevent the destructive burnout of the DUT when the parasitic Bipolar Junction Transistor (BJT) is triggered on by a strike, each DUT drain is biased with a capacitor and a limiting current resistor. This is to limit the amount of energy available as well as the maximum transient current value.

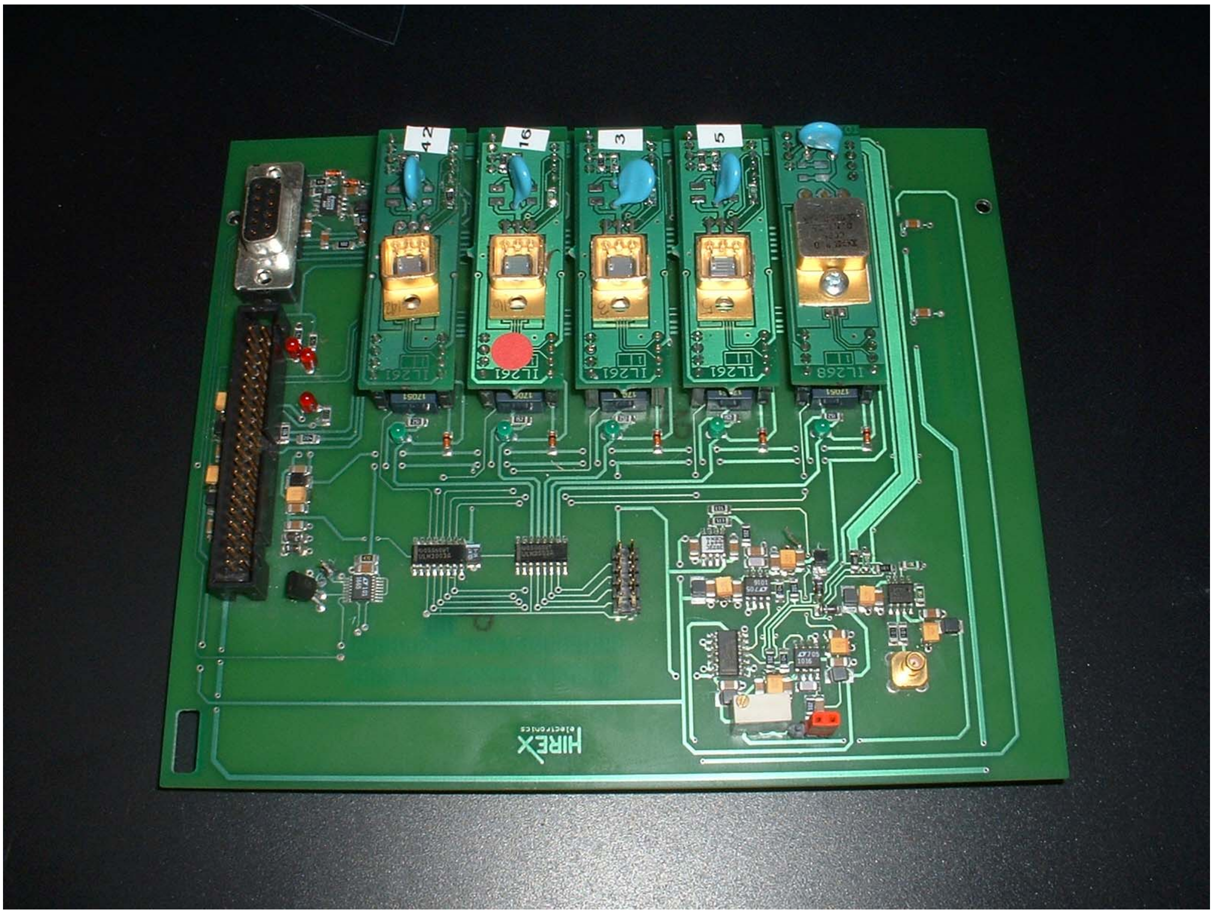

Figure 2 – Test set-up, motherboard

Test set-up which has been used for the present test report, allows for the detection of both Single Event Burn-out (SEB) and Single Event Gate Rupture (SEGR) effects

5.1.1 Single Event burnout (SEB)

SEB can be observed with the MOSFET in the off mode.
To get non-destructive SEBs, selected test principle was to limit as much as possible the energy which could flow into the DUT when the parasitic bipolar transistor enters second breakdown.
To achieve this goal, a resistor Rload (2k42 ohms) in series with the DUT drain limits the current, which can flow from the bias circuit (capacitor of 10nF). In that case the only available energy which can flow into the DUT without any external current limitation is the one stored into the output DUT capacitance C_{DS}.
The equivalent circuit when an SEB is triggered is shown in Figure 3.
Observation of VDS transients is done at Rshunt which form a resistor divider with Rload.

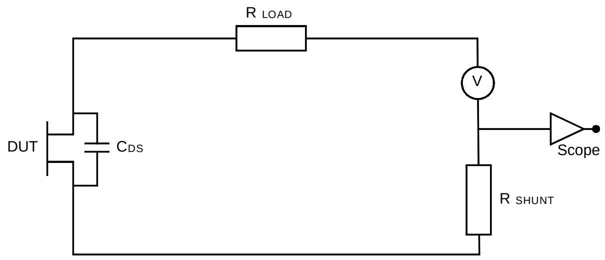

Figure 3 – Equivalent circuit for SEB including the parasitic capacitor of the MOSFET.

Events are counted thanks to a programmable threshold comparator of 50MHz bandwidth. Moreover the monitoring of changes in the leakage dc current Idss will allow to check for eventual permanent degradation.

5.1.2 Single Event Gate Rupture (SEGR)

SEGR is a destructive effect, which can be observed with the MOSFET in the off mode. Monitoring of the IGSS current allows for the detection of a SEGR which corresponds to a permanent degradation of the gate current.
This requires the measurement of µamp current amplitude under high impedance. Test board design is compatible with the accelerator environment by the use of a complete guard ring.

To check the DUT gate integrity after each run, DUT is operated under nominal conditions (VDS = 100V).

5.2 Test Conditions

(in accordance with RD2)

VDS ≥30V
VGS=-4V

6 BNL TEST FACILITY

Test at the Tandem Van de Graaff accelerator was performed at Brookhaven National Lab, Upton, New York (USA) under HIREX Engineering responsibility.

RD4 document provides a description of this facility.

6.1 Dosimetry

The current BNL Tandem dosimetry system and procedures were used.

6.2 Used ions

Ion	**Energy** MeV	**LET(Si)** Mev/(mg/cm²)	**Range (Si)** µm
Br-81	279	37.45	36.09

Table 1 – BNL ions selection

6.3 Beam set-up

For each run, the following information is given in the detailed results tables provided in the next paragraph (paragraph 7):

- Run Number
- Date/Time
- Device ID
- Ion type
- Energy
- Range
- LET
- Tilt angle and Roll
- Test Duration
- Averaged flux
- Fluence
- Equivalent dose per run and per sample
- SET
- Cross-section

7 RESULTS

Each run was performed at room temperature and under normal beam incidence, which corresponds to the worst case conditions.

The detailed results per run are presented in Table 2.

For both s/n 3 and s/n5, neither SEB nor SEGR were detected during testing to a fluences of 5.0E+6 ions/cm^2 under the project required test conditions with V_{DS} =30V and V_{GS}= -4V.

Additional testing, again for both devices and to the same fluence, but now with **V_{DS} =50V** and V_{GS}= -4V, had both devices passing without any SEB/SEGR.

The 2 DUTs were fully functional under nominal conditions at the end of the runs.

Run #	Date/Time	DeviceID	Ion	Energy MeV	Range um	LET(Si) MeV.cm2/mg	Tilt deg	Roll deg	Time sec	Flux #/cm2/sec	Fluence #/cm2	Dose RAD(Si)	TotalDose RAD(Si)	Events SEB	Events SEGR	Test Cond Vds (V)	Test Cond Vgs (V)
1	18/1/04 12:22	5	Br-81	279	36.09	37.45	0	0	580.8	9.16E+03	5.32E+06	3.01E+03	3.01E+03	0	0	30	-4
2	18/1/04 12:36	3	Br-81	279	36.09	37.45	0	0	578.4	8.65E+03	5.00E+06	3.01E+03	3.01E+03	0	0	30	-4
3	18/1/04 12:50	3	Br-81	279	36.09	37.45	0	0	586	8.54E+03	5.00E+06	3.01E+03	6.03E+03	0	0	40	-4
4	18/1/04 13:08	3	Br-81	279	36.09	37.45	0	0	443	1.18E+04	5.23E+06	3.01E+03	9.04E+03	0	0	**50**	-4
5	18/1/04 13:23	5	Br-81	279	36.09	37.45	0	0	406	1.23E+04	5.00E+06	3.02E+03	6.03E+03	0	0	50	-4

Table 2 - Heavy ion detailed results per run

8 CONCLUSION

Heavy ion tests were conducted on two Hi-Rel samples of IRFY140 N-Channel Power MOSFET transistor from International Rectifier, using the heavy ions available at the Tandem accelerator facility at BNL, Long Island, New York, USA.

Testing was carried out with Br-ions having a LET of 37.5 MeV/(mg/cm²). For the two devices tested, neither SEB nor SEGR were detected during testing to a fluence of 5.0E+6 ions/cm^2 under the project required test conditions with V_{DS} =30V and V_{GS}= -4V.

Additional testing at the same LET and on the same devices but now with **V_{DS} =50V** and V_{GS}= -4V, had both devices passing a fluence of 5.0E+6 ions/cm^2 without any SEB or SEGR.