Influence of the Tilt Parameter During SEE Characterization with Heavy Ion Beams

ESTEC contract number 13451/NL/MV, CCN-3, COO-4

Guy Berger

Outline

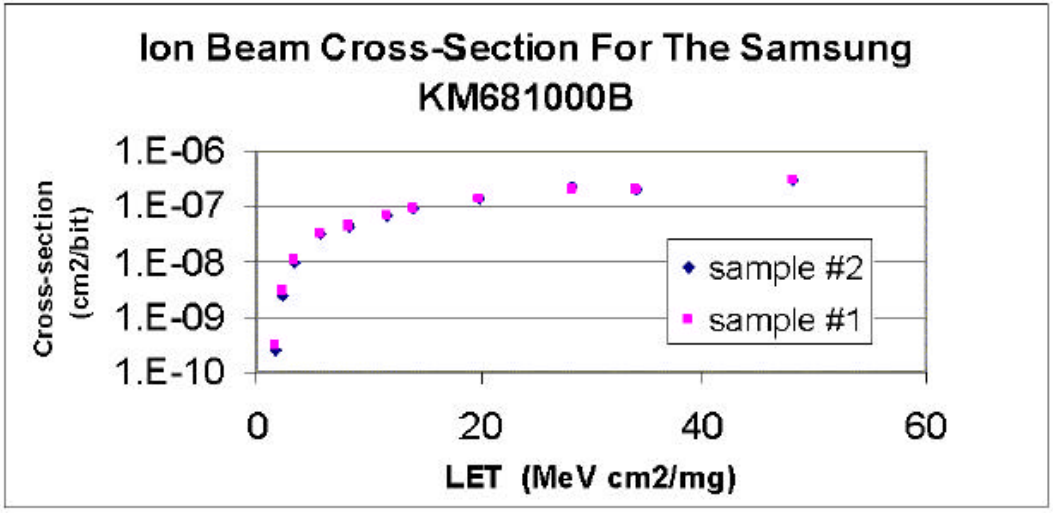
- ✓ Motivations.
- ✓ Test Structures Definition.
- ✓ Test Structure Simulations.
- ✓ Experimental Measurements.
- ✓ Complete Structure Simulations.
- ✓ Conclusions.

Motivations

Q_{dep} Variations ? Ion changing

? Beam to die angle variations

$LET_{eff} = LET / \cos(a)$



B Ae Dynamics (ESA contract)

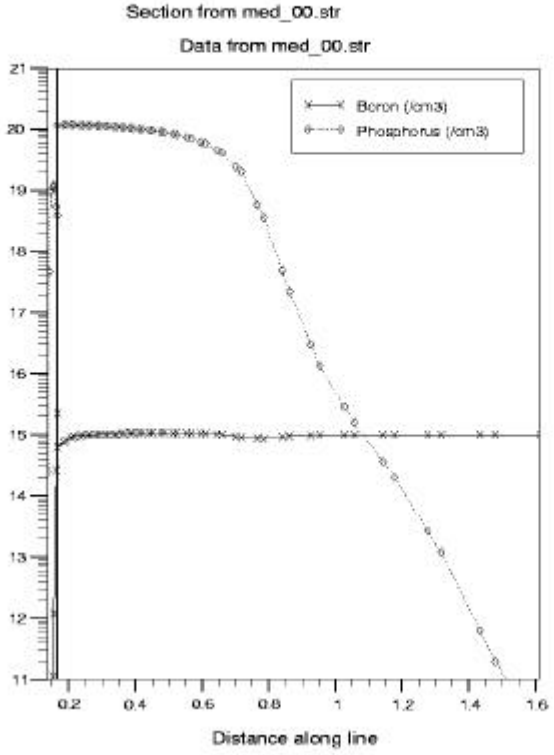
Test Structures Selection

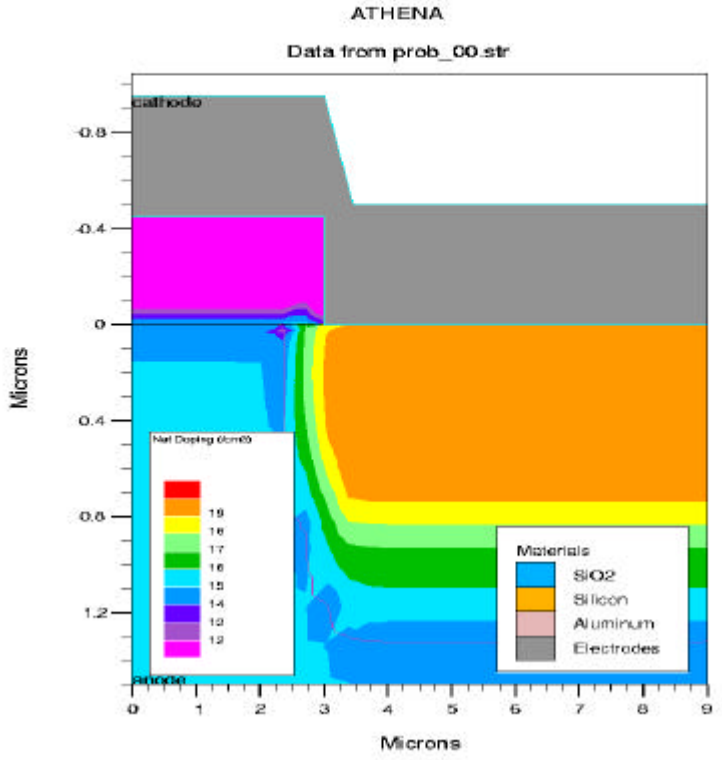
Wet oxide growth (4500 Å)

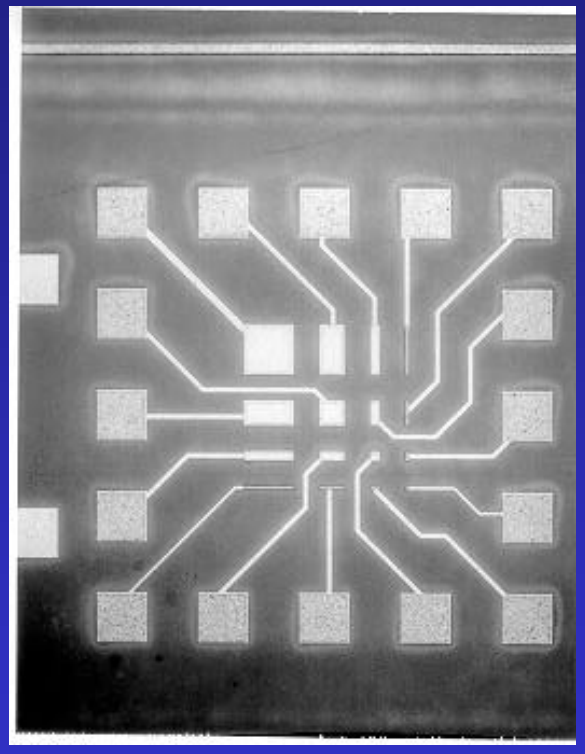
Open windows - Implant N+

Open windows for contacts to implanted zones
Aluminium deposition.

Aluminium etch for interconnect definitions
Oxide deposition for passivation
Open PAD contacts and back contact metallization.


Section from med_00.str
Data from med_00.str
Boron (/cm3)
Phosphorus (/cm3)
Distance along line

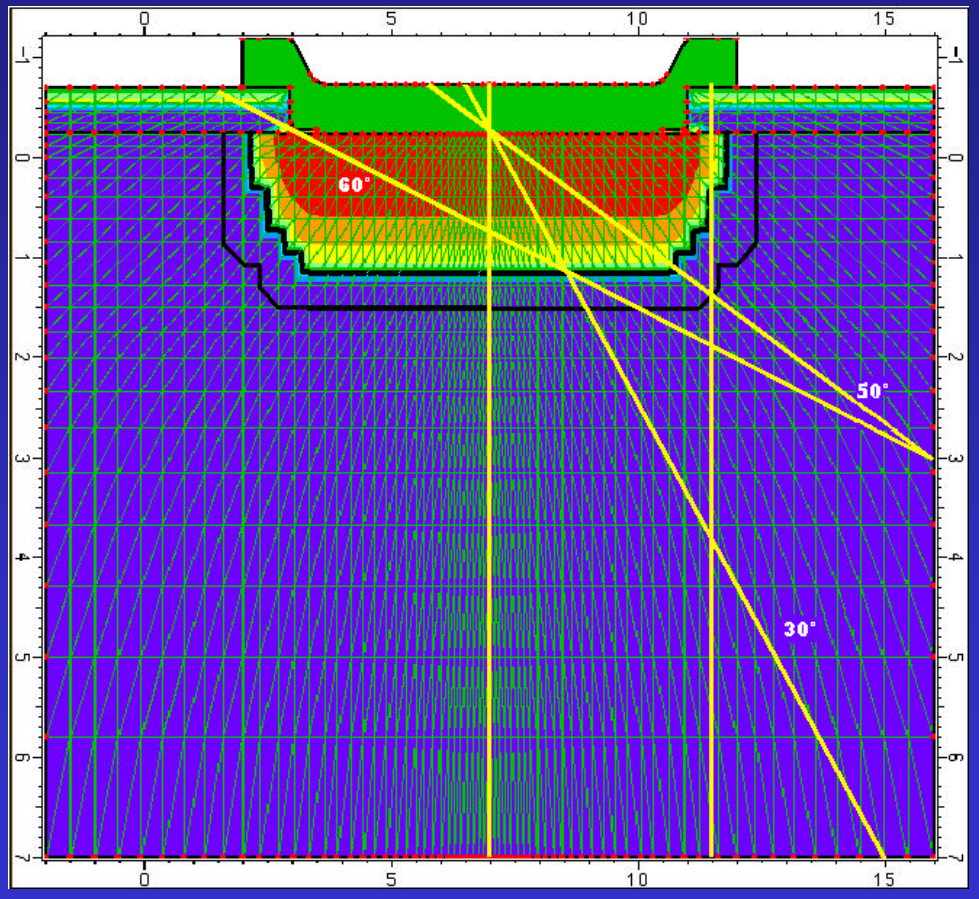

ATHENA
Data from prob_00.str
cathode
anode
Net Doping (/cm3)
Materials
SiO2
Silicon
Aluminum
Electrodes
Microns
Microns



Energy [keV]	Junction Depth [µm]
20	0.75
100	1.1

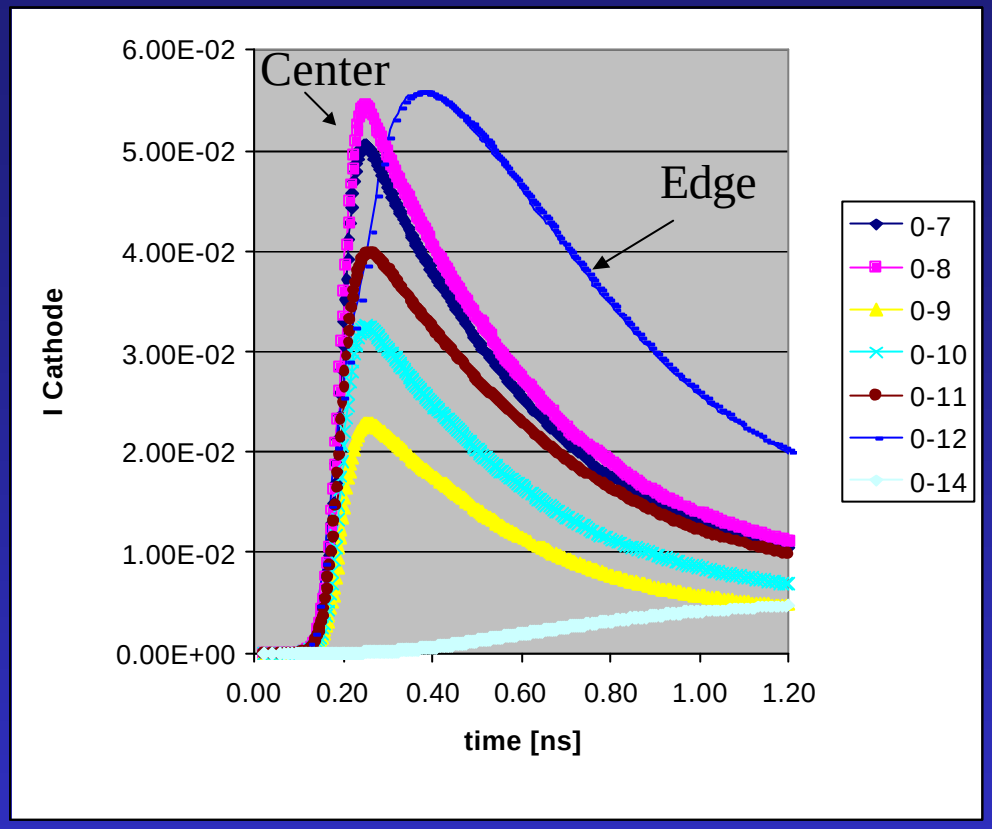
Test Structures Simulations

Structure meshing in ATLAS

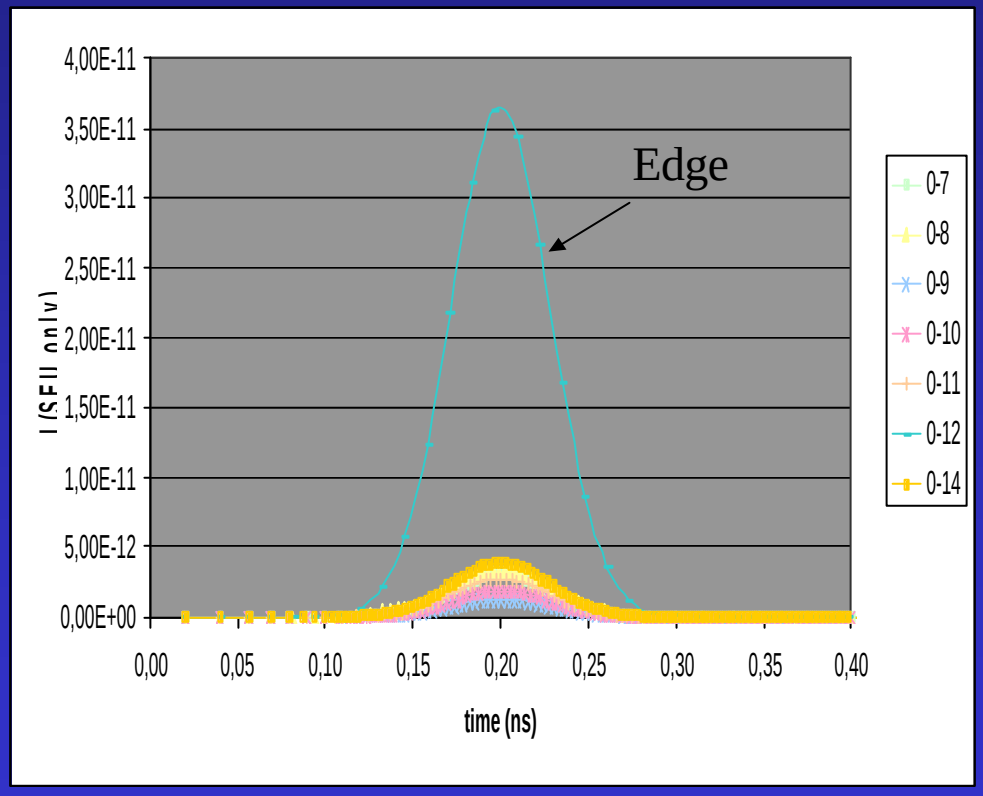


Simulations: Xe 459 MeV

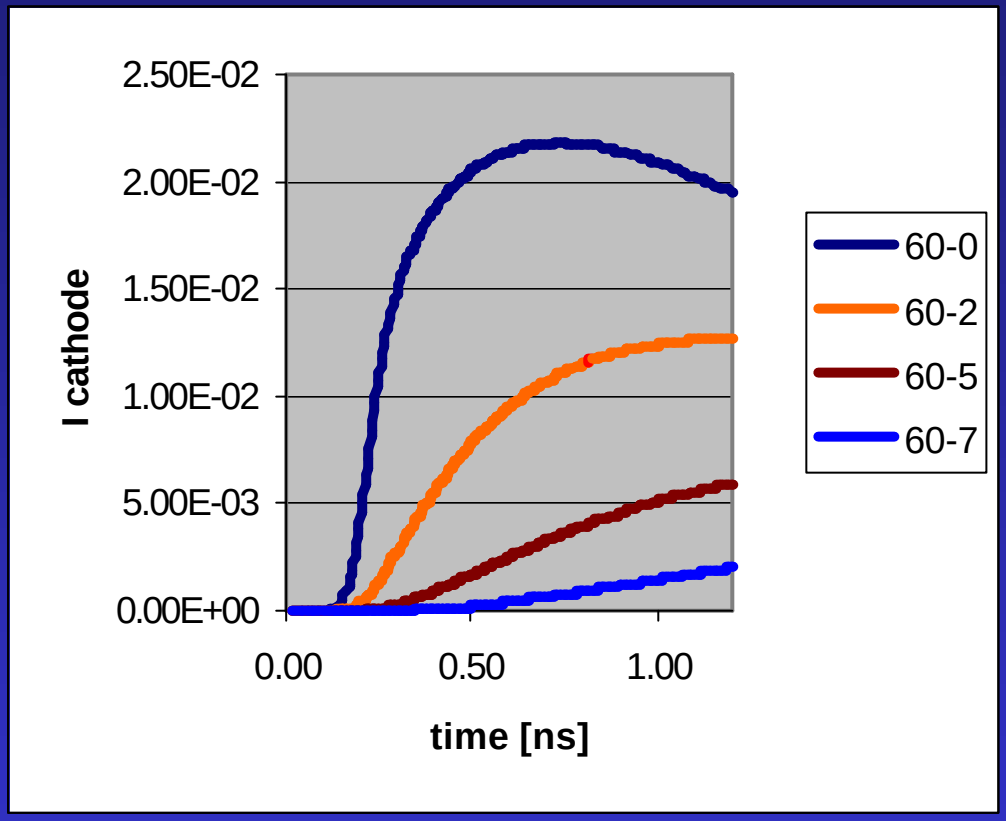
0 ° Irradiation



Total current

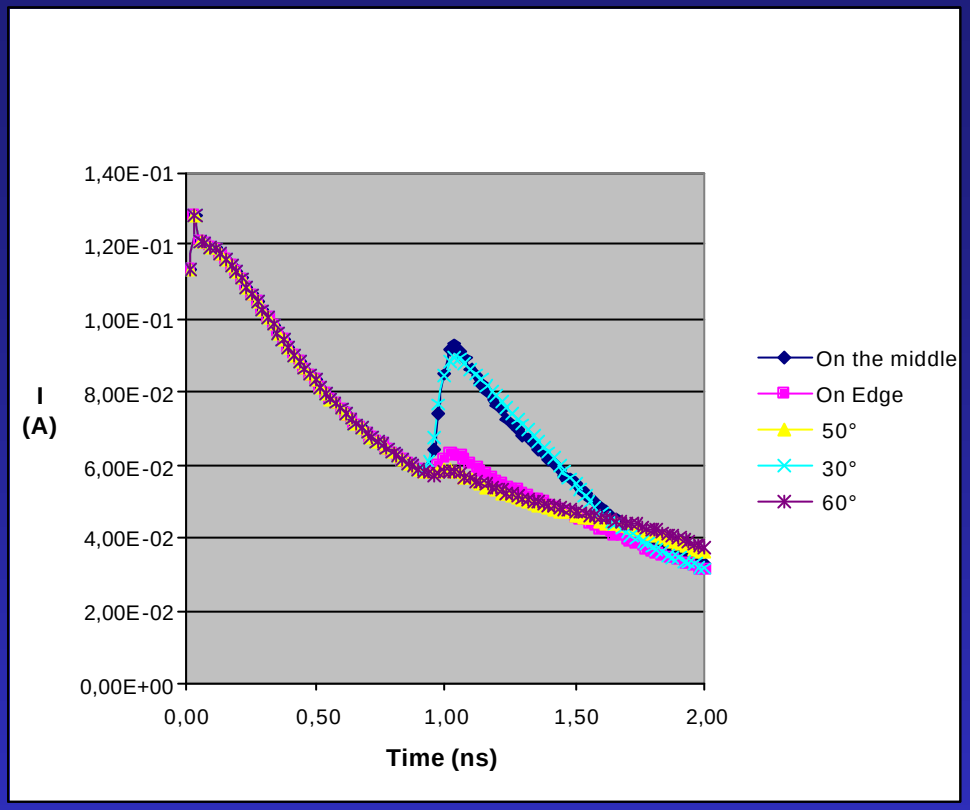


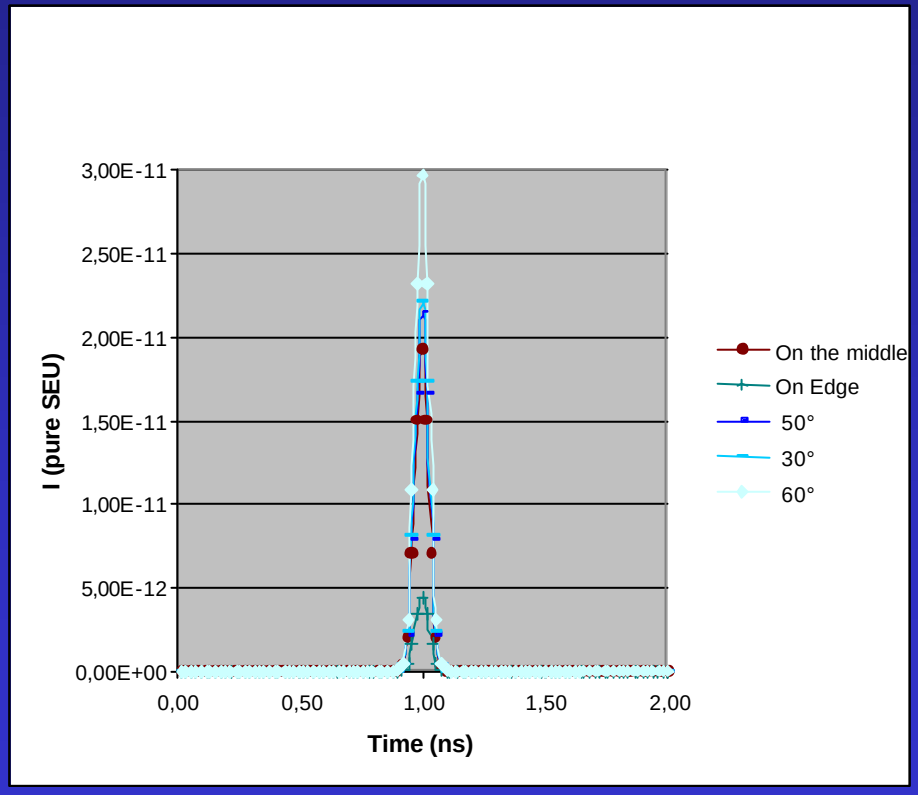
Photocurrent



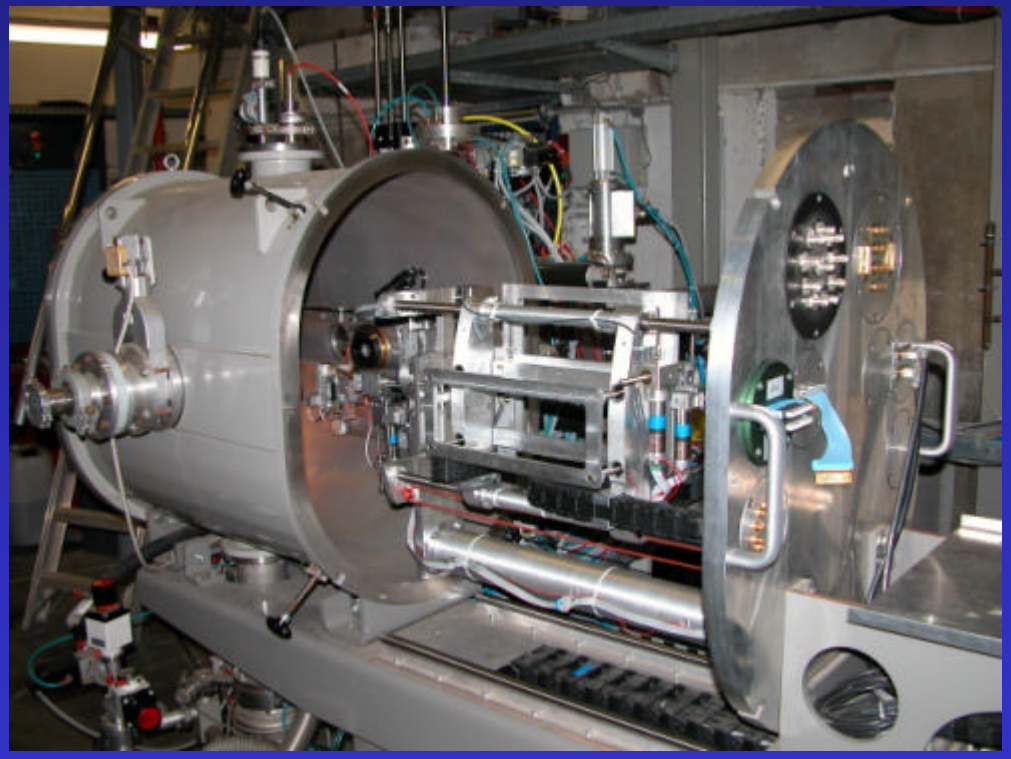
60 ° Irradiation

30° and 50° entry points in center
60° strike on the left of structure





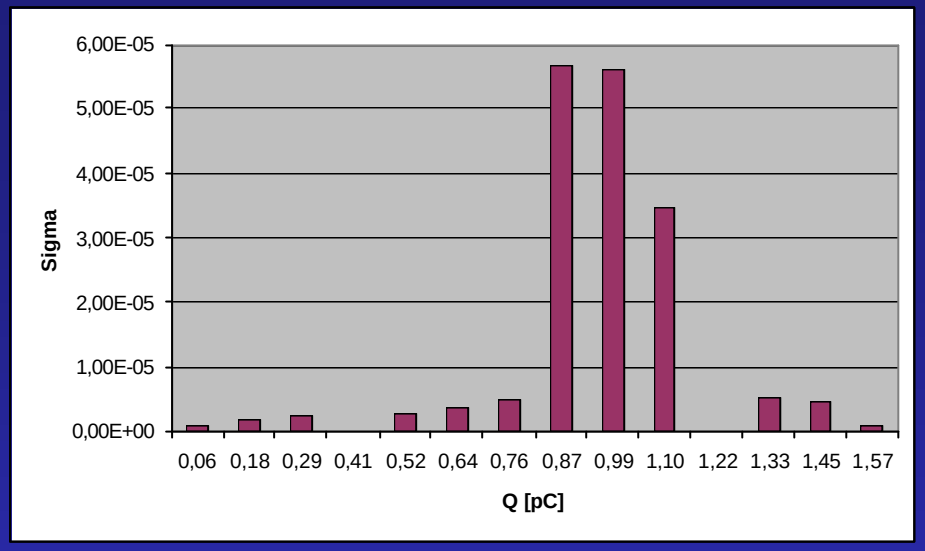
Test Structures Irradiations



^{132} Xe $^{26+}$ at 459 MeV

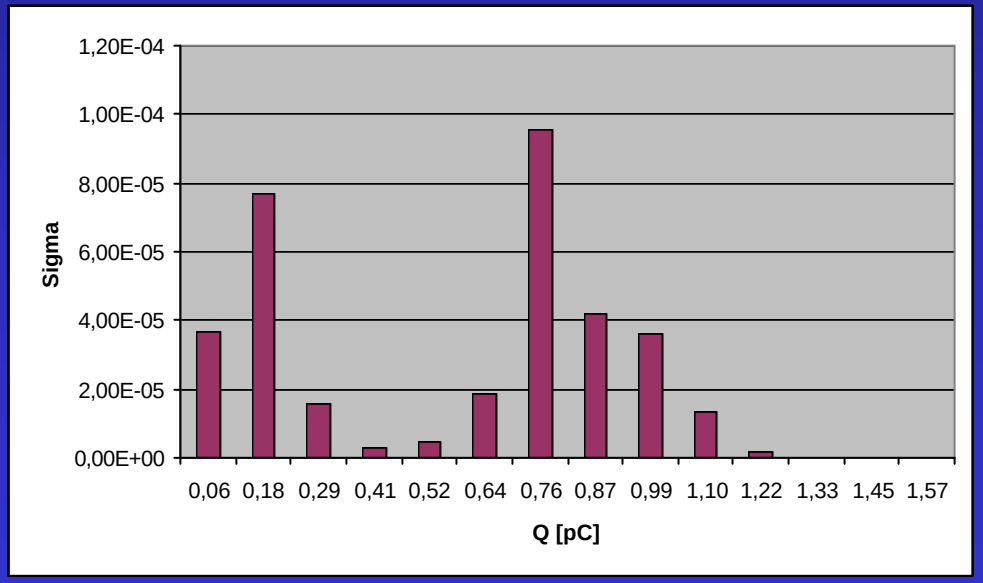
Range = 43 µm Si

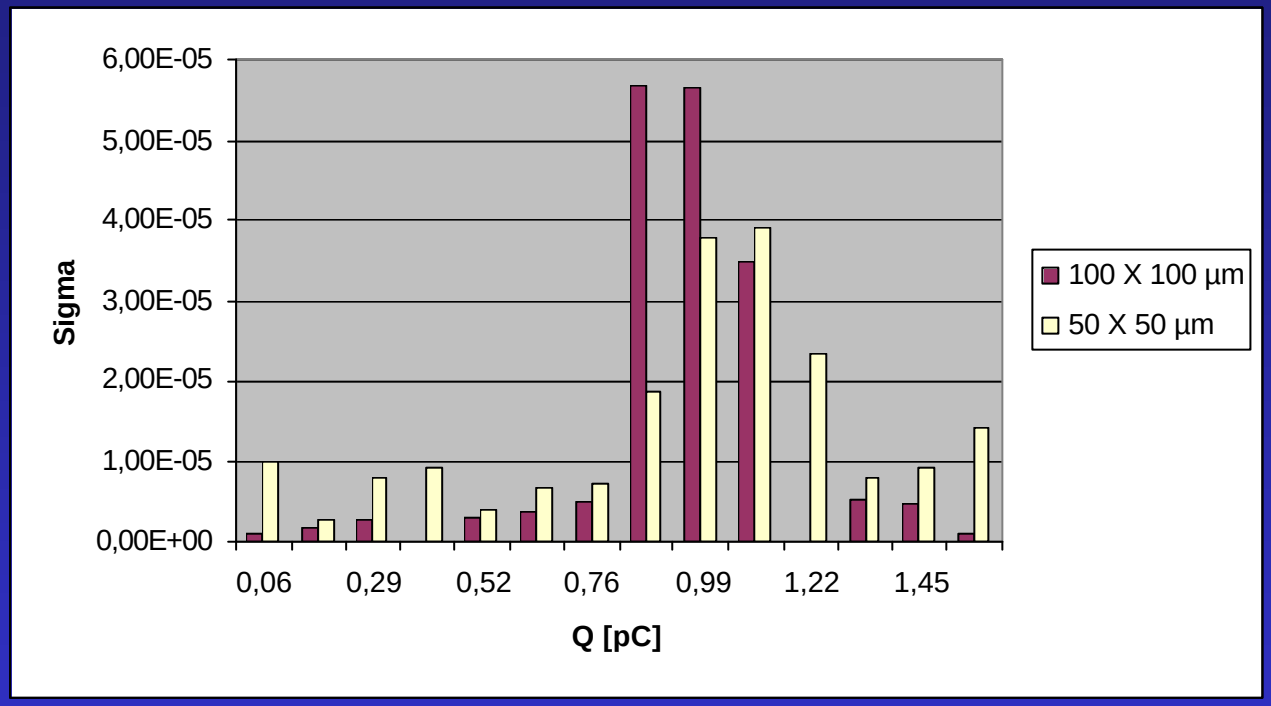
LET_{Si} = 55.9 MeV/mg/cm²



0 ° Irradiation

60 ° Irradiation





Perim – area Ratio:

100 µm: 4e-2 μm^{-1}

50 µm: 8e-2 μm^{-1}

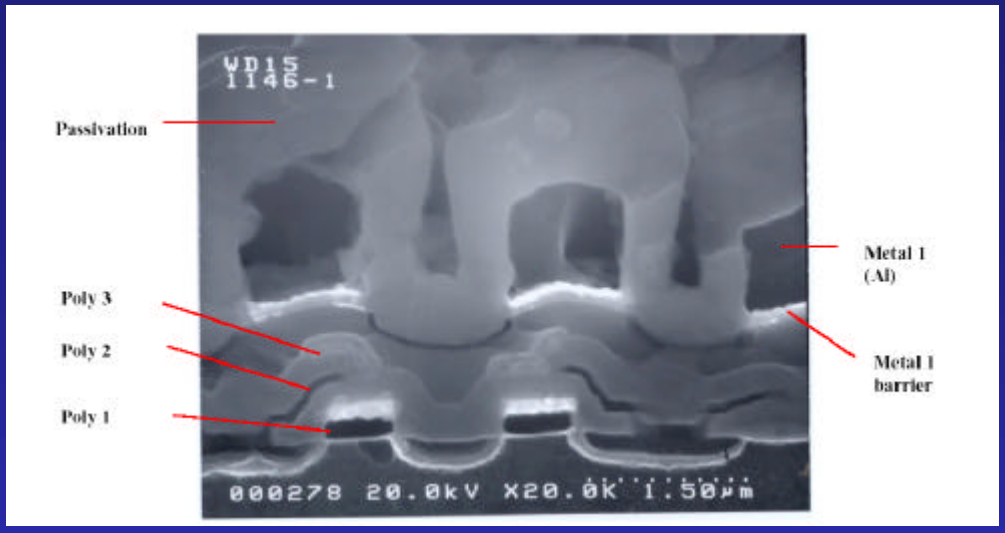
Structure Selection

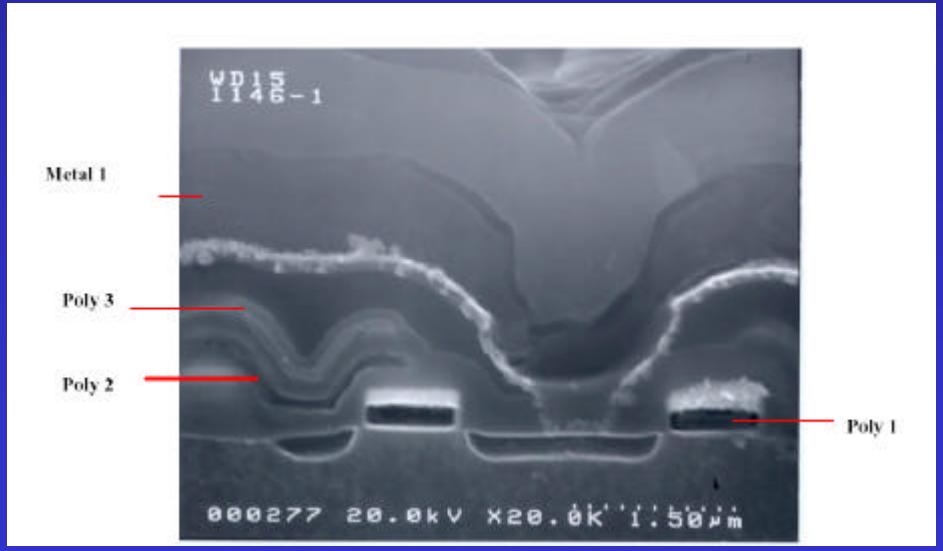
M5M51008 1MB SRAM

AVP process can be summarized as follow:
(Ref. NMRC - Construction Analysis DTE1146 part 1)

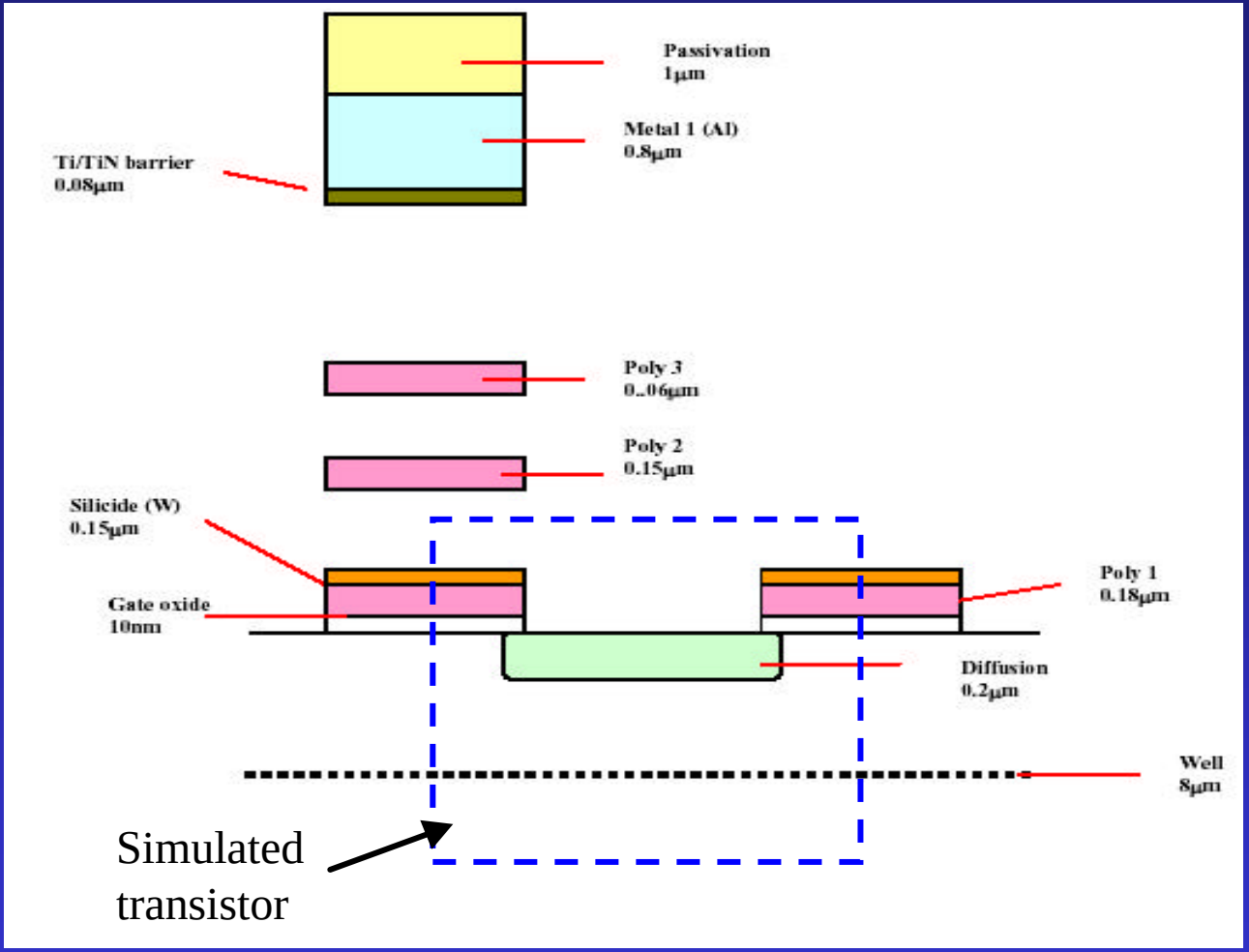
- 0.8 µm polysilicon gate CMOS process.
- No epitaxial layer.
- One level of metallisation.
- METAL 1 is composed of Al with a Ti/TiN barrier layer.
- High resistance SRAM cell.
- Three levels of polysilicon:
  - Poly 3 is a thin lightly-doped layer which forms the cell resistors.
  - Poly 2 is a normally doped layer which forms the cell ground plane.
  - Poly 1 is a W silicided layer which forms the cell word lines.

Transistor cross sections





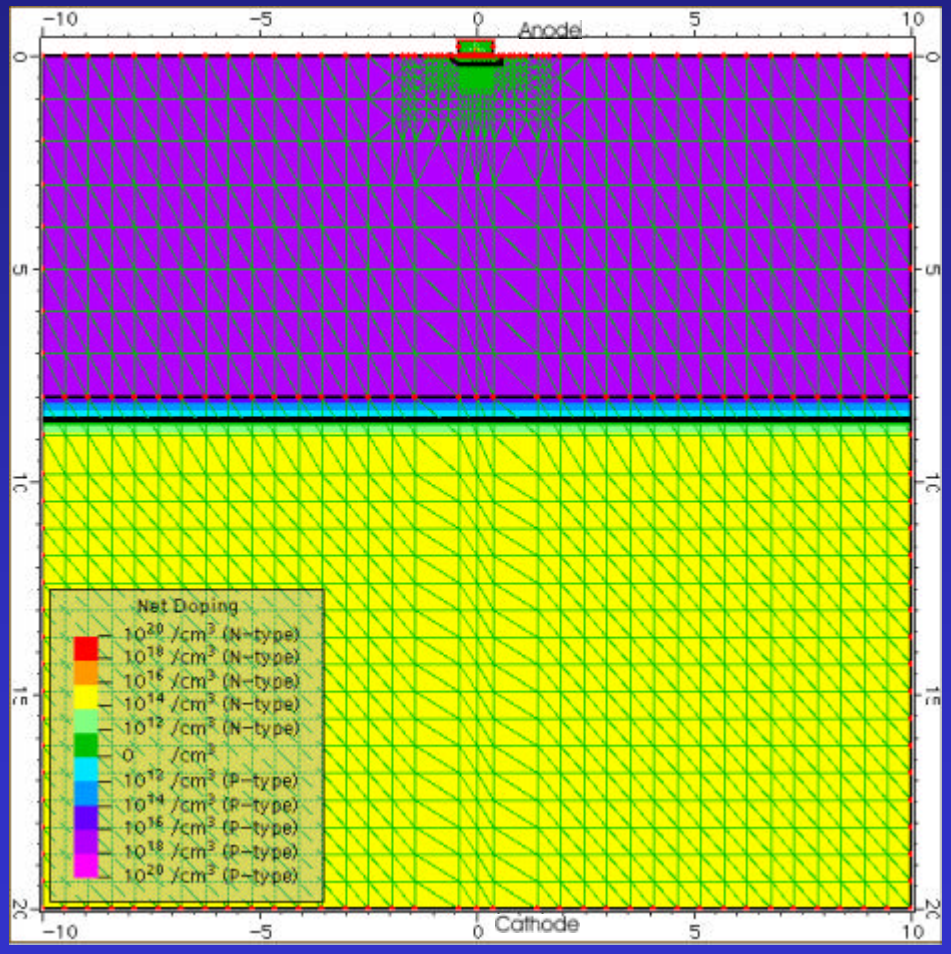
Vertical Geometry



Structure Simulations

1st step: Diode

Xe beam 459 MeV



Reverse bias : 6 V
0° impact

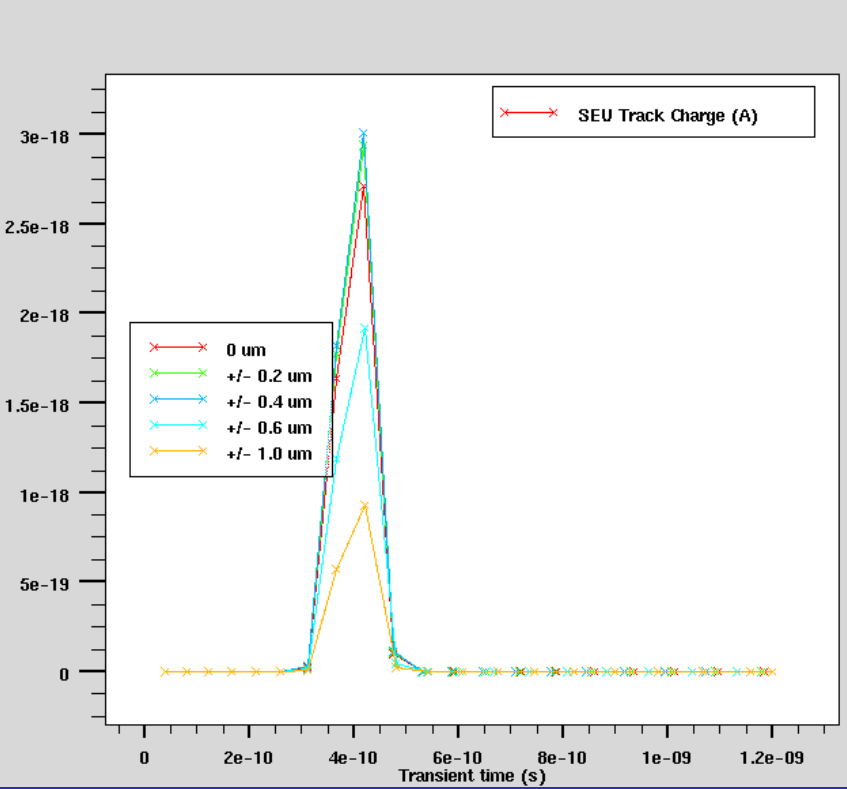
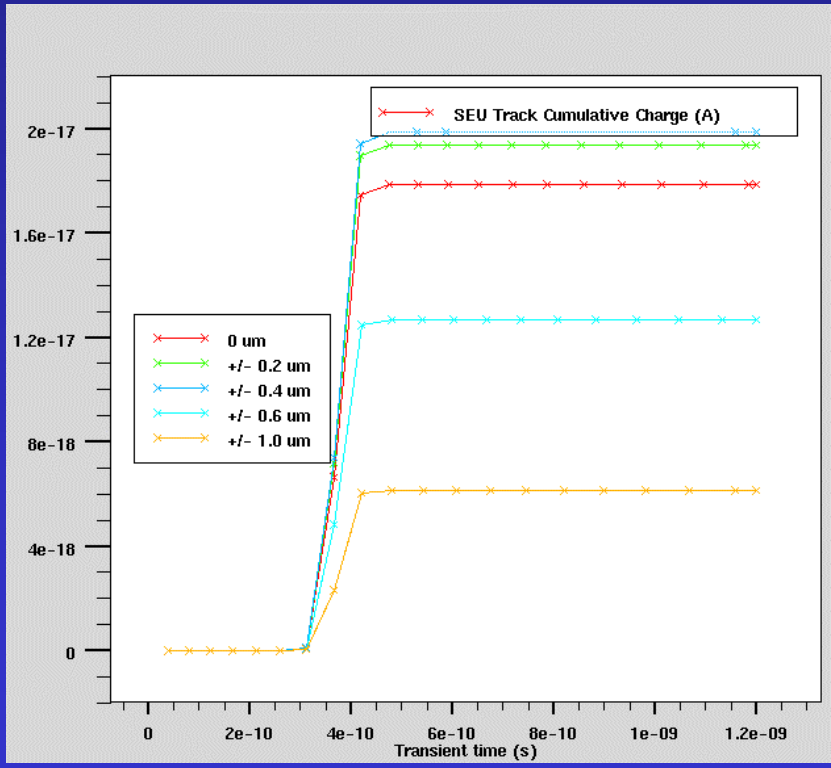
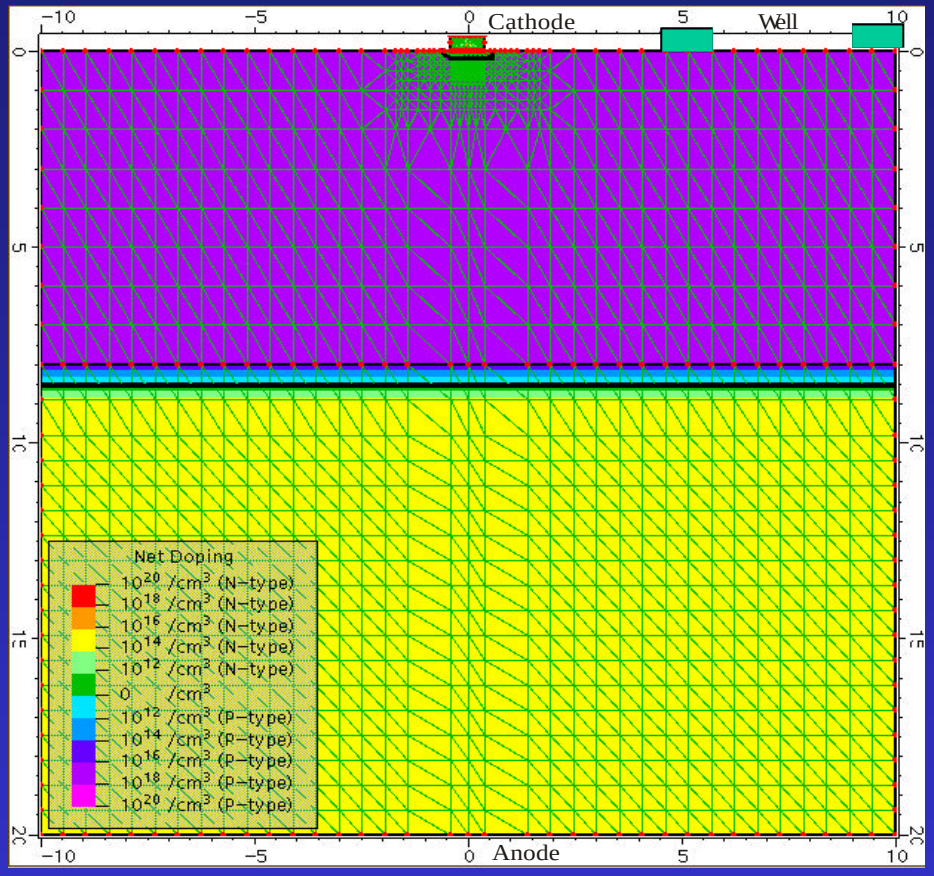


Photo I



Cumulative photo I



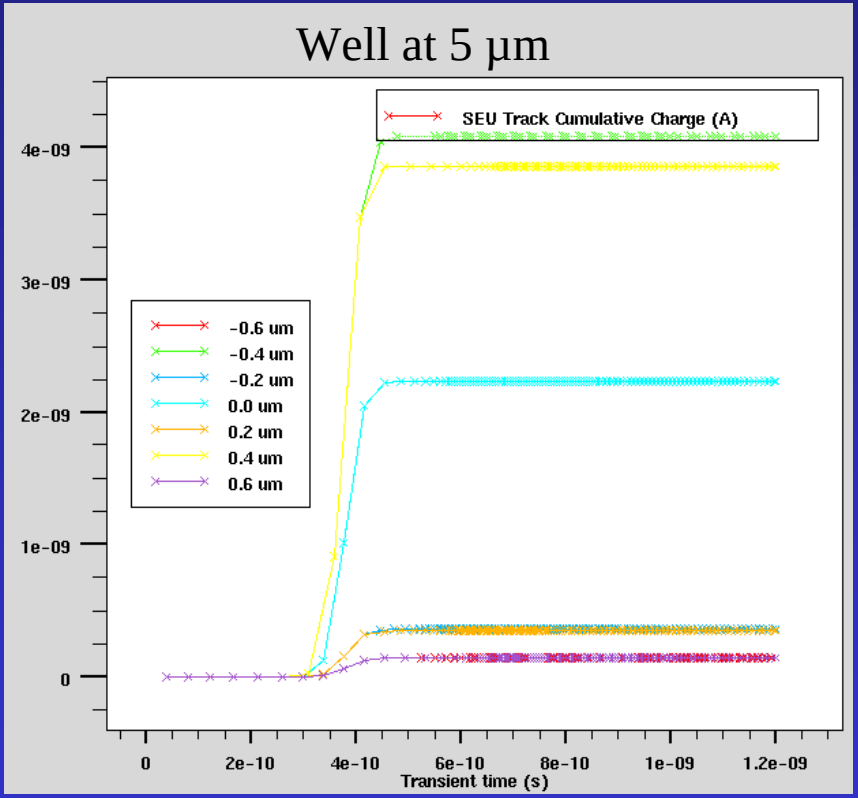
2nd step: well added

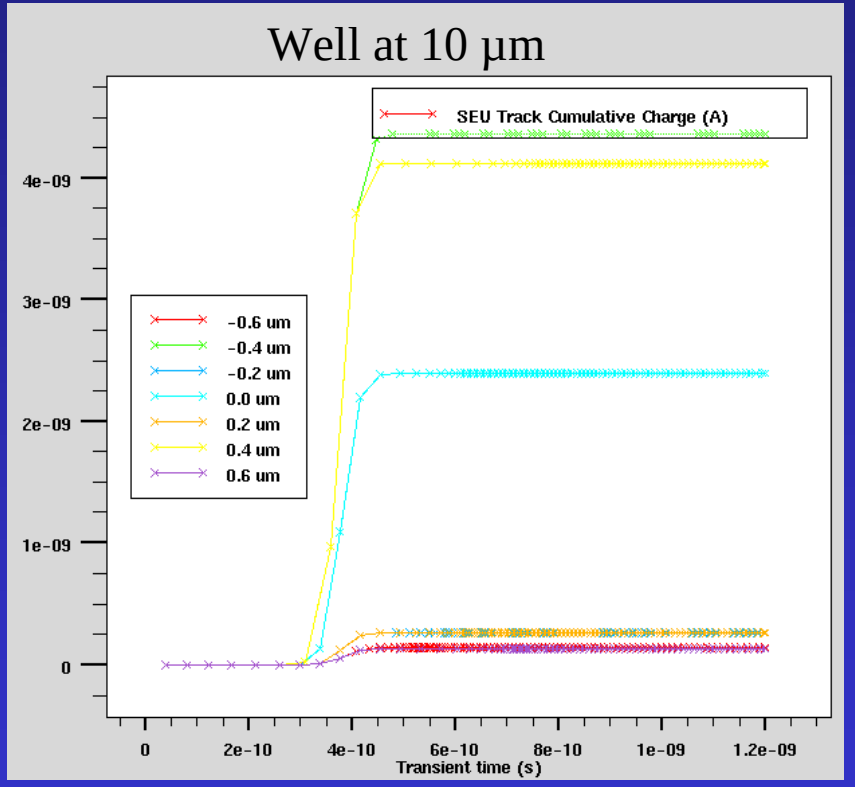
Studied effects:

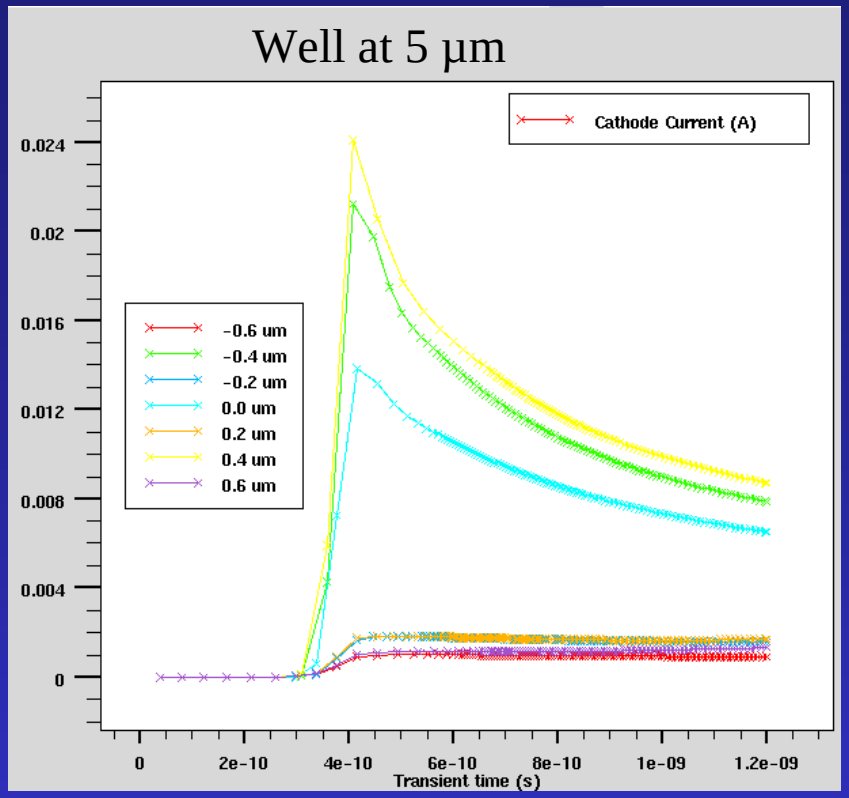
- Well and ion strike localization
- Well position and bias influence
- I dependency on ion track angle

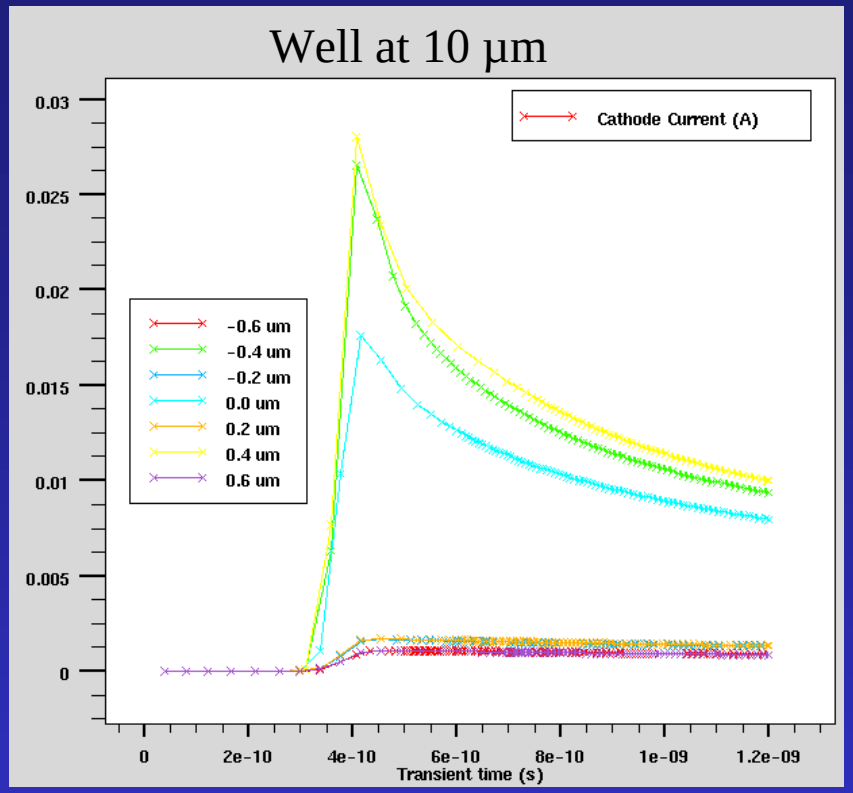
1- Well and ion strike localization:

Structure reverse biased at 6V, $V_{well} = V_{substrate} = 0V$



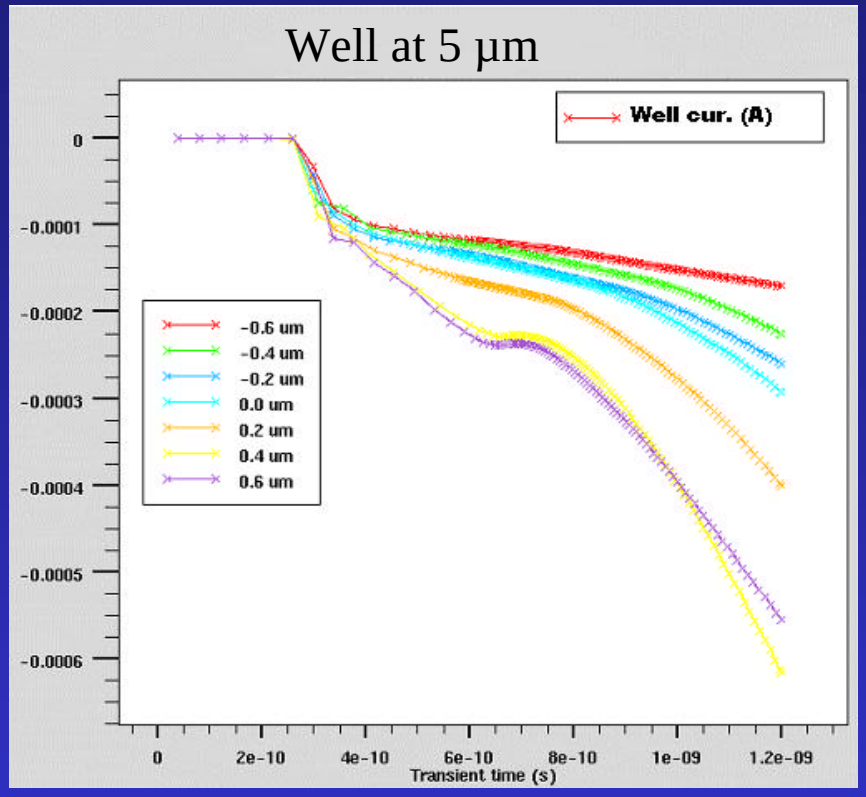




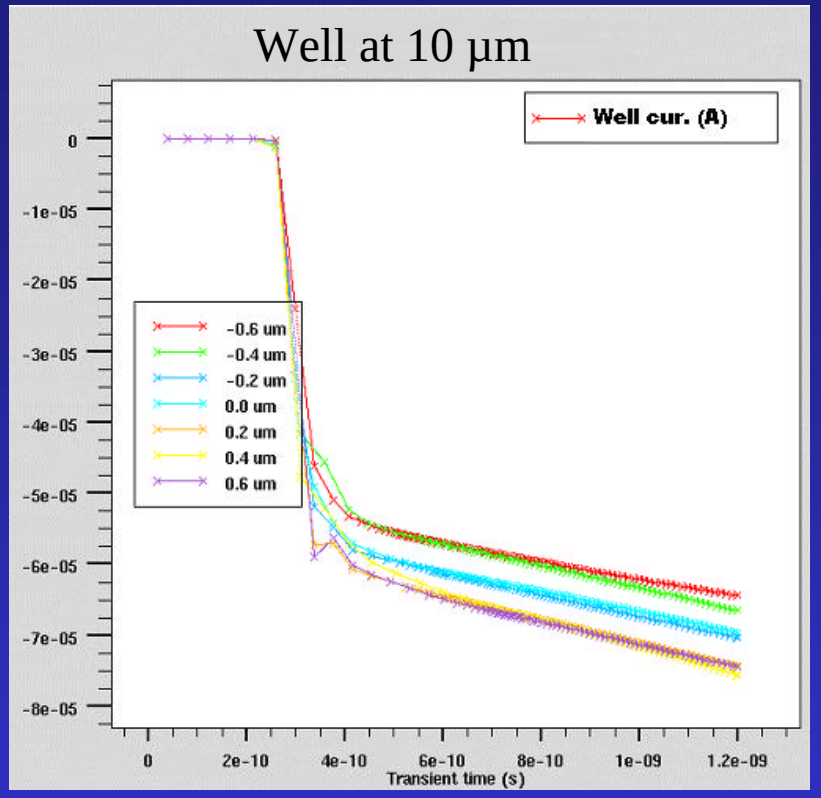


- Ic larger for strikes in high inversion region
- Ic larger for 10 µm Well position

Well at 5 µm



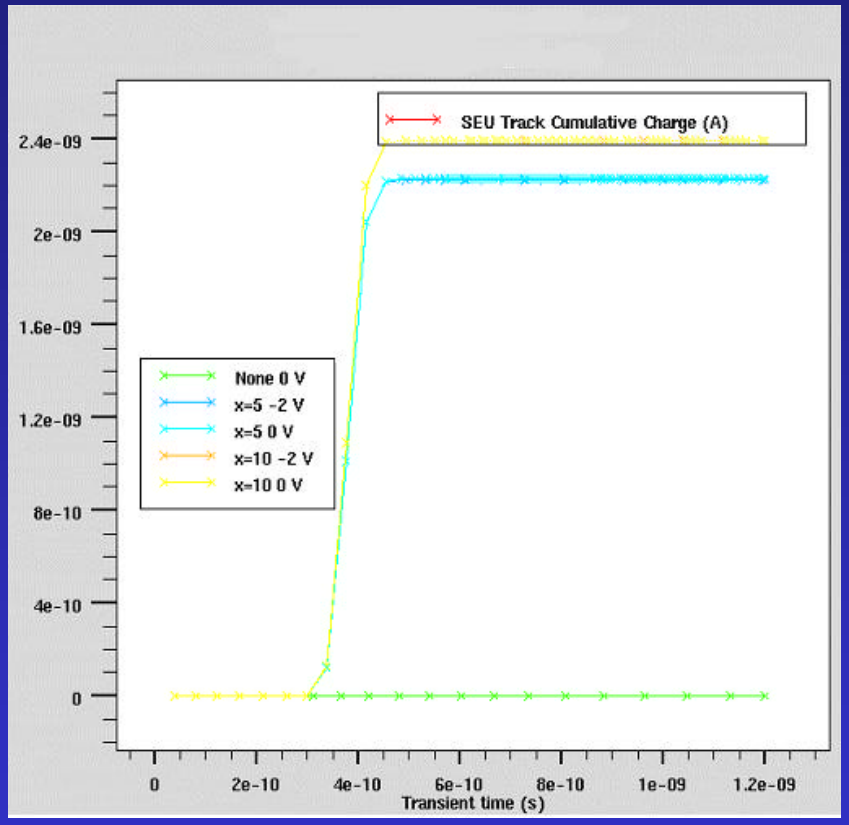
Well at 10 µm

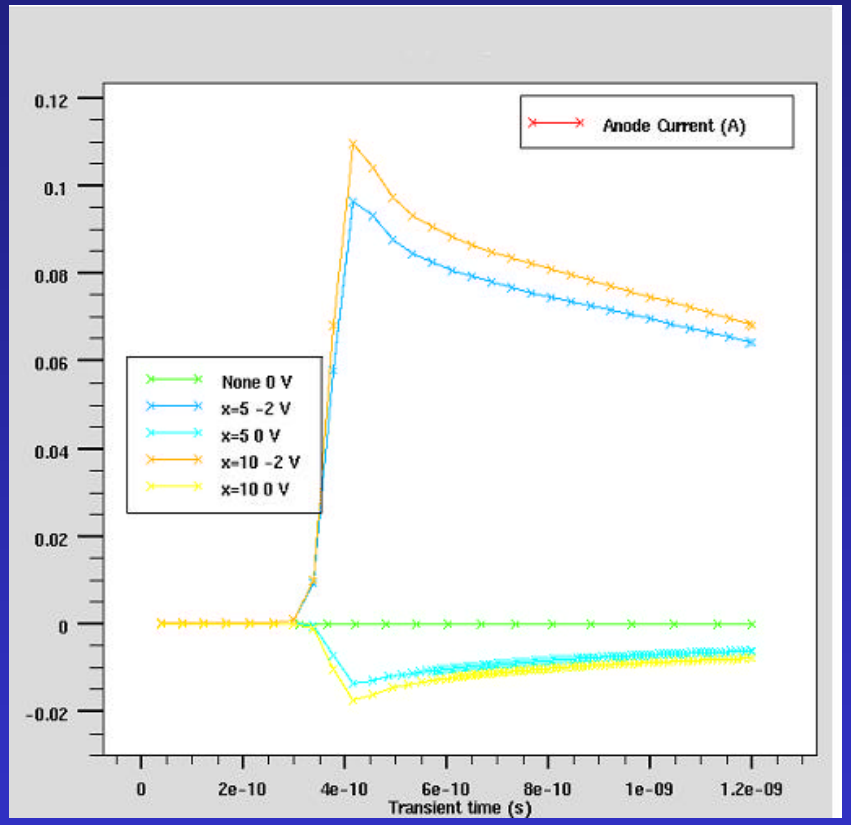


- Iw smaller for edge located well

2- Well position and bias influence :

Well at 5 and 10 µm / 0V and –2 V rev. bias





- No influence of bias on cum. Q
- Ia increase with reverse bias
- Cum. Q and Ia larger for remote position of the well

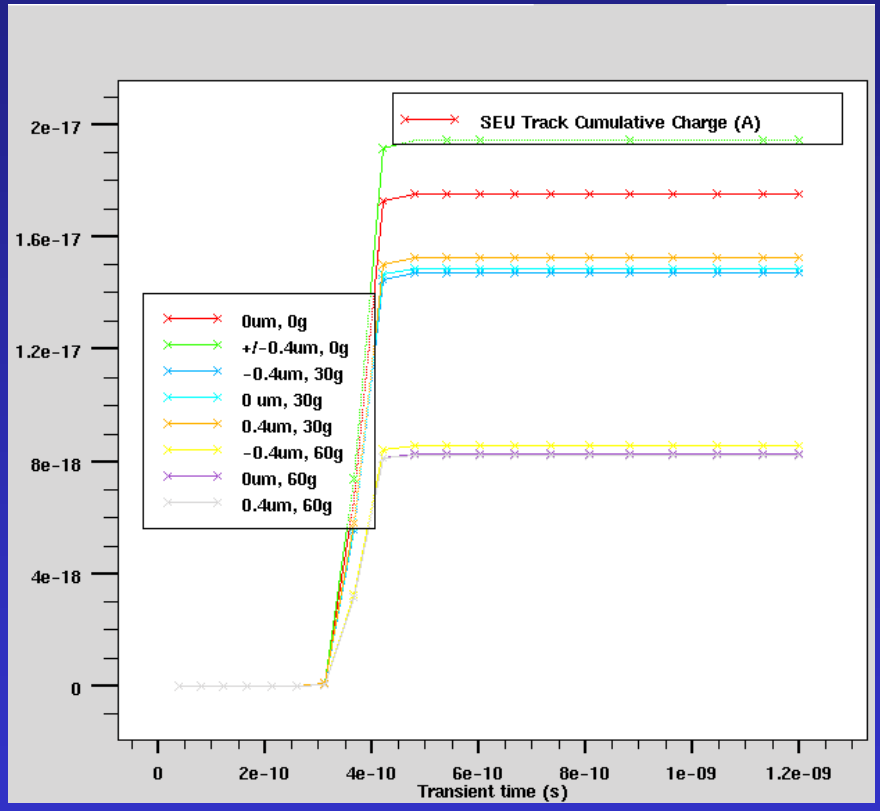
3- I dependency on ion track angle:

3 structures analyzed:

- No Well contact.
- Well at 10 µm.
- Well at 5 µm.

For each structures: ion strike at 0° – 30° and 60° with different entry points

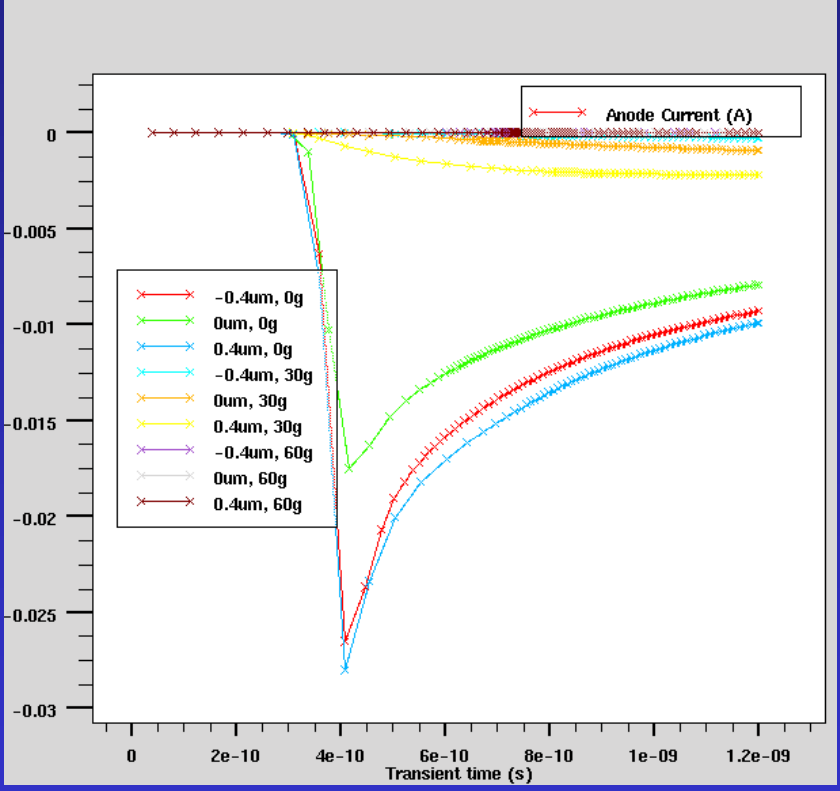
3.1 – No Well:



- ✓ Lower values for large angles.
- ✓ Edge impact → larger Q

3.2 – Well on edge (10 µm):

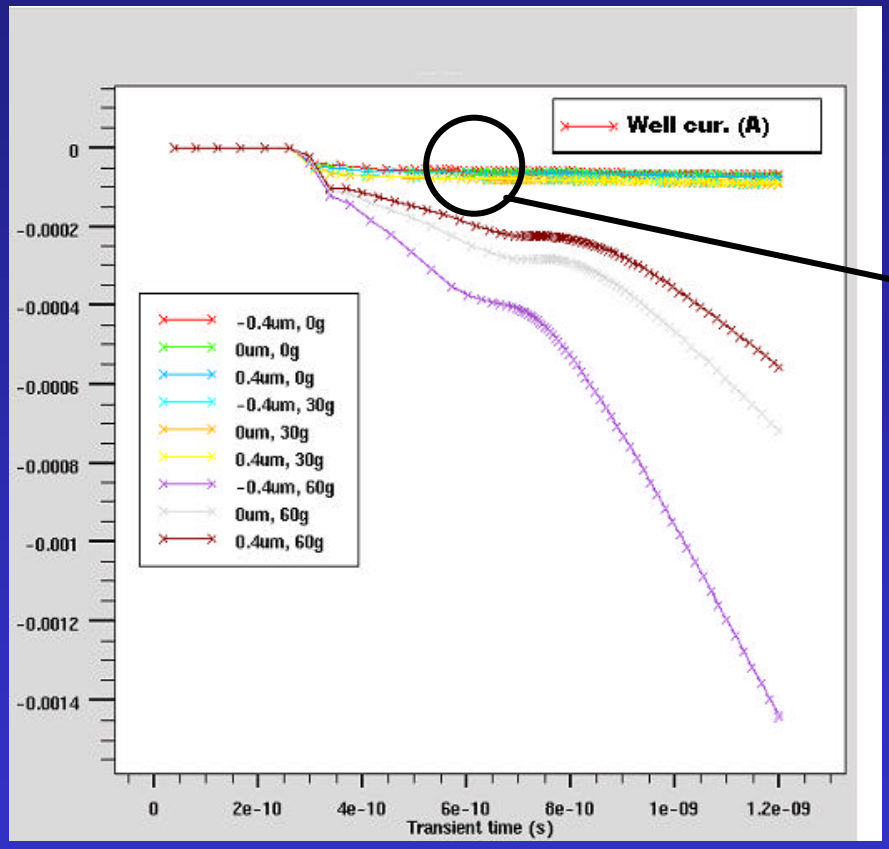
Anode current

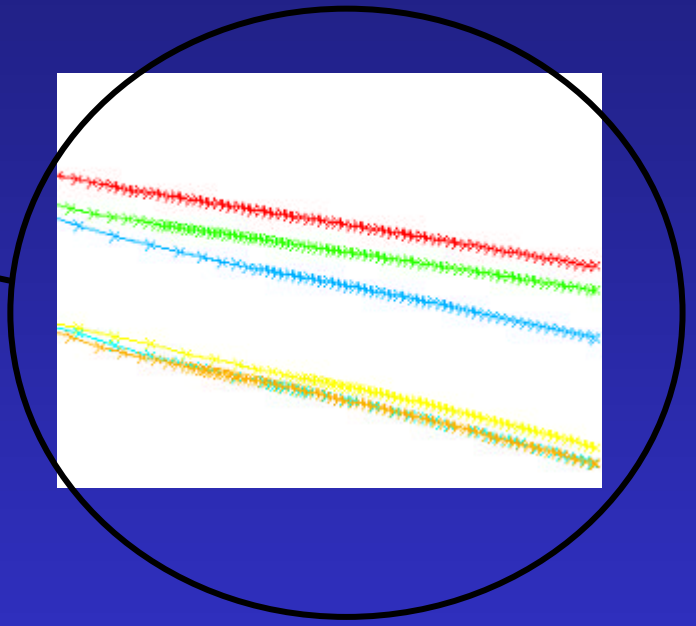


- ✓ Larger for large angle.
- ✓ Larger if edge strike.
- ✓ Larger if strike on the same side as Well

3.2 – Well on edge (10 µm):

Well current

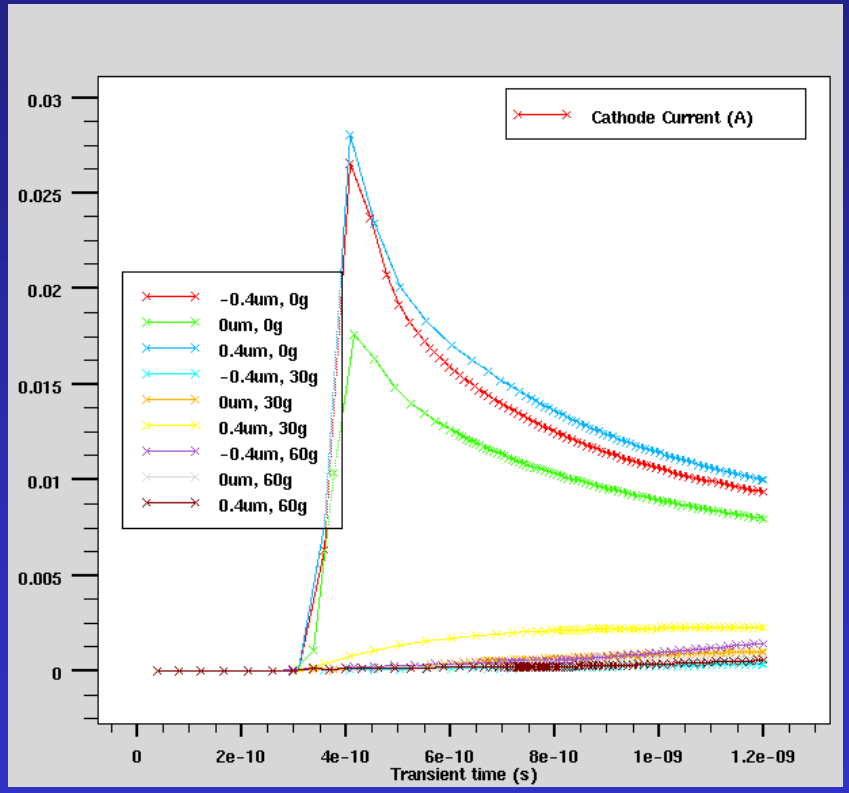




- ✓ Most negative for large angle.
- ✓ Lowers while scan impact from well side to opposite.

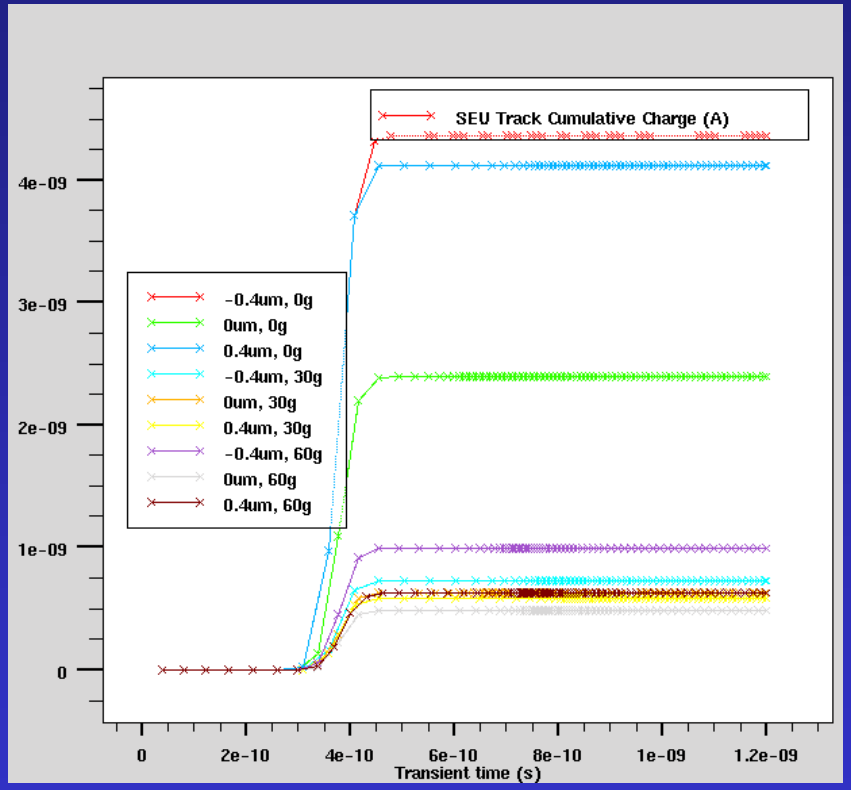
3.2 – Well on edge (10 µm):

Cathode current



- ✓ Higher for 0° strikes.

Cumulative Charge:



- ✓ Larger for 0° strikes.

Conclusions

- ✓ Diode simulations:

  - Higher photocurrent for strike at beginning of ox.
    (high depletion → Q move faster to electrodes)

  - Lower I while angle increases.

- ✓ Well contact (*SRAM transistor structure*):

  - Same effect, current higher for normal incidence.
    (Ic modification extands longer while tilted. 0° Q are in the same direction as current flow → faster contribution to Ic)

Q_{coll} in PN diodes with CMOS-like shallow junction depth and high substrate doping decrease in amplitude and shows longer time constants when the ion strikes are tilted or on the periphery of the device