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SEE Verification Test of Unitrode and T.I. UCC 1806 Using Application Test conditions

by

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Abstract

Two different UCC1806 controllers were SEE assessed against He-Ion Single Event Burnout. Soft Error events as pulse drop-outs and activation of protection latch were also charaterised. The UCC1806 controllers were tested in a closed loop mode on two different DC/DC converter applications.

MAIN PURPOSE OF TEST

A project alert was raised to prove SEB tolerance of UCC1806. Knowing the test results from the Rosetta UCC1801 test campaign (30 January 2001,4th D/TOS-QCA Final presentation Day), application relevant heavy ion SEE testing of UCC1806 was carried out at the HIF, UCL, Belgium – assessing in priority order the following:

- **To prove that no hard-failure occurrence under test conditions representative for DC/DC implementations 1 & 2 of the UCC1806 – up to a LET of 34 MeV/(mg/cm^2).**

- **To characterise as many soft-error phenomenon as possible**

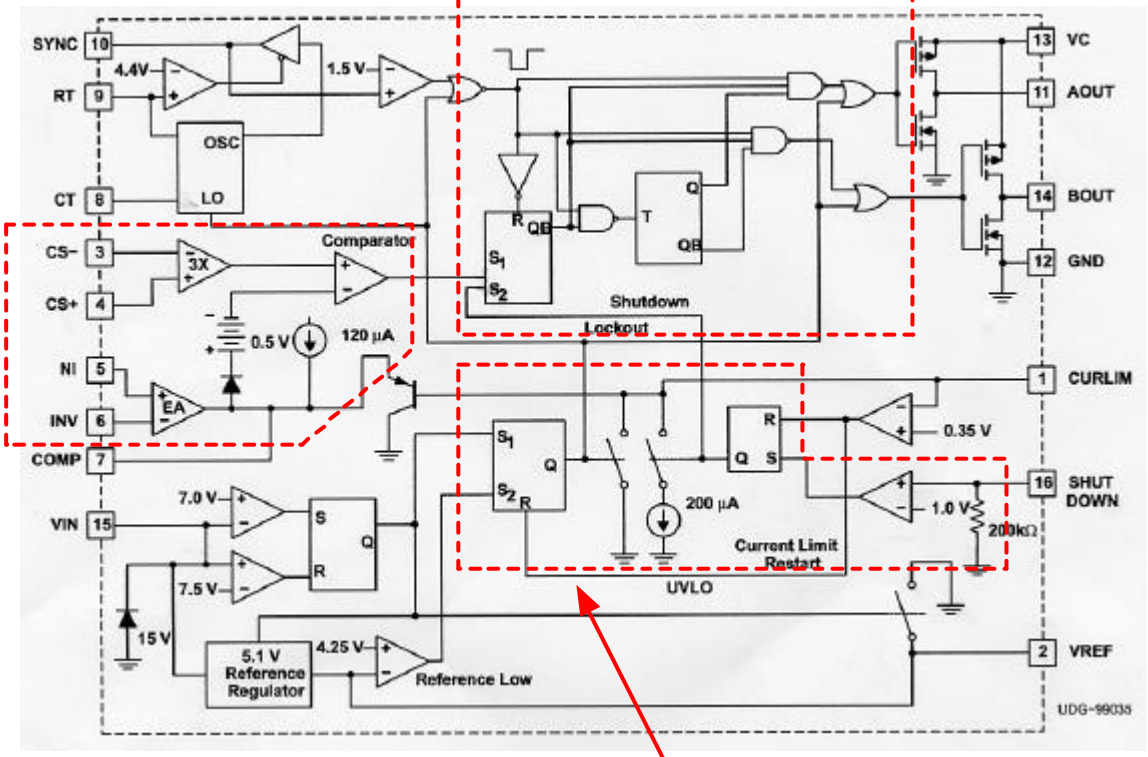
- **To quantify the soft-error event occurrence**

- **To propose methods of preventing SEE in DC/DC converter design implementation**

THE UCC1806 CHIP ARCHITECTURE

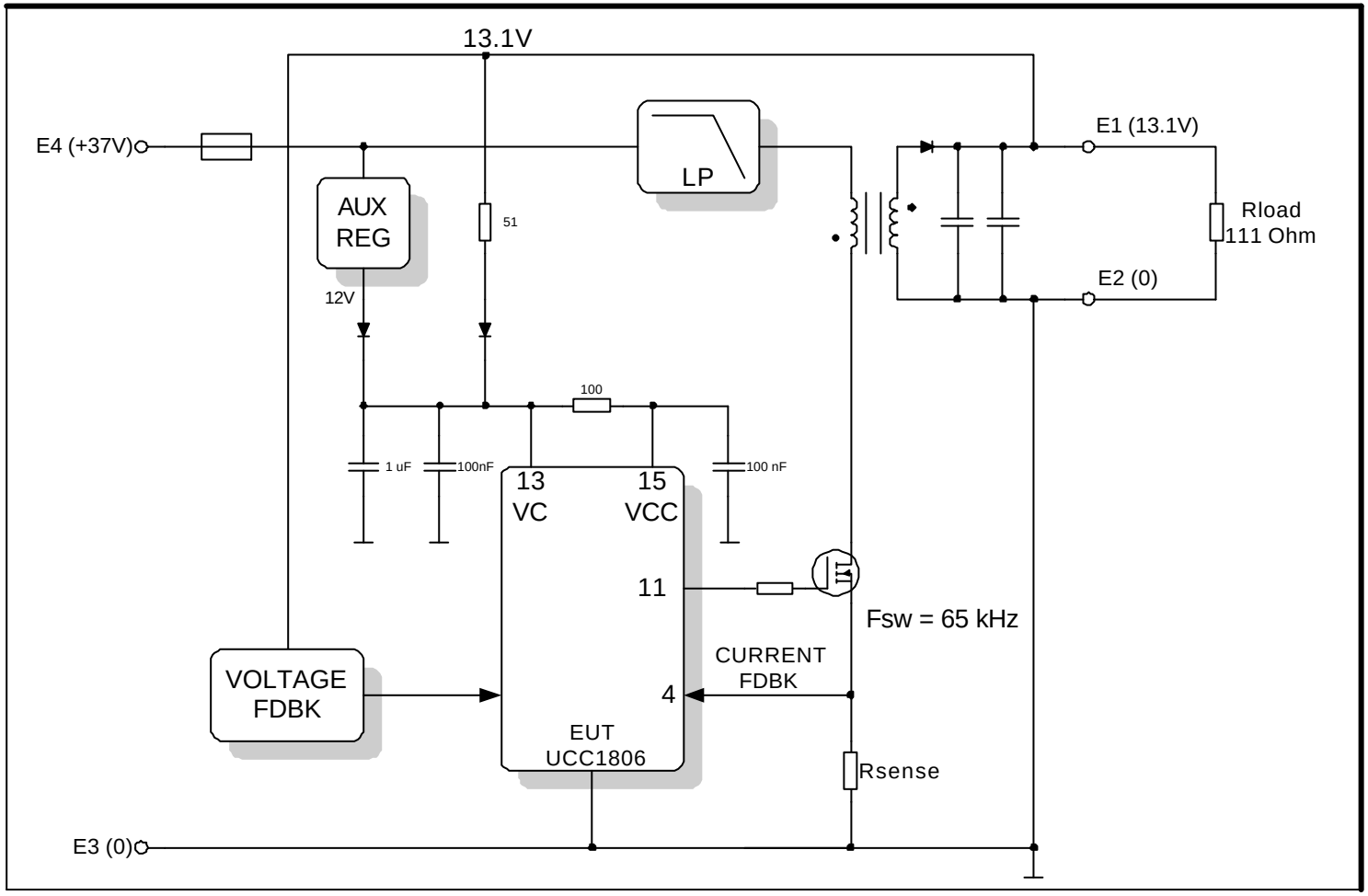
SF1 - Pulse Drive Logic

SF3 - Control Loop Amp/Cmp



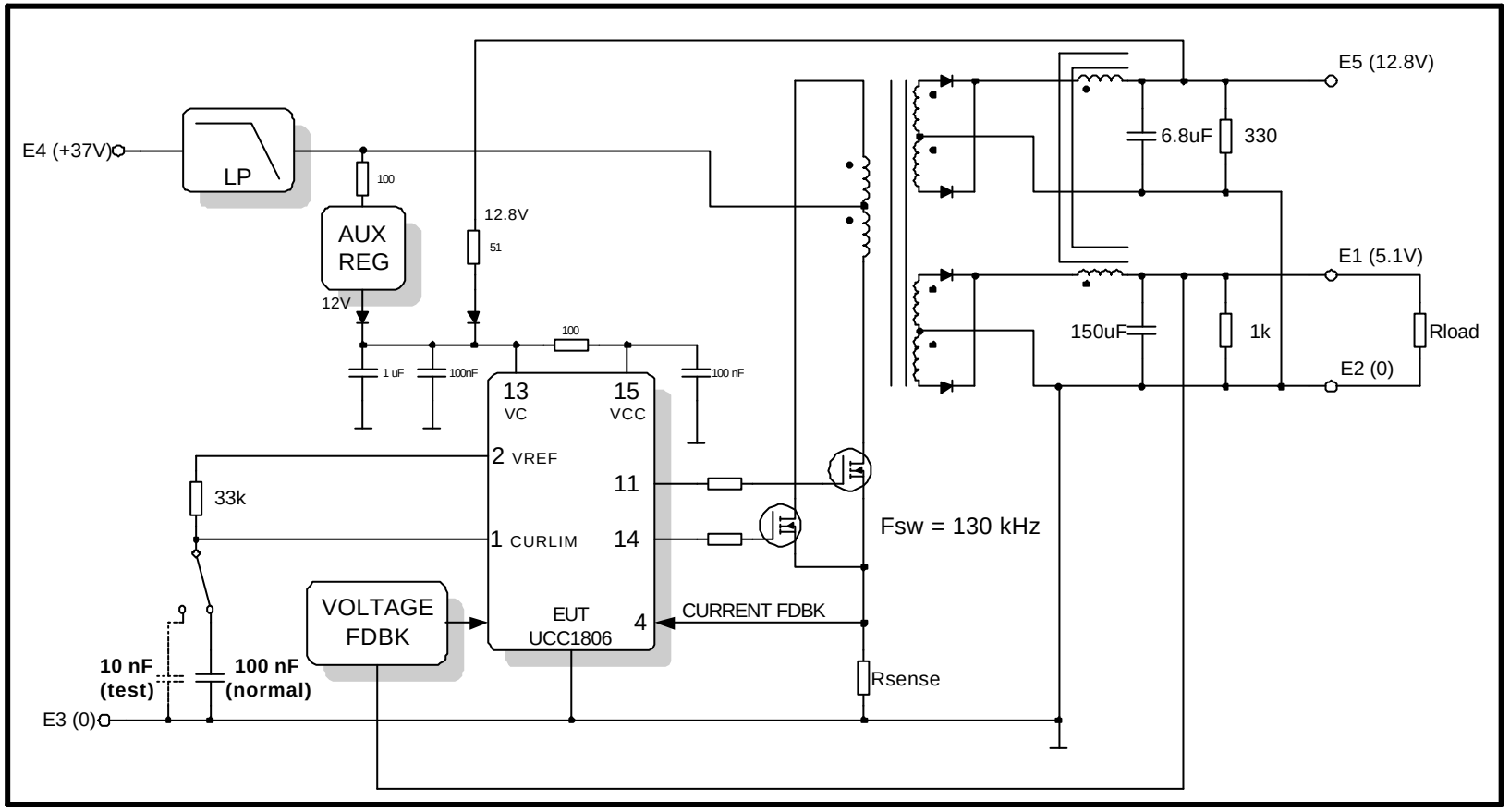
SF2 - Protection Latch Logic

TEST BOARD 1 – PROVIDED BY TERMA



TEST BOARD 2 – BUILT UP BY ESTEC

(The board is as close to the project application as possible)



TEST SAMPLES

Two different lot date codes were available for tests of UCC1806. Samples tested carried the following marking:

Unitrode samples

- 8A9845
- UCC1806 J/883B
- 5962-9457501 MEA
- **U Q** (Unitrode)

Texas Instrument samples

- 1A-T 0126C
- 5962-9457501 MEA
- UCC1806 J/883B
- **THA Q** (Texas Instruments)

RESULTS FROM TERMA TEST BOARD

LET MeV/(mg/cm^2)	ION TYPE TILT	FLUENCE [P/CM^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3
14.1	AR - 0º	5.0X10^6	#01	1.5	0	NOTE (1)	NOTE (2)	0
28.2	AR - 60º	1.0X10^6	#01	1.5	0	NOTE (1)	NOTE (2)	0
34.0	KR - 0º	1.0X10^6	#01	1.5	0	NOTE (1)	NOTE (2)	0
48.1	KR - 45º	1.0X10^6	#01	1.5	0	NOTE (1)	NOTE (2)	0
68.0	KR - 60º	1.0X10^6	#01	1.5	0	NOTE (1)	NOTE (2)	0

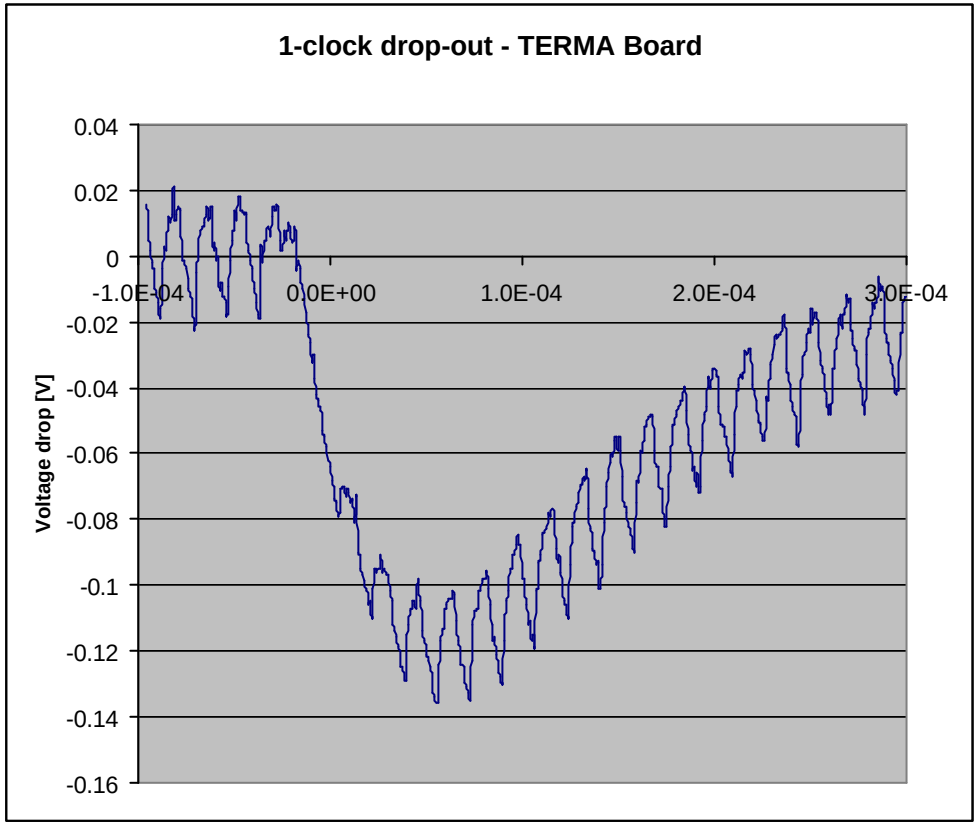
Main conclusions:

- No hard failures
- SEU causing 1-clock drop-outs on outputs are present (SF1)
- SEU in protection latch assumed (SF2), but not proven by this application

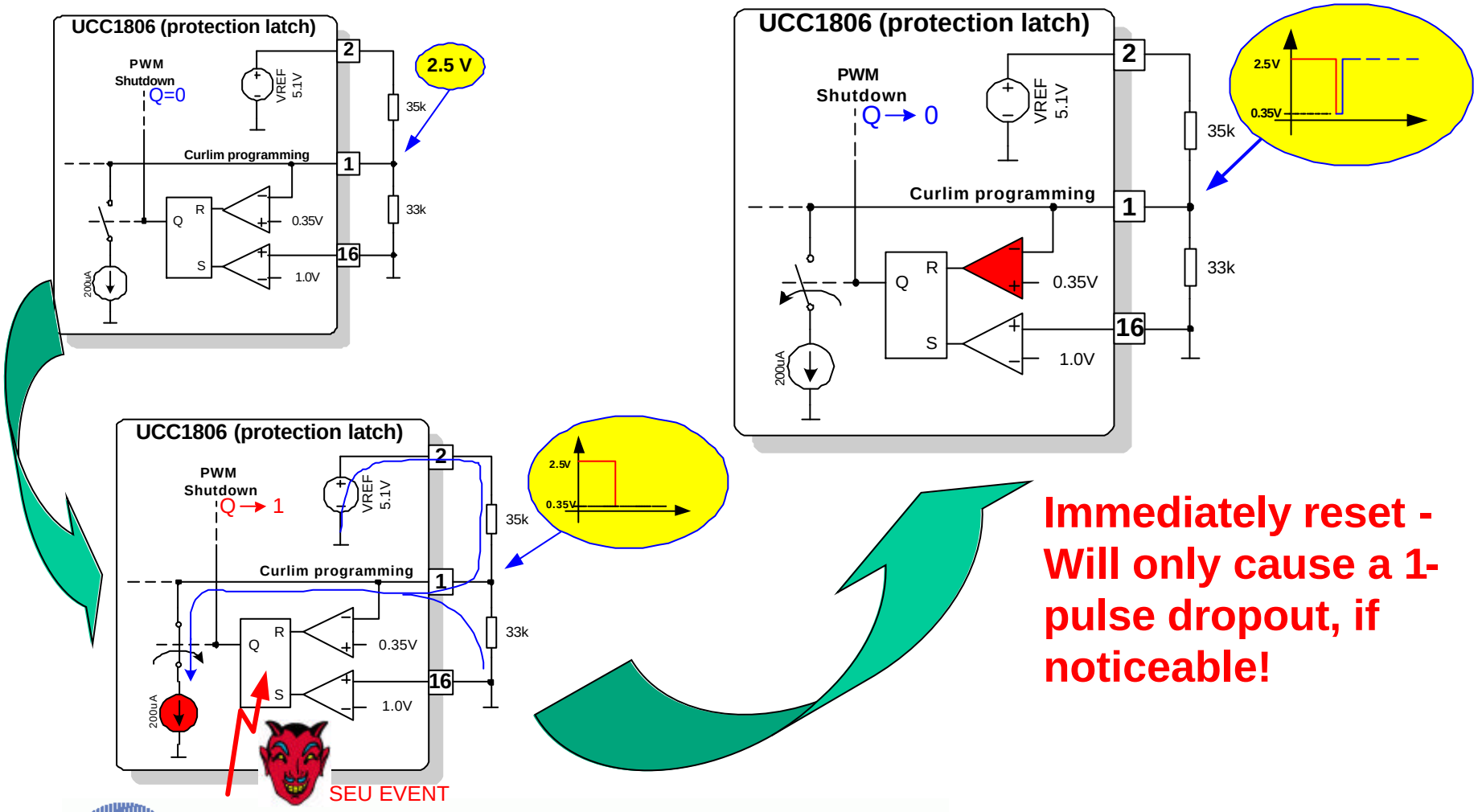
TERMA TEST BOARD – OUTPUT 1-PULSE DROPOUT (SF1)

The interrupted UCC1806 switching is restored automatically. Here the case is a "1-clock cycle" interruption. The voltage-drop amplitude is determined by the configured output current and the output capacitance value together with our <u>resistive</u> load.

The measured drop is close to the theoretical.



TERMA TEST BOARD – PROTECTION LATCH SEU (SF2)



Immediately reset - Will only cause a 1-pulse dropout, if noticeable!

RESULTS FROM ESTEC TEST BOARD (1) / UNITRODE #03

LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3
14.1	Ar - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	6	0
14.1	Ar - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
19.9	Ar - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
19.9	Ar - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	7	0
28.2	Ar - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	21	0
28.2	Ar - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	16	0
34.0	Kr - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	16	0
34.0	Kr - 0º	1.0x10^6	#03	LOAD1	0	Note (3)	21	0
48.1	Kr - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	23	0
48.1	Kr - 45º	1.0x10^6	#03	LOAD1	0	Note (3)	18	0
68.0	Kr - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	24	0
68.0	Kr - 60º	1.0x10^6	#03	LOAD1	0	Note (3)	26	0

Note (3): The effect of 1-clock cycle drop out on the PWM output switching was not recorded.

Main conclusions:

- No hard failures
- SEUs causing 1-clock drop-outs on outputs are present (SF1)
- SEUs in protection latch are present (SF2)

RESULTS FROM ESTEC TEST BOARD (2) / T.I. s/n #TI4

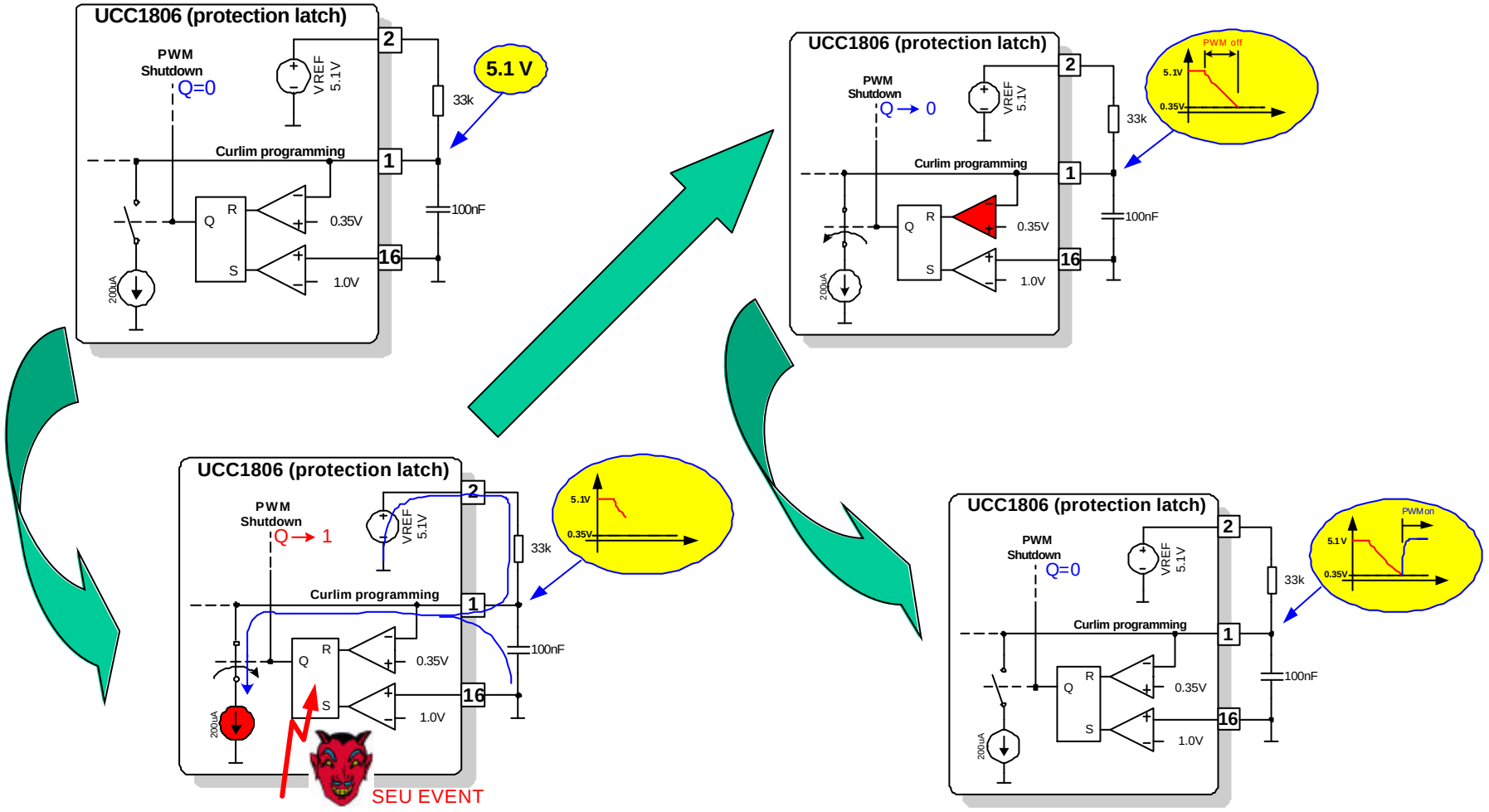
LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3 Note (5)
14.1	Ar - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	6	0
14.1	Ar - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	11	0
19.9	Ar - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	15	0
19.9	Ar - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	9	0
28.2	Ar - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	21	0
28.2	Ar - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	15	0
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	10	0
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	18	0
48.1	Kr - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	22	0
48.1	Kr - 45º	1.0x10^6	#TI4	LOAD1	0	Note (4)	24	0
68.0	Kr - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	18	0
68.0	Kr - 60º	1.0x10^6	#TI4	LOAD1	0	Note (4)	21	0

Note (4): The effect of 1-clock cycle drop out on the PWM output switching was not recorded.

Main conclusions:

- No hard failures
- SEUs causing 1-clock drop-outs on outputs are present (SF1)
- SEUs in protection latch are present (SF2)

ESTEC TEST BOARD – PROTECTION LATCH SEU (SF2)



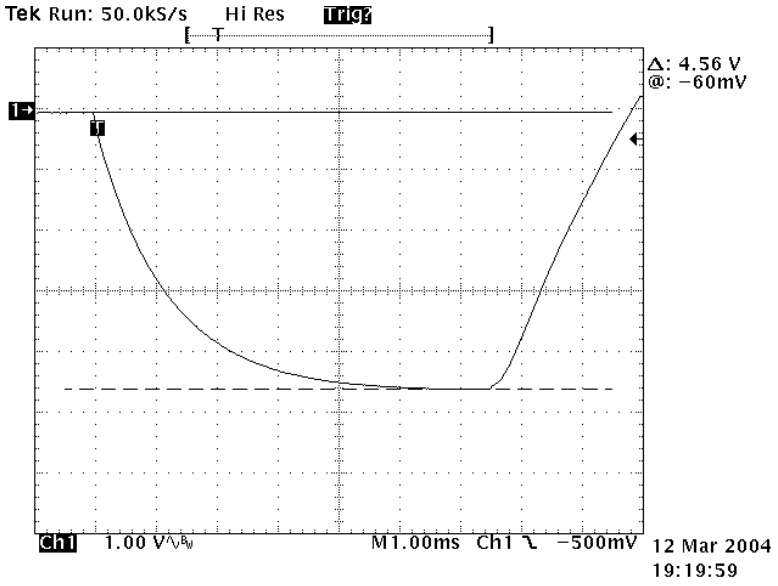
ESTEC TEST BOARD – SF2 DROP-OUT ON A 5V / 1A LOAD

Experimental data:

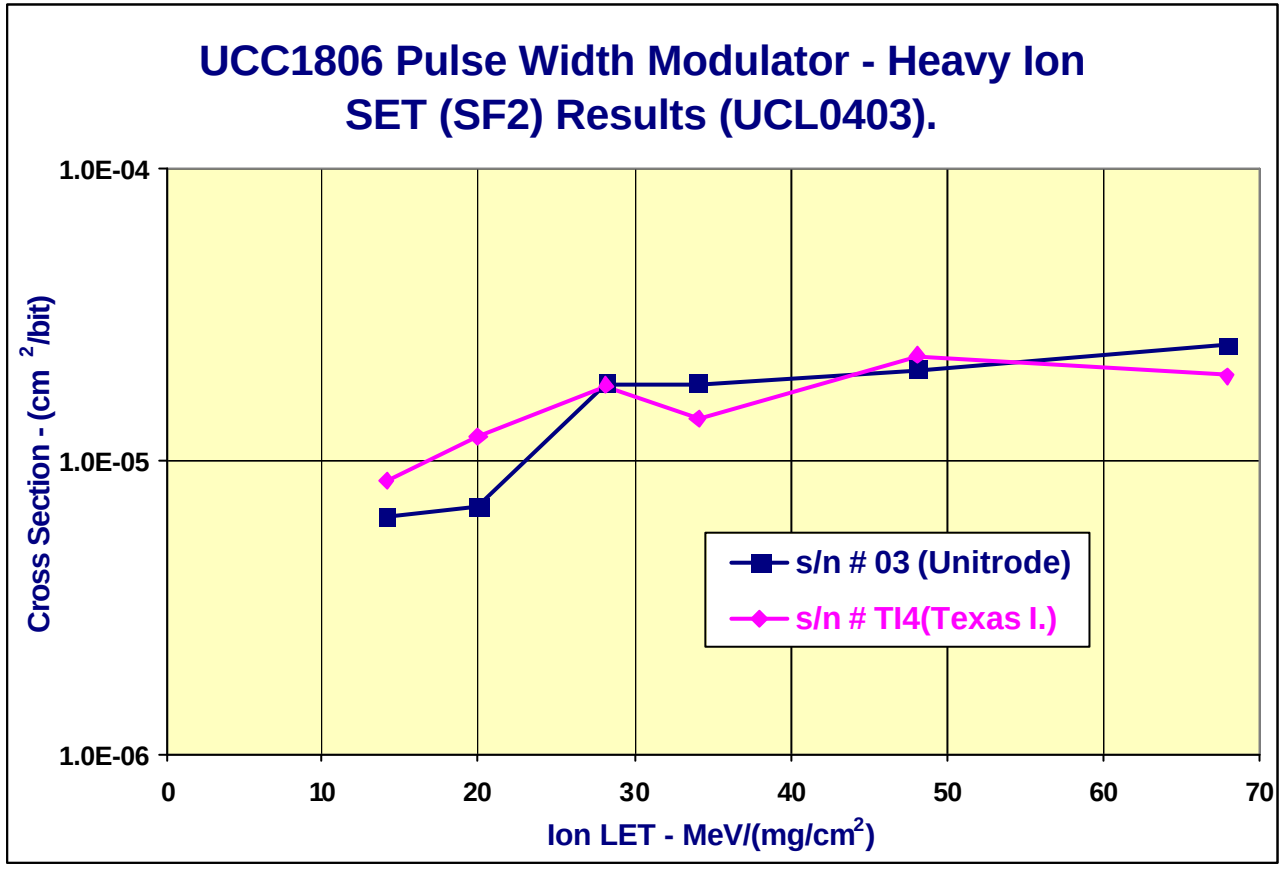
- Sample: Texas Instruments s/n #TI4
- LOAD1 **(+5V @ 1A load)**
- LET 34 MeV/(mg/cm^2)

The dropout time duration (i.e. PWM clock interruption) is ca 6.5 ms.

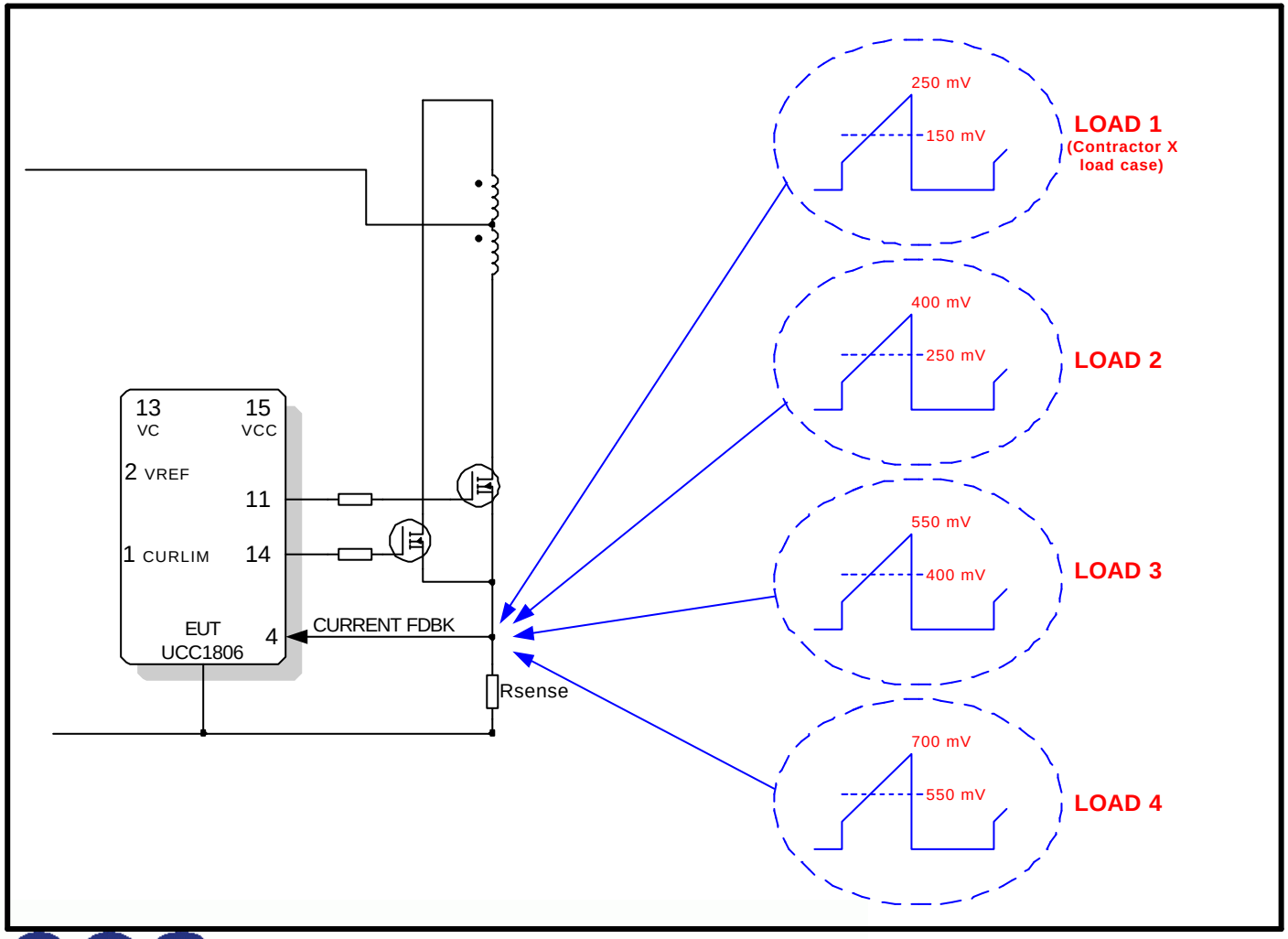
The result is a **–4.6V drop** on the +5V output voltage. **This is a typical scenario on an application with large capacitance on PIN1.**



ESTEC TEST BOARD – SF2 SUMMARY



EXTENDED TESTS – INCREASING VOLTAGE LEVEL ON PIN4



EXTENDED TESTS - RESULTS

LET MeV/(mg/cm^2)	Ion type Tilt	Fluence [p/cm^2]	s/n	Load Pout [W]	RESULT			
					HF	SF1	SF2	SF3 Note (5)
EXTENDED TESTS / PIN4 VOLTAGE BIASING SESITIVITY								
34.0	Kr - 0º	1.0x10^6	#TI4	LOAD1	0	Note (4)	19	0
68.0	Kr - 60º	5.0x10^5	#TI4	LOAD1	0	Note (4)	20	0
34.0	Kr - 0º	5.0x10^5	#TI4	LOAD2	0	Note (4)	13	1
68.0	Kr - 60º	5.0x10^5	#TI4	LOAD2	0	Note (4)	13	0
34.0	Kr - 0º	5.0x10^5	#TI4	**LOAD3**	0	Note (4)	5	**~100**
68.0	Kr - 60º	5.0x10^5	#TI4	**LOAD3**	0	Note (4)	21	**~120**
34.0	Kr - 0º	1.0x10^6	#TI4	**LOAD4**	0	Note (4)	18	**~200**
68.0	Kr - 60º	5.0x10^5	#TI4	**LOAD4**	0	Note (4)	19	**~150**

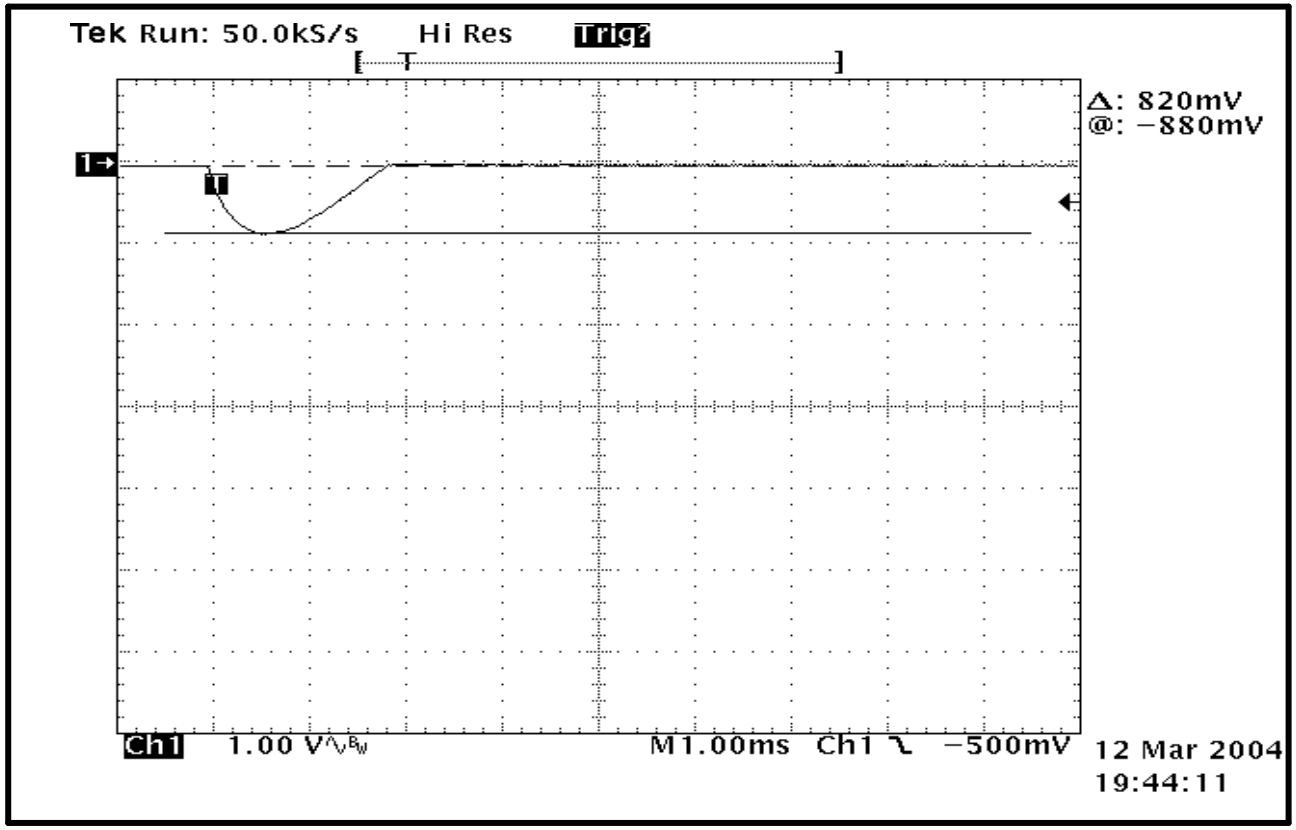
Note (4): The effect of 1-clock cycle drop out on the PWM output switching was not recorded.

Note (5): Trigger detection level for the negative transients was set to –0.5V

Main conclusions:

- No hard failures
- Besides having the SF2 behaviour, a new SEU transient behaviour appears on the voltage output, SF3. The only explanation is (for now) that analogue circuits in the voltage/current feedback are affected.

CONTROL LOOP INDUCED VOLTAGE TRANSIENT – SF3



This behaviour can not be re-created with PWM interruption