Radiation Characterization of Advanced Submicron Devices

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SEEDS FOR TOMORROW'S WORLD

OUTLINE

- Project structure
- Results of the liquid helium temperature irradiations (HERSCHEL components)
- Results of the radiation assessment of advanced components
  - 0.13 µm bulk CMOS
  - 0.13 µm PD SOI CMOS
- Outlook

PROJECT STRUCTURE

- Work order 14924/00/NL/ND start date: 15 February 2001 –14 February 2003

- Two main parts:

  Radiation assessment of cryogenic electronics

  Radiation assessment of deep submicron CMOS devices (0.13 μm CMOS generation)

- Since 1 January 2004: rider till end of 2005

  Radiation assessment of sub 100 nm CMOS devices

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MOTIVATION:WHY CRYOGENIC IRRADIATIONS?

- The radiation response of CMOS components shows a pronounced temperature dependence, e.g., at cryogenic temperatures, no interface states are formed.

- Total-dose damage should be worst case at cryogenic temperatures (no annealing), while the opposite holds for displacement damage.

- At cryogenic temperatures, specific effects (kink/ hysteresis) may occur.

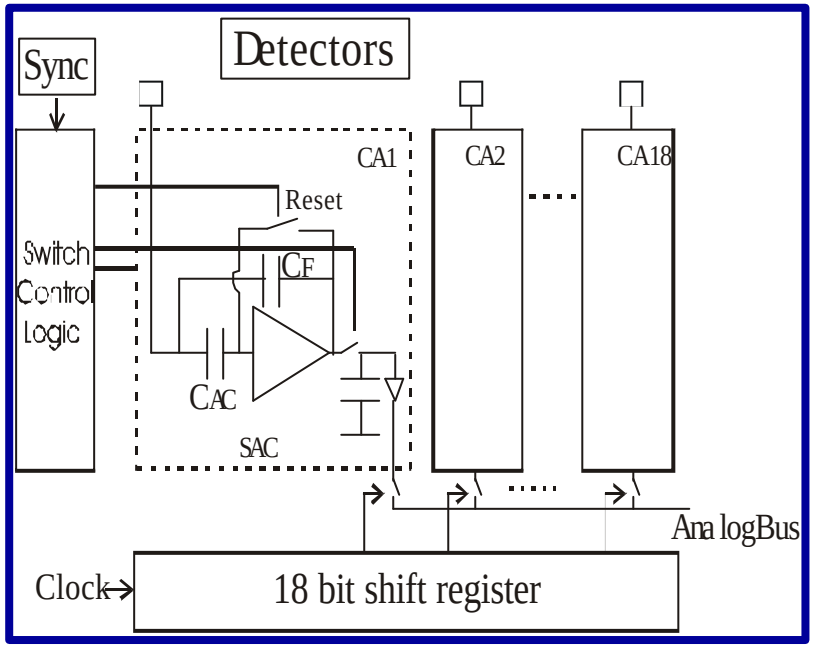
⇒ *Importance of cryogenic radiation testing*

CRYOGENIC IRRADIATIONS

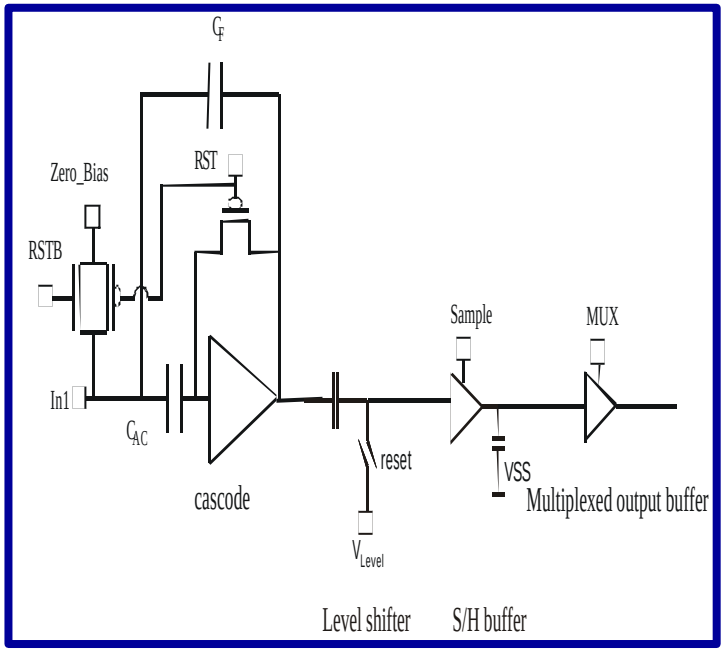
- The selected parts have been fabricated in a 0.7 μm non-hardened CMOS technology, which is used for prototyping the PACS read-out electronics for the HERSCHEL mission (AMI-Semiconductor, Oudenaarde).
- Both single transistors (amplifier) and read-out circuits and circuit blocks have been irradiated at LHT.
- Facilities:
  - ^{60}Co Gamma's at ESTEC in Noordwijk, up to 15/30 krd(Si) at a dose rate of 100 rd(Si)/min.
  - 60 MeV protons at Cyclone (Louvain-la-Neuve), to a fluence of 10^{11} p/cm^2 (1x to 3x10^8 p/cm^{2}s flux).

PROTOTYPE CIRCUITS

Complete PACS CRE ARRAY

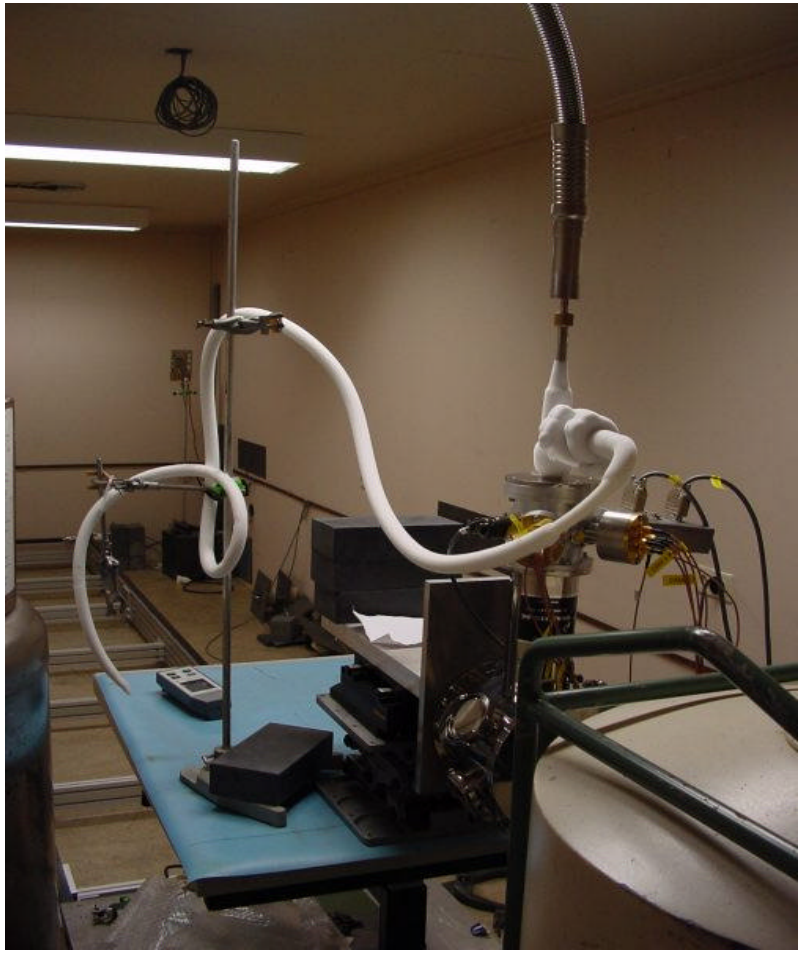


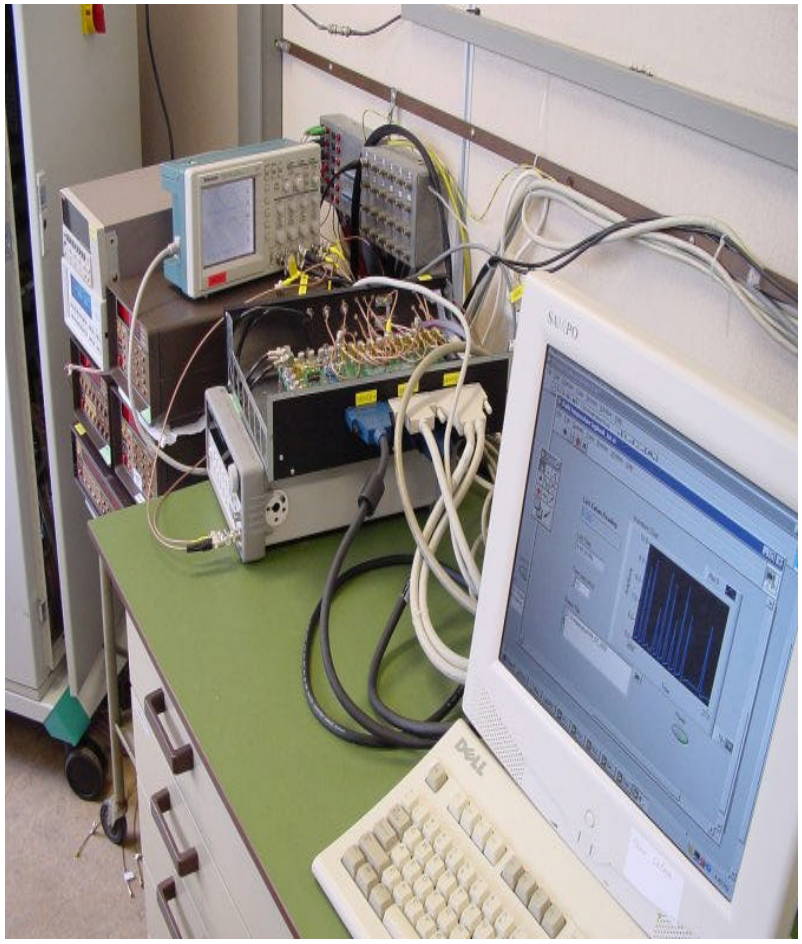
Layout single channel



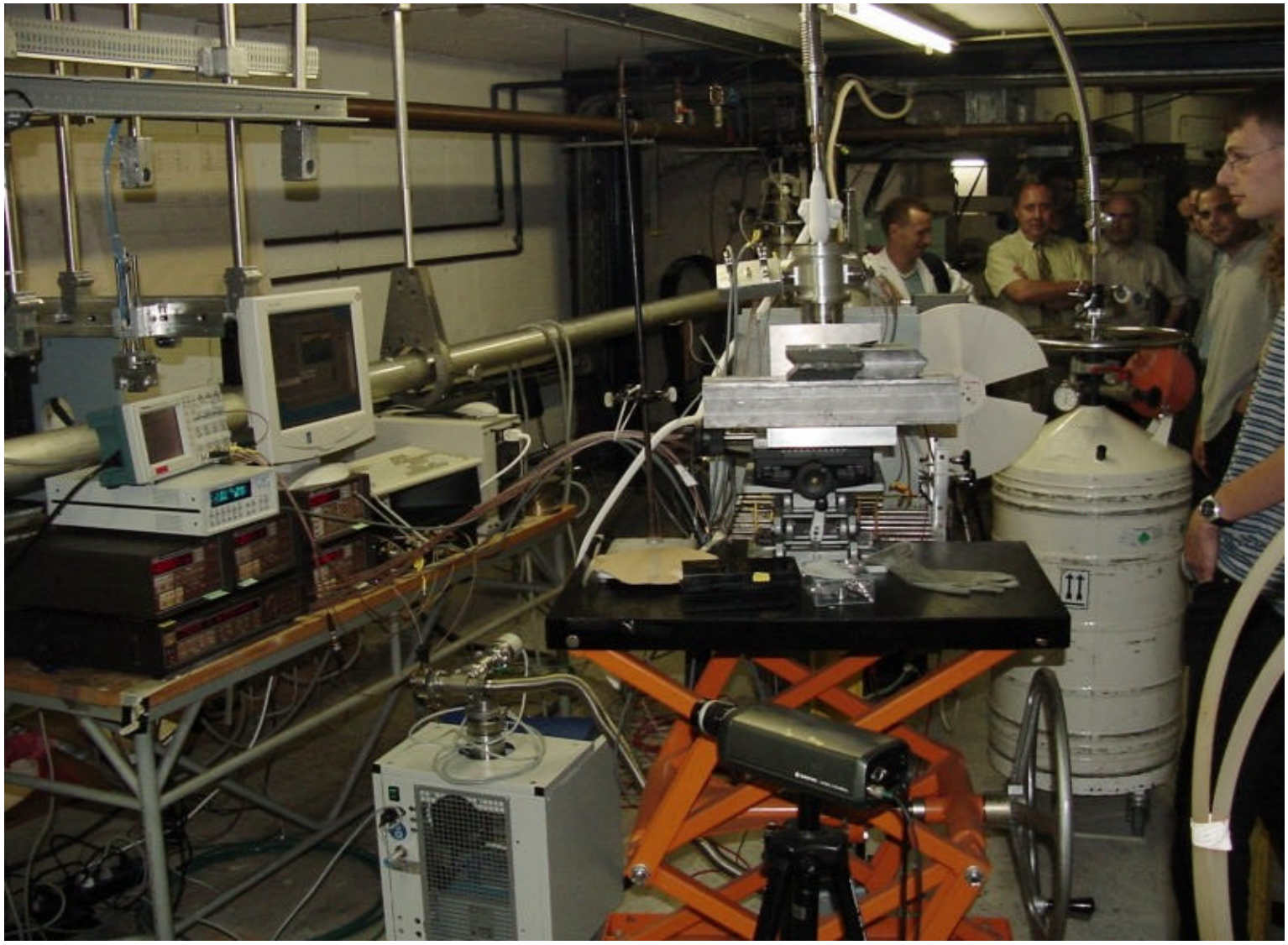
CRYOGENIC IRRADIATION SET-UP –1

CRYOGENIC IRRADIATION SET-UP - 2



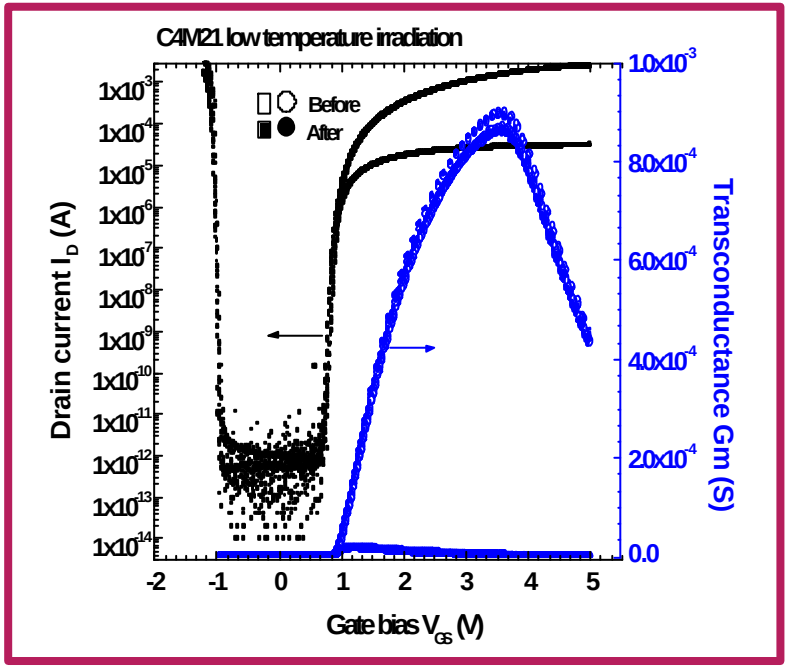


CRYOGENIC IRRADIATION SET-UP - 3

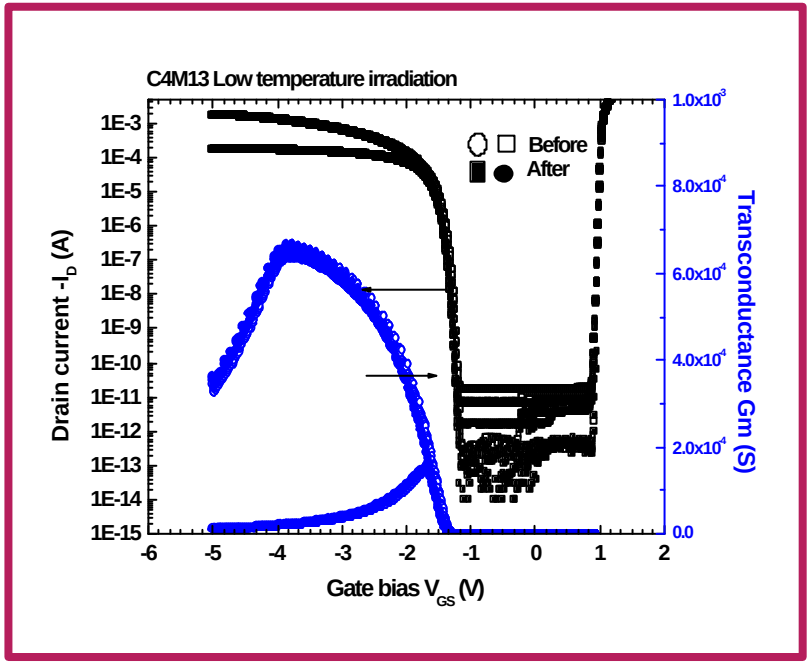


RESULTS: TRANSISTORS

nMOSFETs: I_D-V_{GS}

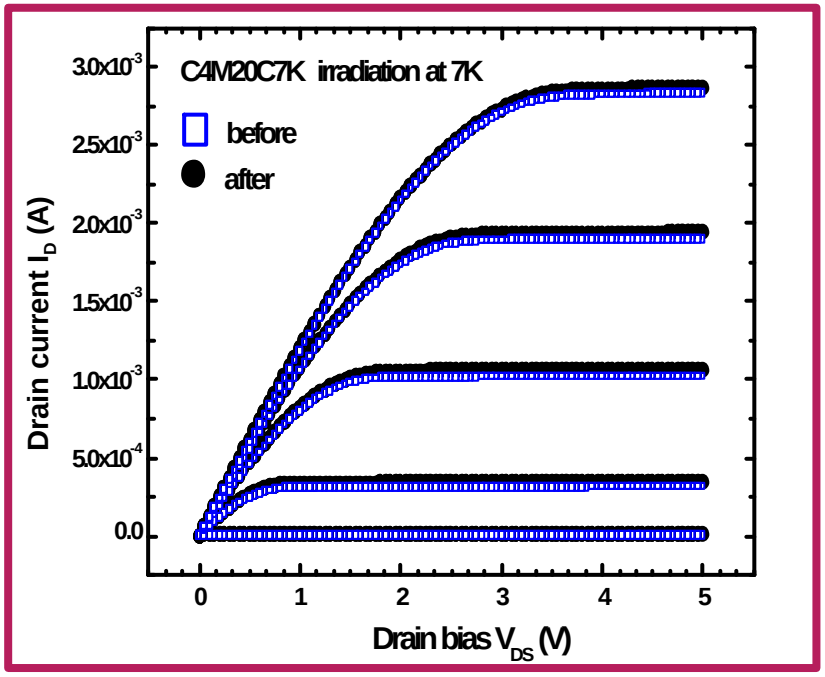


pMOSFETs: I_D-V_{GS}

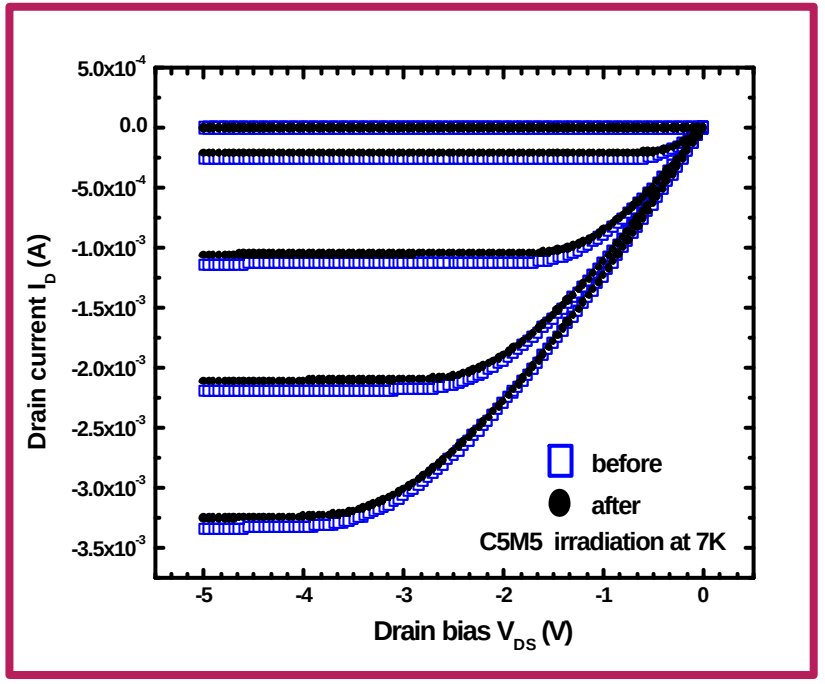


RESULTS: TRANSISTORS

nMOSFETs: I_D-V_{DS}



pMOSFETs: I_D-V_{DS}

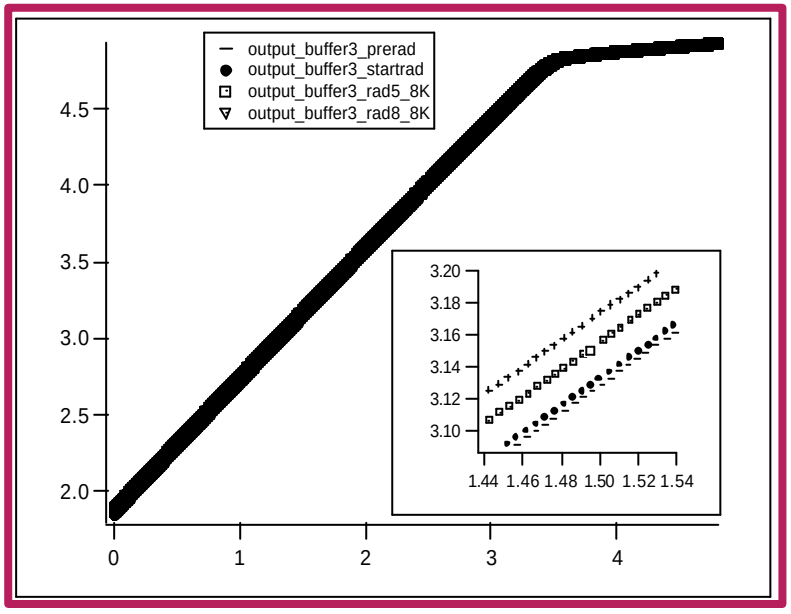


RESULTS:TRANSISTORS

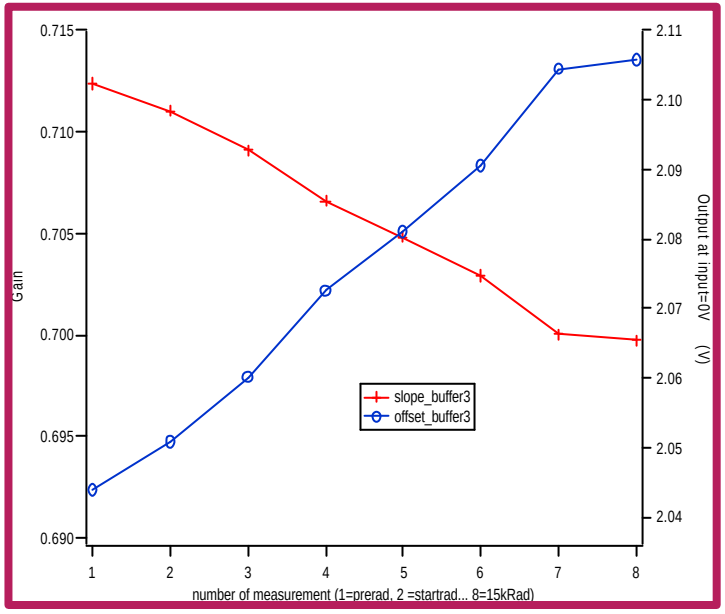
- The parameters changes of the transistors up to a total dose of 30 krd(Si) are small.
- No kink effect is oberved for the n-channel transistors.
- Edge related subthreshold leakage can disappear after a LHT gamma irradiation.
- ESD protection working at 300 K no more operational at 4.2 K.

RESULTS: CIRCUIT g's

p-MOS buffer

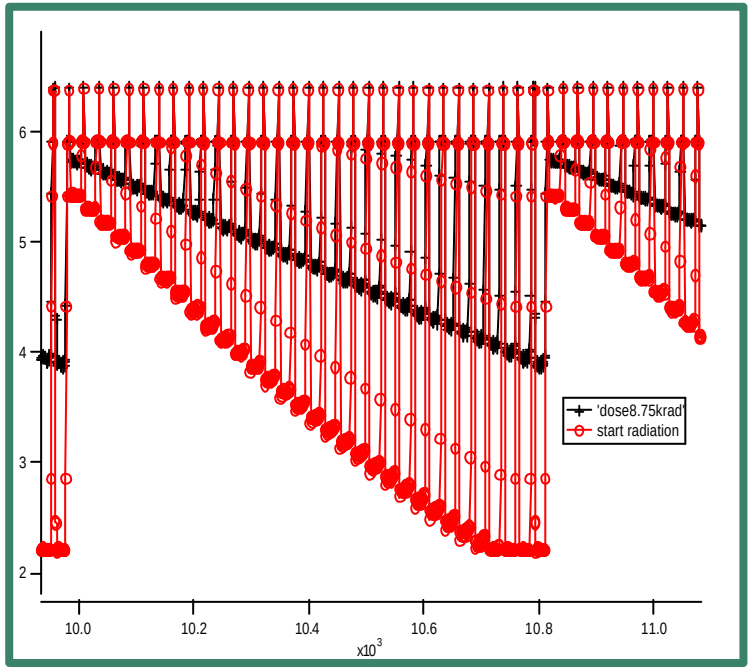


Gain and offset

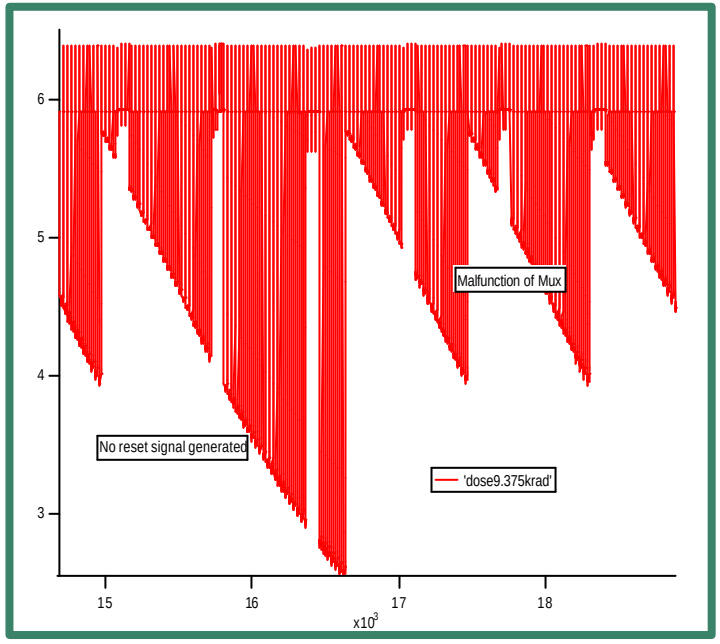


RESULTS: CIRCUIT PROTONS

PACS output signal up to 9 krd(Si)

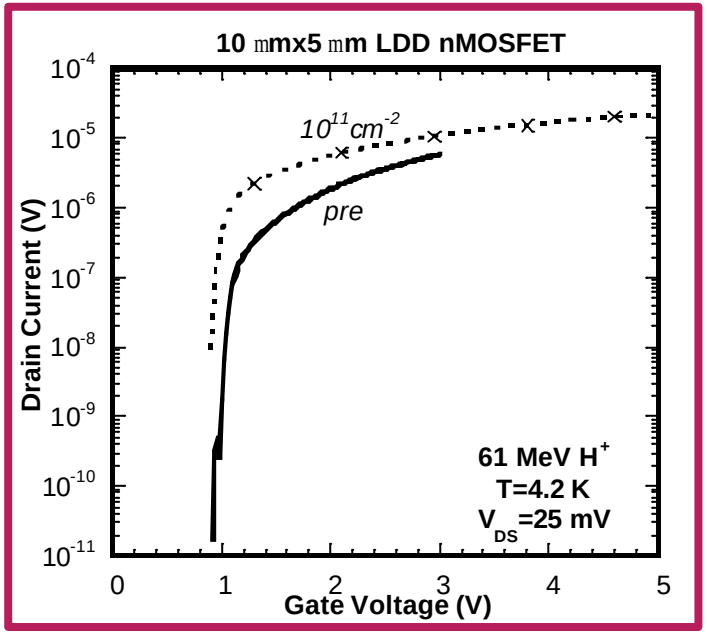


PACS output MUX signal stuck at zero



DISCUSSION

Room temperature irradiation



- **Earlier room temperature exposures demonstrated more pronounced parameter changes.**
- **On transistor level, no significant differences between g's and protons.**

CONCLUSIONS

- It has been shown that the exposure temperature plays an important role. In other words, one can not rely on room temperature radiation testing to predict the radiation response at cryogenic temperatures.

- Tests on transistor level can help to understand the physical degradation mechanisms, but are insufficient to explain the circuit behaviour.

- It has been shown that for space applications both cryogenic g and proton testing are necessary. Circuit failure at LHT was only observed under 60 MeV proton irradiation.

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Goal

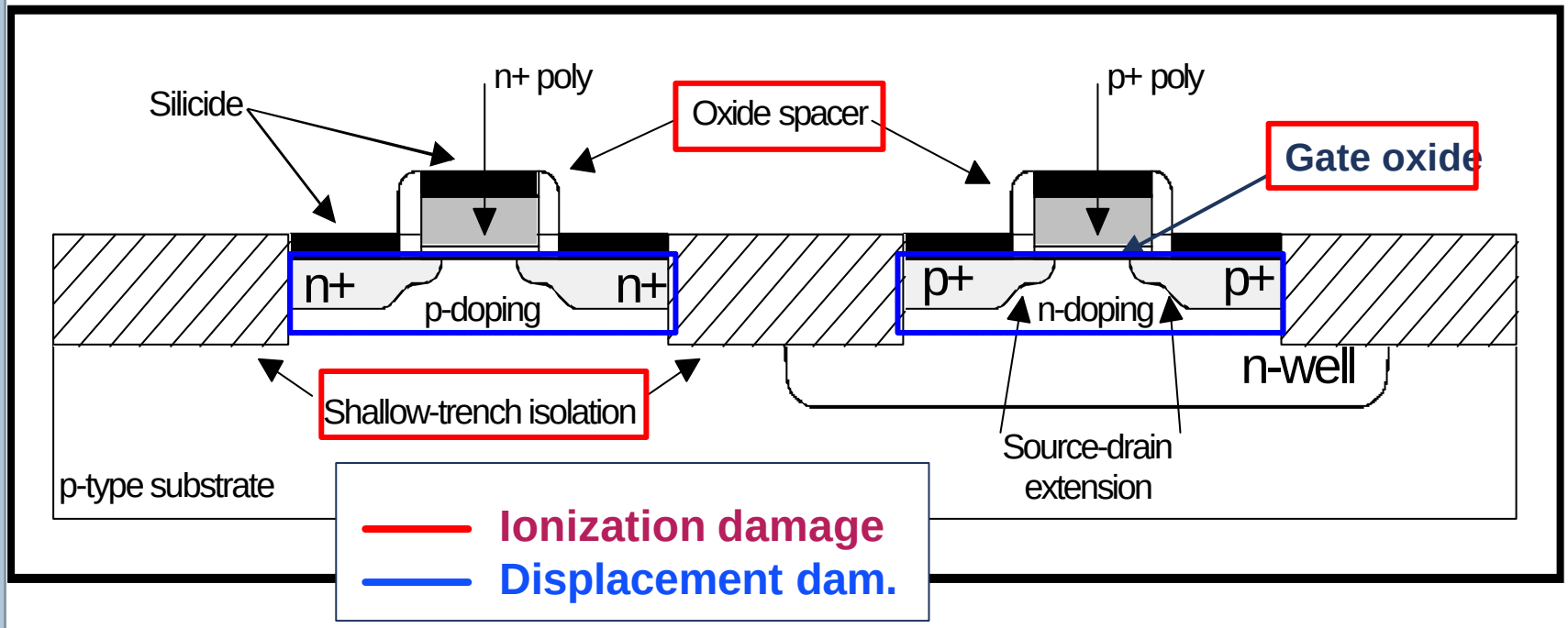
in line with the **Custom Off The Shelf (COTS) philosophy**, we investigate the impact of 60 MeV proton and gamma irradiations on the behavior of NO and RNO deep submicron MOSFETs currently fabricated at IMEC in a 0.13 μm CMOS technology with STI based isolation.

Study of the impact of irradiation **on :**

- Shallow trench isolation
- Gate oxide reliability
- Electrical device parameters

0.13 mm CMOS Technology

- Shallow trench isolation
- NO and RNO gate oxides
- n+ and p+-doped polysilicon gates (low threshold)
- Source-drain extensions LDD (hot-electron effects)
- Self-aligned silicide (spacers)
- Non-uniform channel doping (short-channel effects)



Irradiation Matrix

Devices

Two wafers namely **wafer 7 (NO)** and **wafer 9 (RNO)** from lot PLINE 9008. Fabricated in a 0.13 µm technology : **STI**, **2 nm gate oxide**, **150 nm polysilicon gate** and **80 nm nitride spacers.**

W =10 µm and L = 0.08 µm till 10 µm mounted in 24 pins dual-in-line packages for the irradiation under bias (V_G=1.5V)

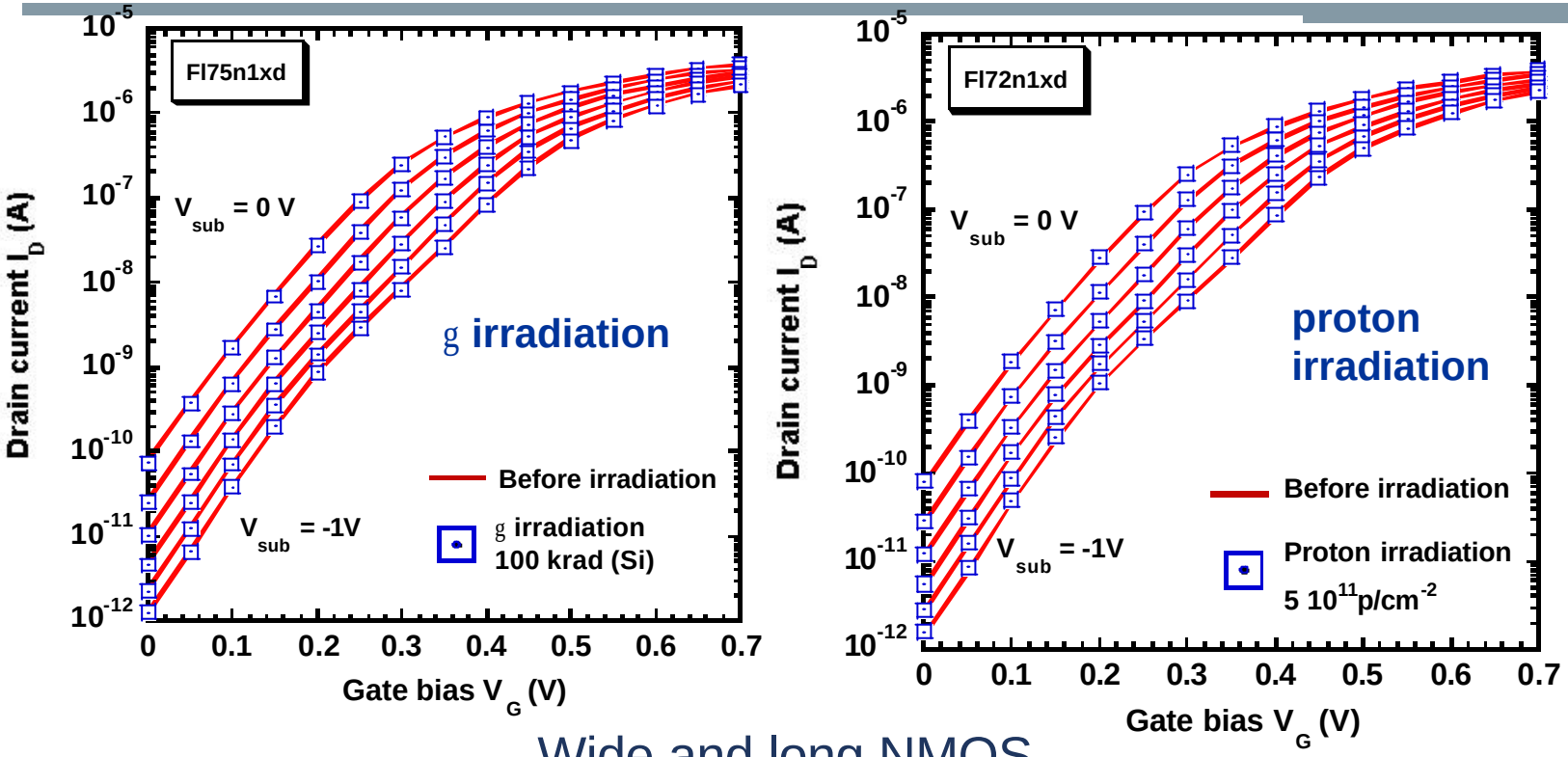
+

Pieces of wafer with L-arrays and W-arrays for the irradiation without bias.

Electrical test conditions

1/ $I_D(V_G)$ measurements for V_{DS}=25 mV (ohmic regime) and 1.5 V (saturation regime)
2/ $I_D(V_{DS})$ for different V_G
Measurement performed for V_{BS}=0 V;
+ Additionnal measurement with I V_{BS}I=0 to 1V
+ 1/f noise, gated diode, HF CV

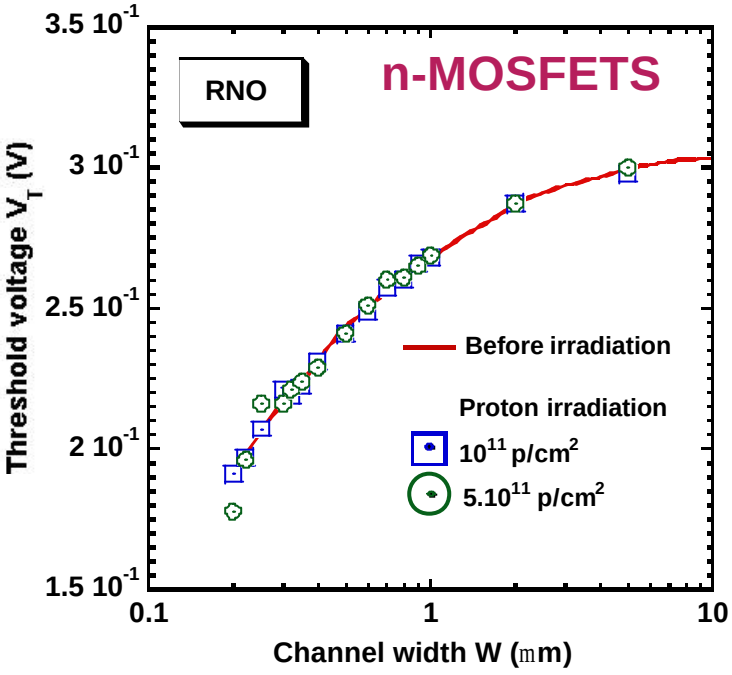
No Subthreshold "hump" in IMEC STI module

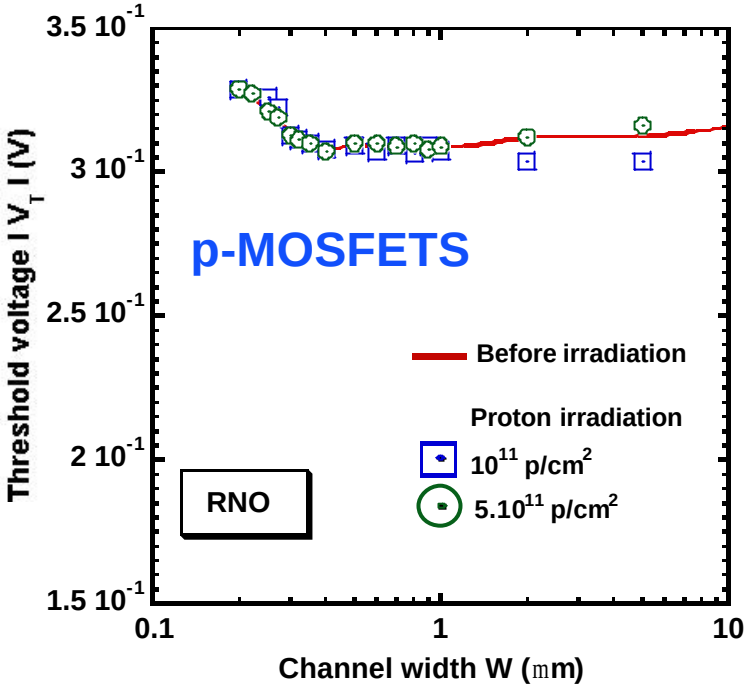


Wide and long NMOS device **(W/L=10mm/10mm)** is free of sub-threshold hump

No strong sub-threshold hump observed in IMEC STI module for n-MOS devices at high (negative) substrate bias after irradiation

Threshold voltage of W-arrays does not show evidence for radiation induced degradation

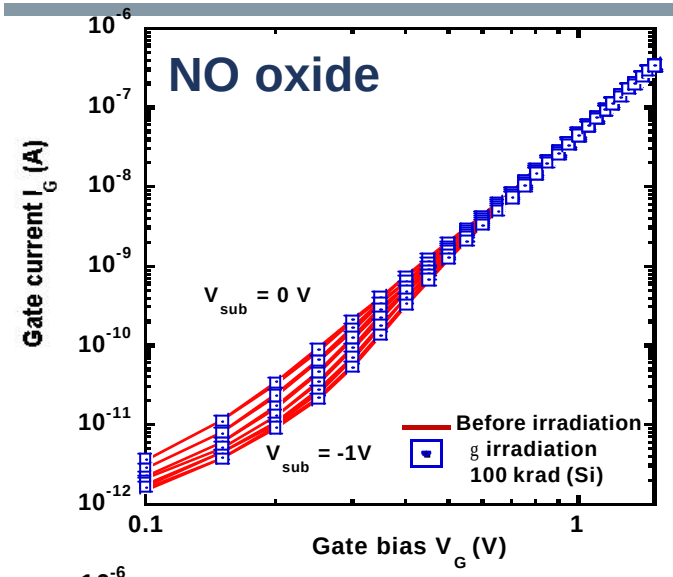


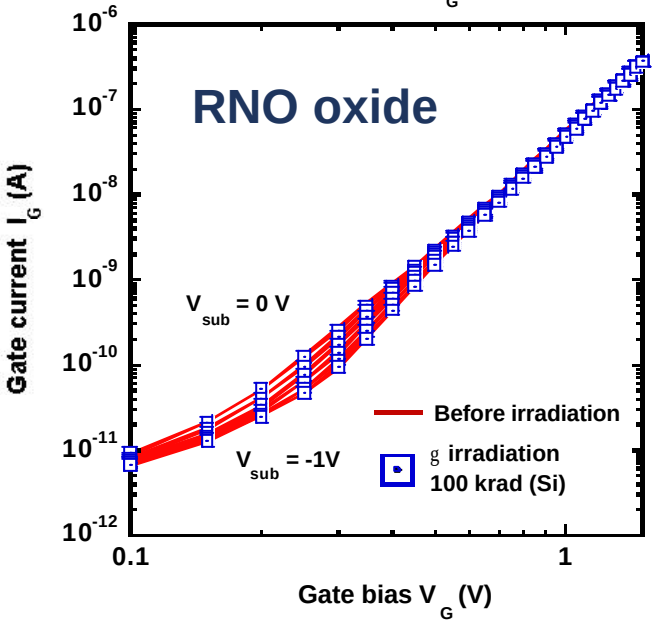


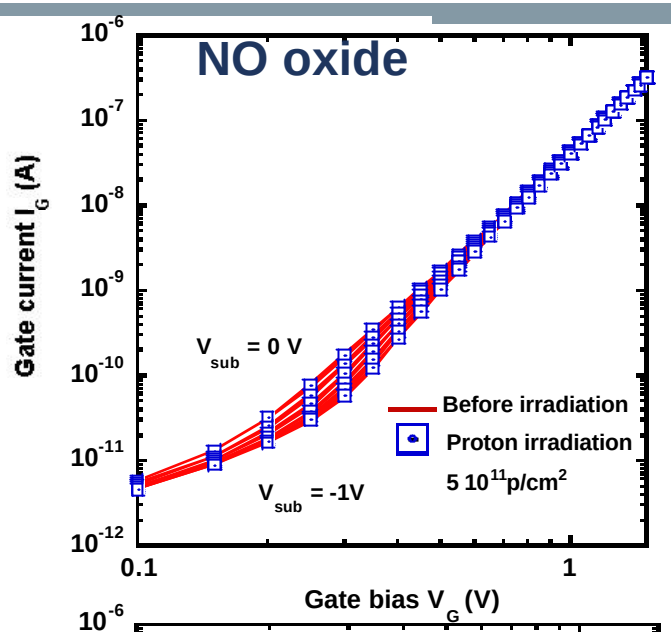
IMEC STI module is a good candidate for integration in hard technology

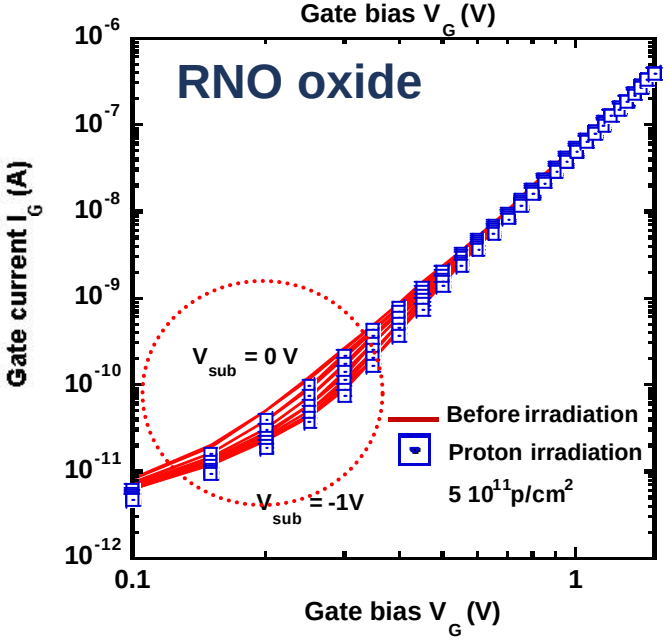
until a total dose of 100 krad(Si)

Gate current does not show evidence for radiation induced degradation



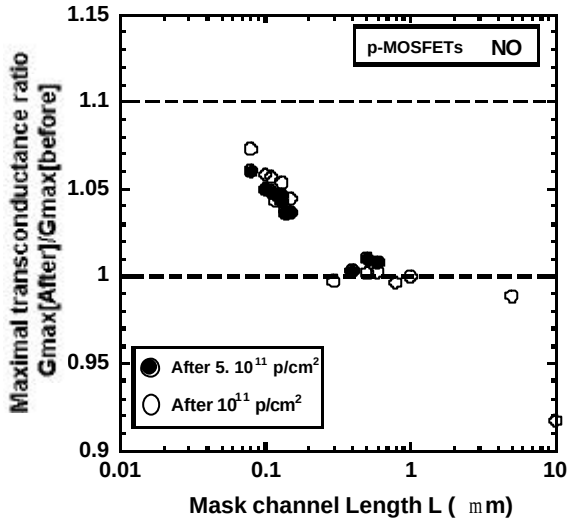


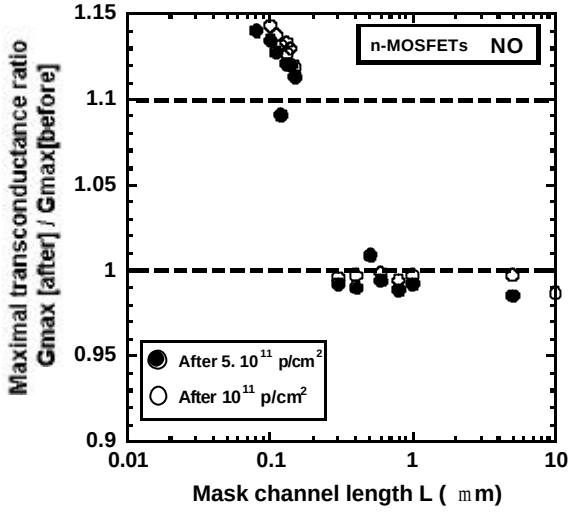




Irradiation impact on electrical parameters

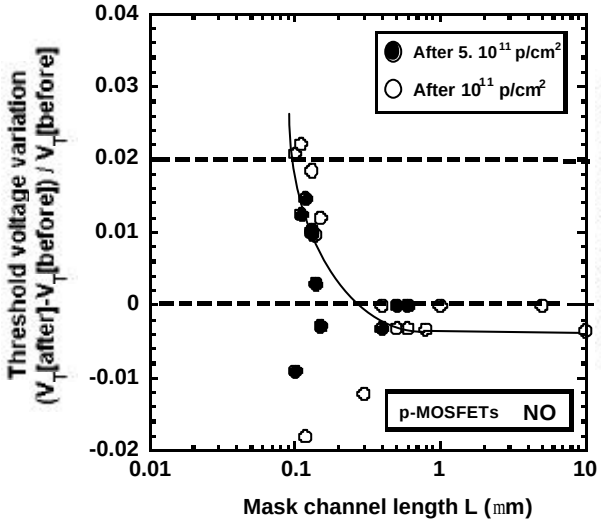
Devices irradiated under bias I V_G I=1.5V

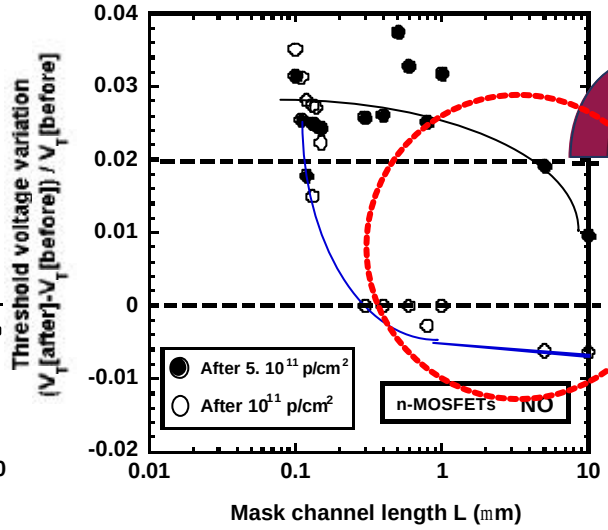




NO

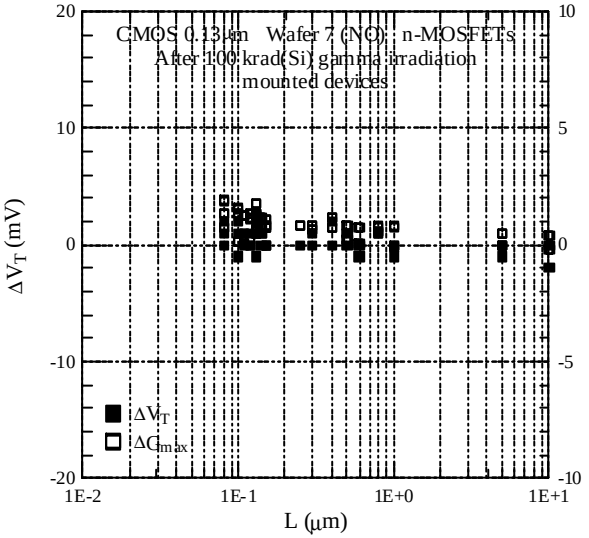
- Smaller variation for p-MOSFETs
- Increase of the G_m and V_T for small channel length

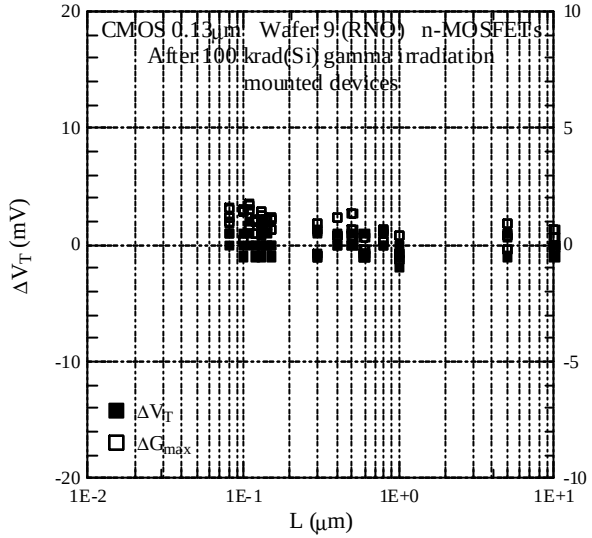


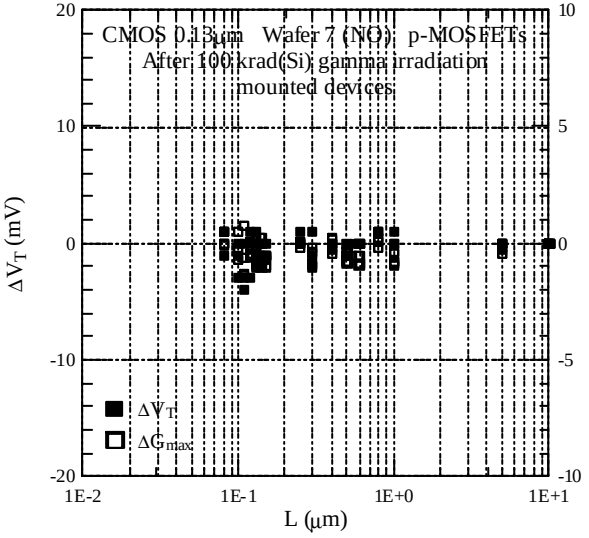


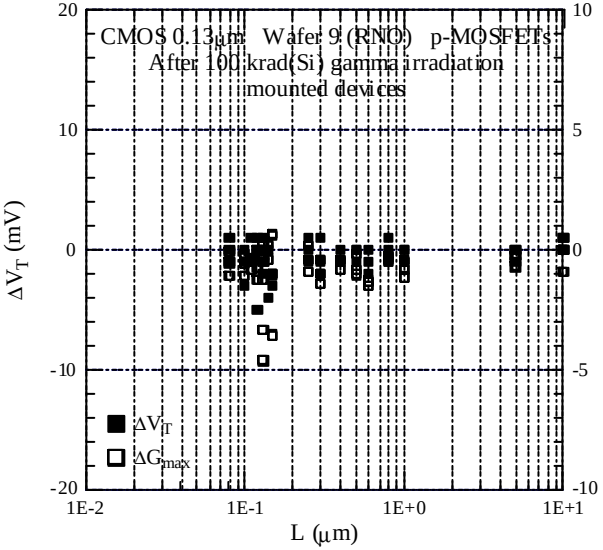
Increase of V_T for long device for the highest fluence

100krad(Si) g irradiated devices under bias do not show significant variations





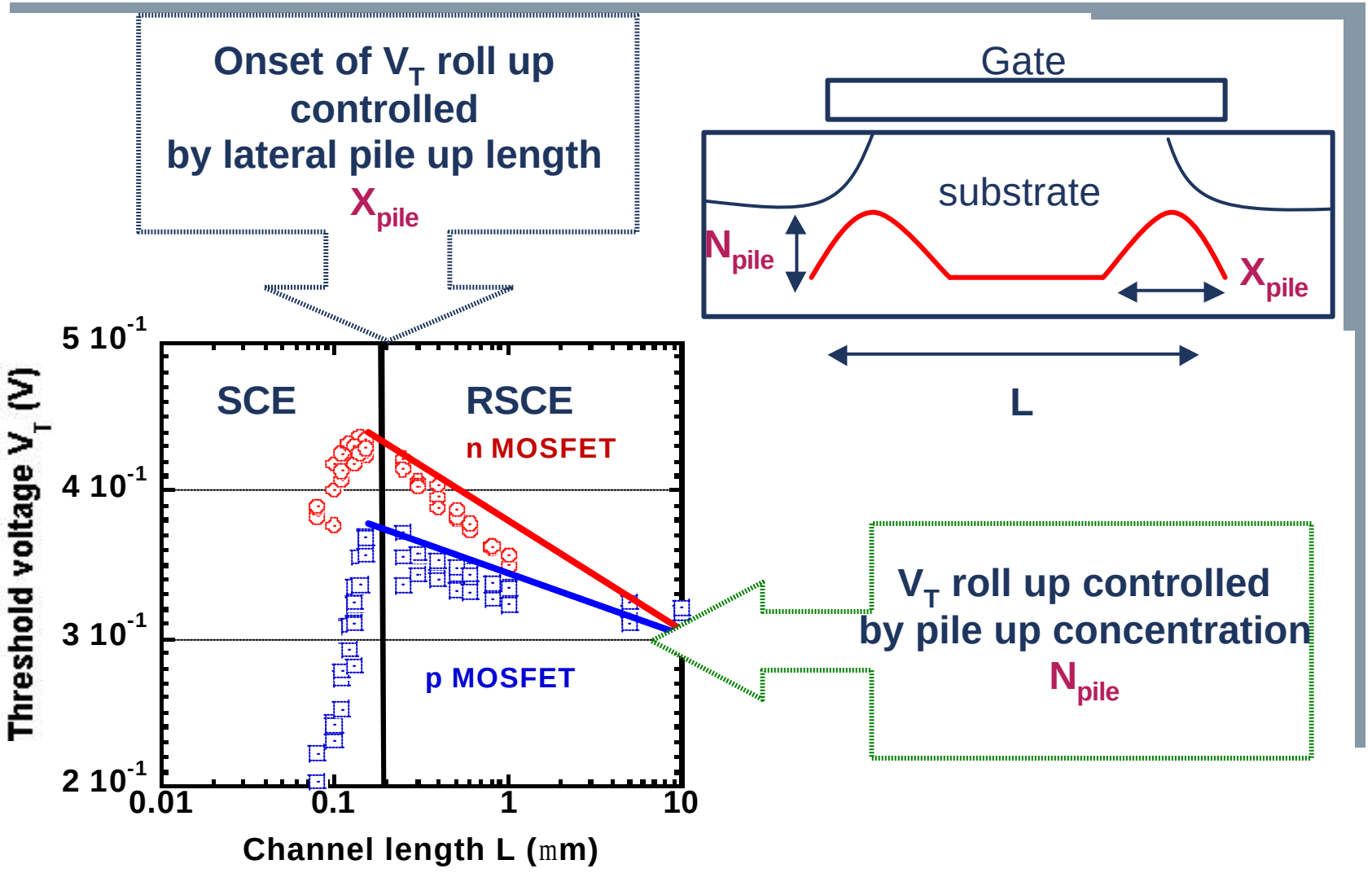




No ionization damage

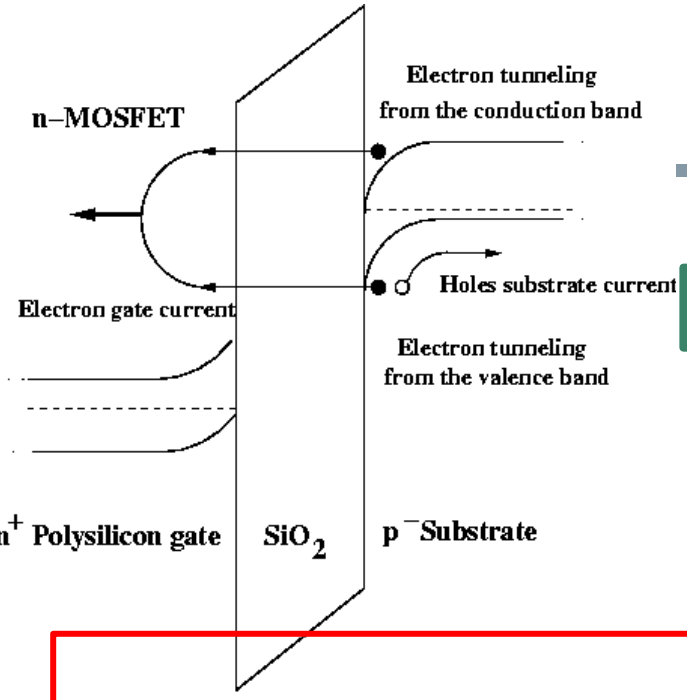
Variations after Proton irradiation are probably due to damage in the substrate

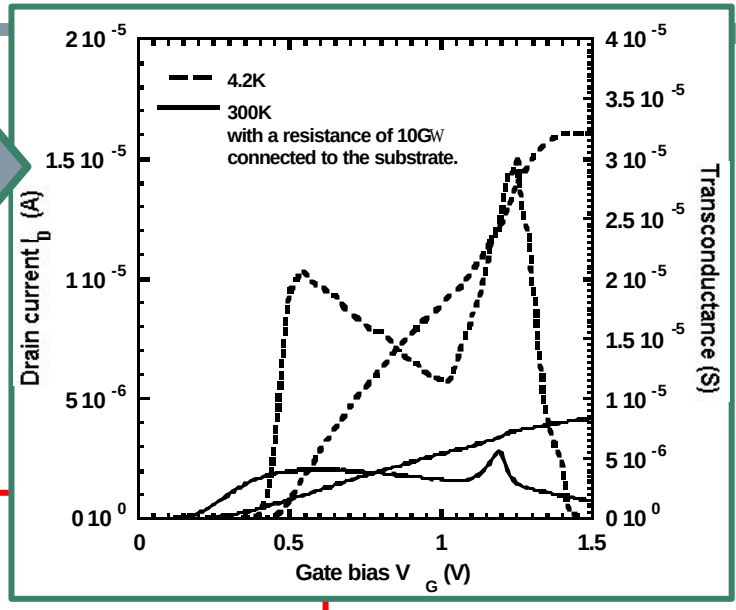
Doping profile and Reverse Short Channel Effect

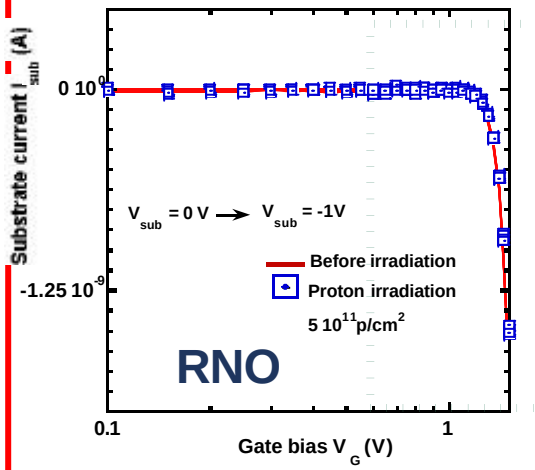


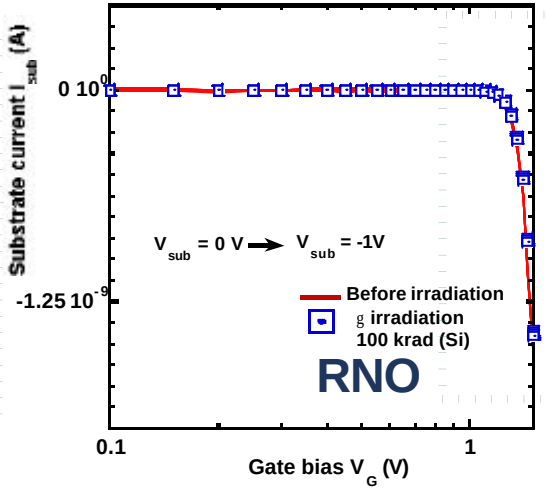
Doping profile variation induced by displacement damage ?

Substrate current and self-biasing substrate









Common gate structure !

No variations in the substrate current

Conclusions

- This scaled technology can withstand proton and gamma space irradiation

- I-V, C-V and noise measurements show no substantial degradation of the STI and the gate oxide for **IMEC technology**

- The transconductance increases for short channel n-MOSFETs irradiated under bias

- The variations of G_m an V_T of n-MOSFETs irradiated without bias show complex rebound behavior

These small variations could be related to substrate damage and specific to the common gate test structure ?

Devices from IMEC 0.13 μm technology are radiation hard

But need for experimental results on circuit level (SEU)

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Motivation

- One of the advantages of SOI CMOS is its inherent resistance against ionization damage (SEU). It is an obvious candidate for space applications, in view of the COTS philosophy.

- Potential drawback is the charging of the buried oxide by Total Ionizing Dose (TID) degradation (n-channel transistors).

- Deep submicron CMOS is radiation hard due to scaling of the gate dielectric. What about new radiation damage mechanisms?

Experimental 1

Devices

- MOSFETs fabricated in a 0.13 μm Partially Depleted SOI CMOS technology.
- UNIBOND wafers; t_f=100 nm; t_{box}=400 nm; t_{ox}=2.5 nm.
- Splits with and without halo or pocket implantation have been studied.
- W=10 μm; common gate and source, no body contact.

Experimental 2

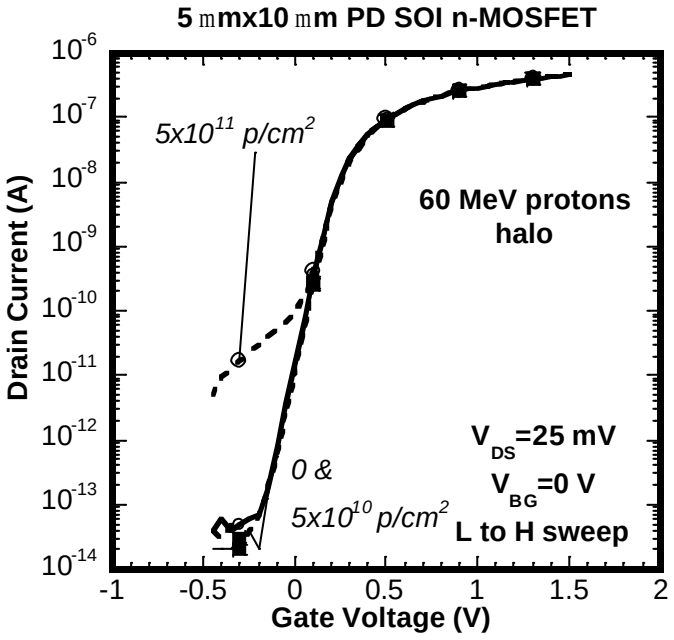
Irradiation Conditions (unbiased)

Beam/Particle	Energy (MeV)	Dose or Fluence krd(Si) or p/cm^2	Facility
Protons	**60**	**5x, 10x, 50x10^{10}**	**Cyclone**
Protons	7.5	2.7x10^{12}&2.7x10^{13}	Demokritos
γ	1.066	13.5&100 krd(Si)	Louvain-L-N

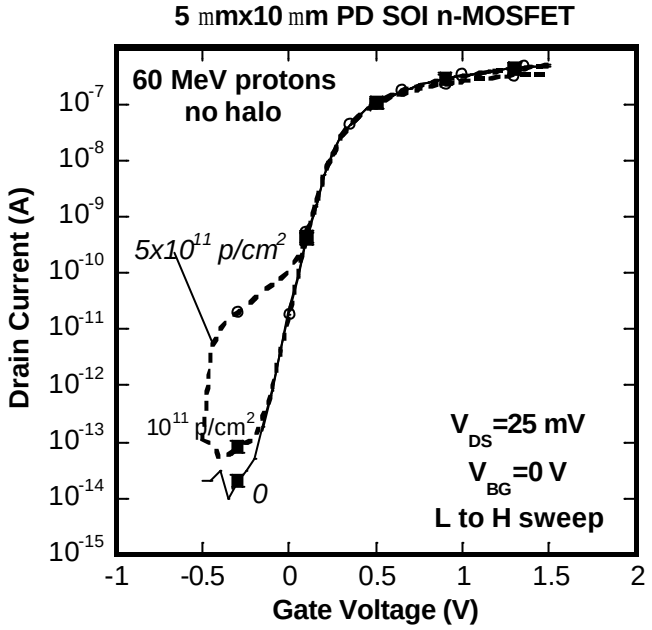
Results

Input characteristics for long n-channel transistors

With halo



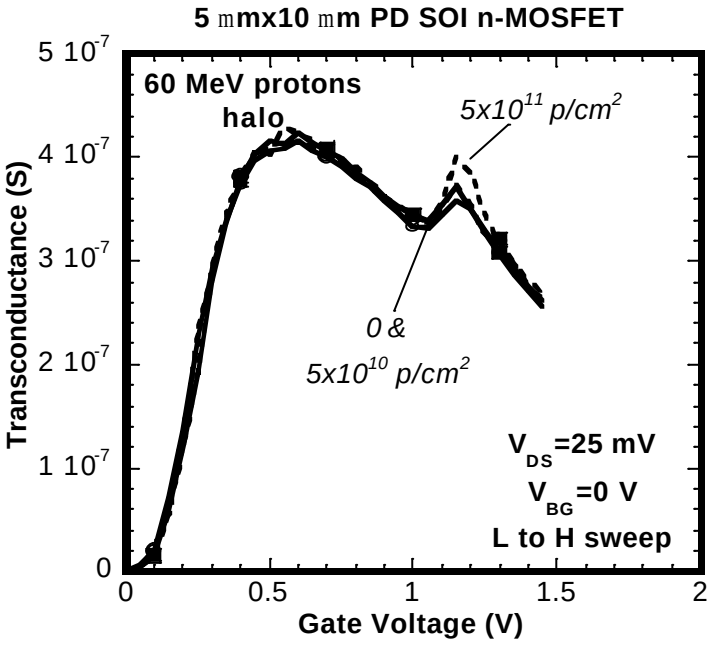
No halo



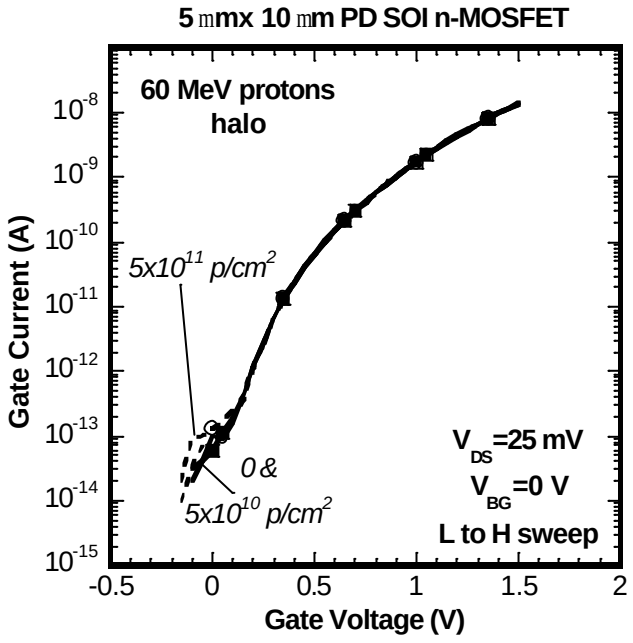
Results

Input characteristics for long n-channel transistors

LKE peak



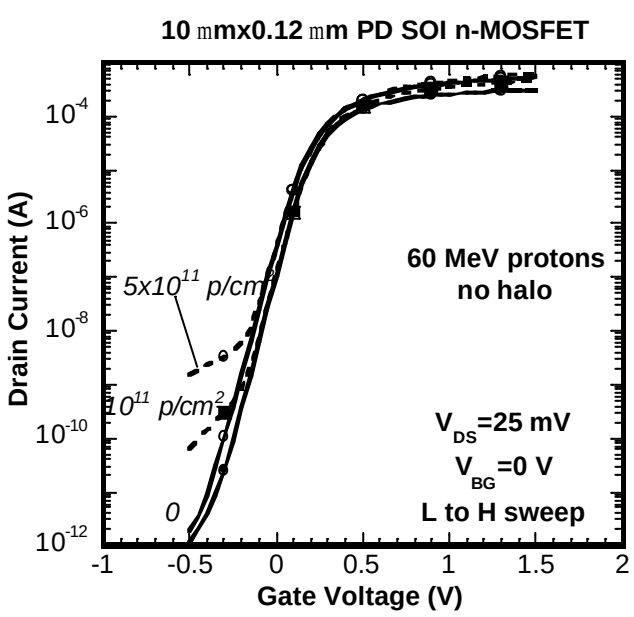
Gate Current



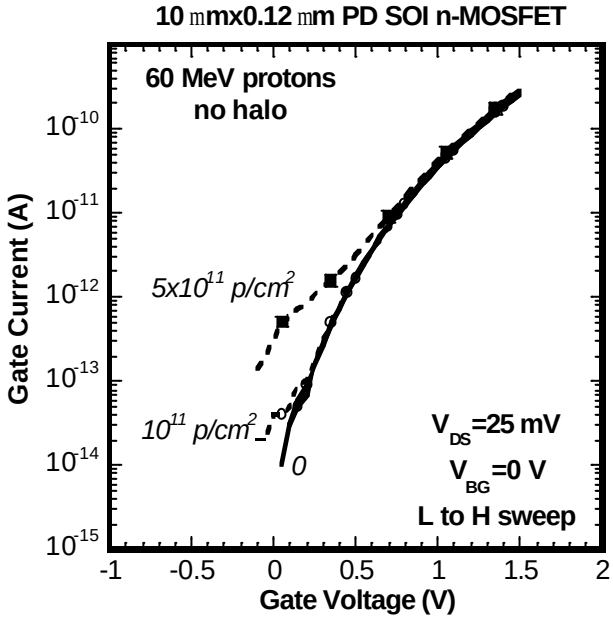
Results

Input characteristics for short n-channel transistors

Subthreshold Leakage



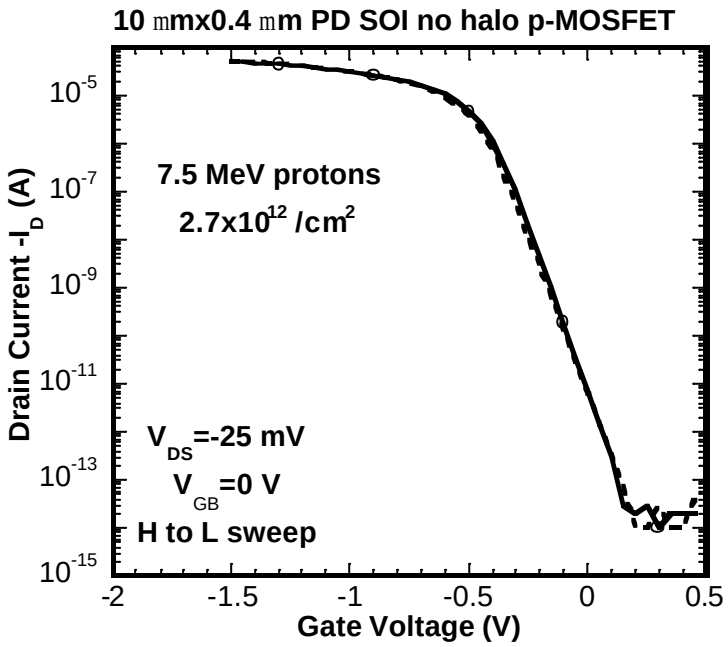
Gate Current



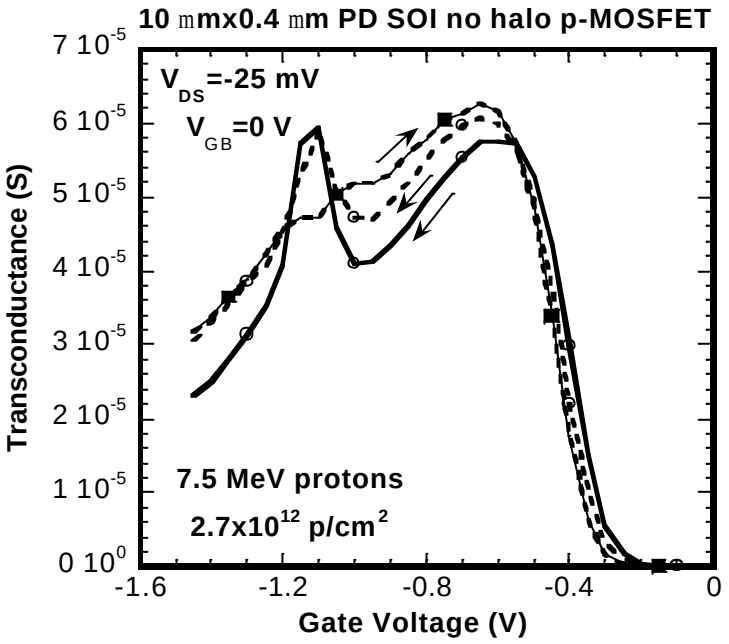
Results

Input characteristics short p-MOSFET

Subthreshold regime

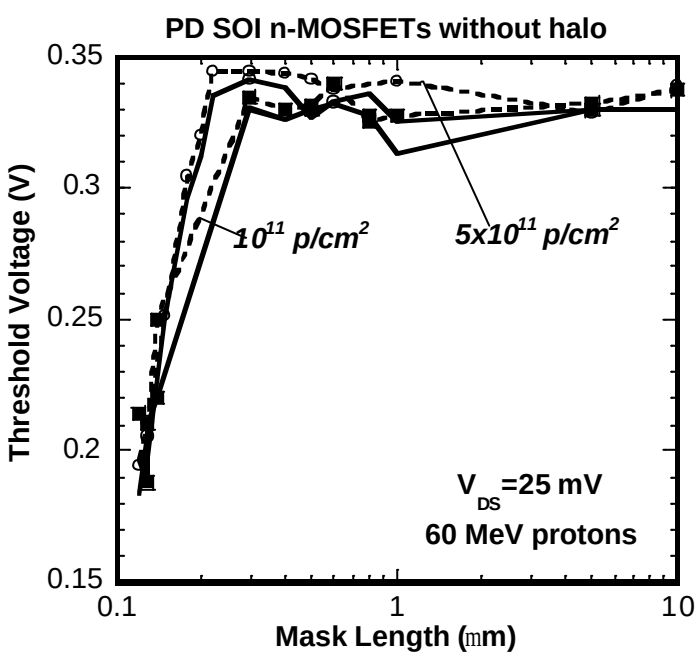


LKE peak

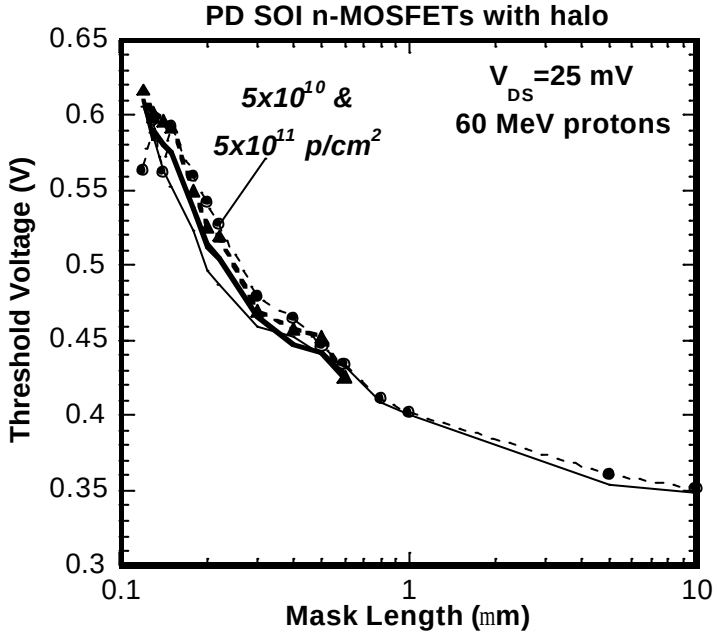


Results: Threshold Voltage

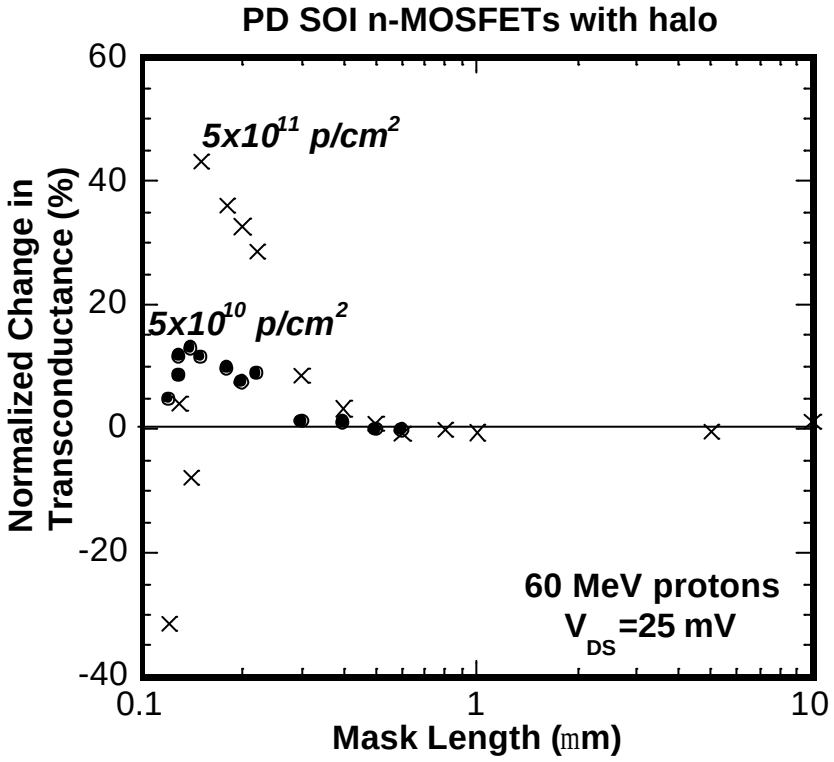
No halo



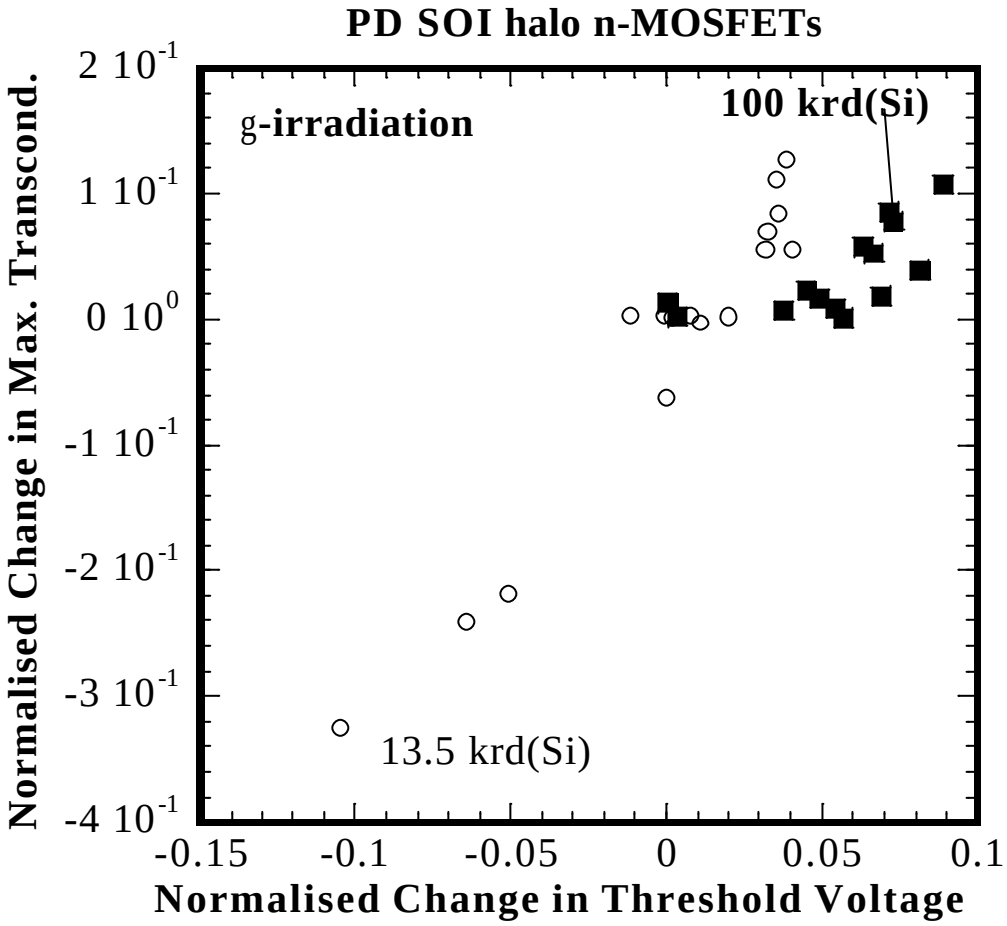
halo



Results: Transconductance



Discussion: Length Dependence



Summary and Conclusions

- Overall, only small changes are induced in the static device parameters. The PD SOI CMOS is suitable for space applications from a viewpoint of TID damage.

- Charging of the BOX induces an edge leakage current component in the subthreshold regime for the n-MOSFETs.

- The observed changes show a typical length dependence, which points to the two-dimensional nature of the induced damage. This also follows from the impact of the halo on the degradation. Without halo, a more pronounced parameter change is usually found.

OUTLINE

- Project structure
- Results of the liquid helium temperature irradiations (HERSCHEL components)
- Results of the radiation assessment of advanced components
  - 0.13 μm bulk CMOS
  - 0.13 μm PD SOI CMOS
- **Outlook**

OUTLOOK

- Radiation assessment of 90 and 65/45 nm CMOS (digital).
- Radiation assessment of dual-gate oxide for 90 nm SoC CMOS: 1.5 and 2 nm oxides grown on F and N ion implanted silicon.
- Radiation assessment of hi-k gate MOSFETs (45 nm node): HfSiON gates with 1.7-1.8 nm EOT.
- FinFETs (advanced SOI); high-mobility FETs (strained silicon layers; Ge-FETs).

Summary and Conclusions

- Evidence for some new radiation damage mechanisms was found: after 60 MeV protons, RILC could be observed.

- There is also a change in the so-called Linear Kink Effects (LKE's). The switch-off transients become faster in this regime, due to the additional edge leakage. The same applies for the associated Lorentzian noise overshoot.

Acknowledgements

- Many thanks to the IMEC Project Team, including Cor Claeys, A. Mercha, J.M. Rafí, M.L. David, Y. Creten, J. Putzeys, P. De Moor and C. Van Hoof.

- We also appreciated very much the assistance of G. Berger and his Colleagues at Cyclone cyclotron during the proton irradiations. A. Mohammadzadeh is acknowledged for his continuous and stimulating interest and support in the radiation activities. He also organized the g-irradiations at ESTEC together with R. Nickson.