Radiation Test-Bed for High Capacity Memory Components

Final Presentation of ESTEC Contract No. 11356/95/NL/FM, CCN-7

TU Braunschweig

Test-Bed Design Approach

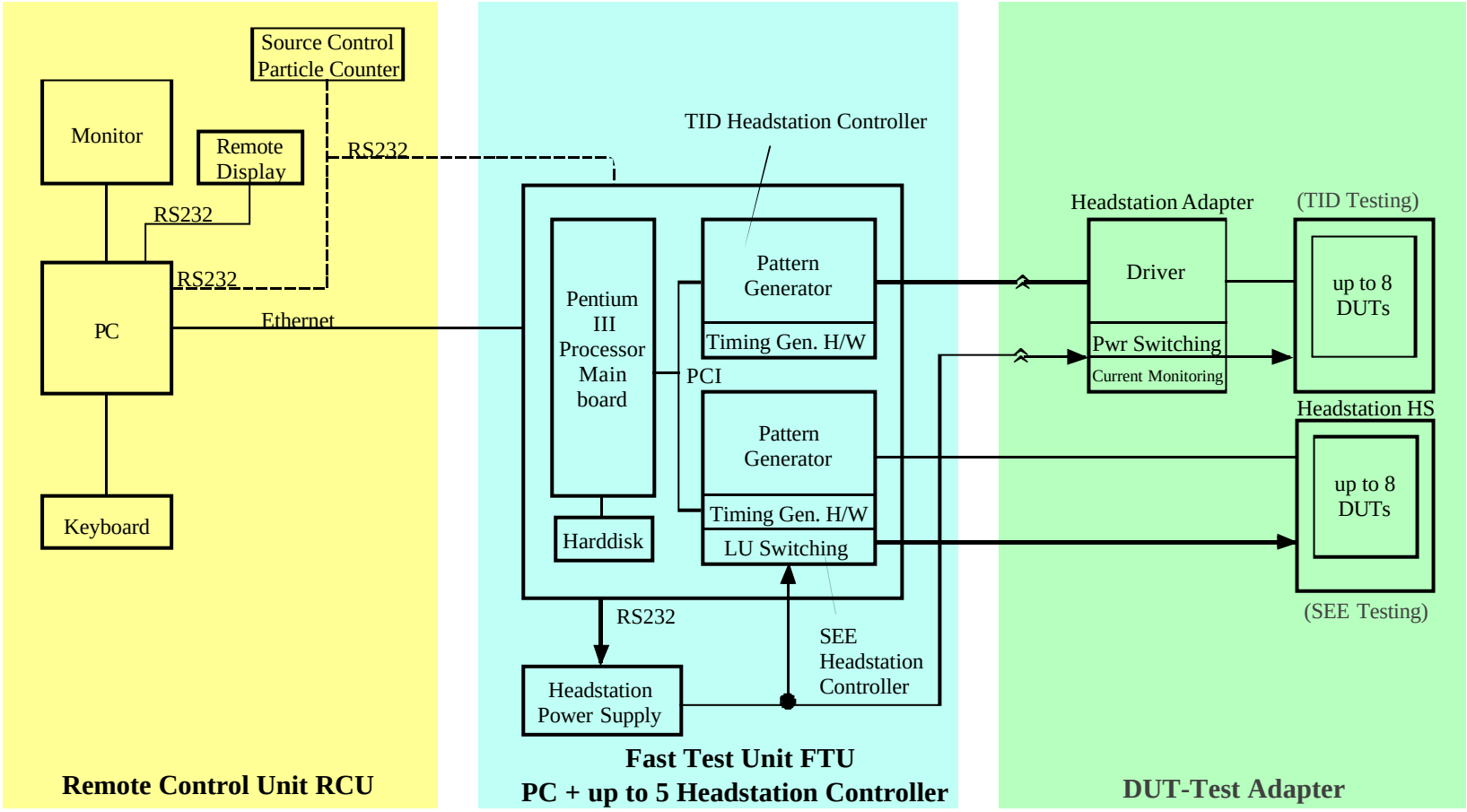
Test-Bed design mainly driven by three requirements:

- in situ testing
  - mandatory to detect and isolate special functional errors of state of the art devices, e.g. Flash Memories, FIFO´s etc
- real time event detection and recording
  - supports isolation of special failure types, e.g. cluster errors (simultaneous multibit errors) or partial SEL
  - supports complete testing of large capacity devices within reasonable test time
- flexible and easily adaptable platform
  - more and more sophisticated „memory systems on a chip“ are available and a test bed needs to be adaptable to these devices with special functions in a short time frame

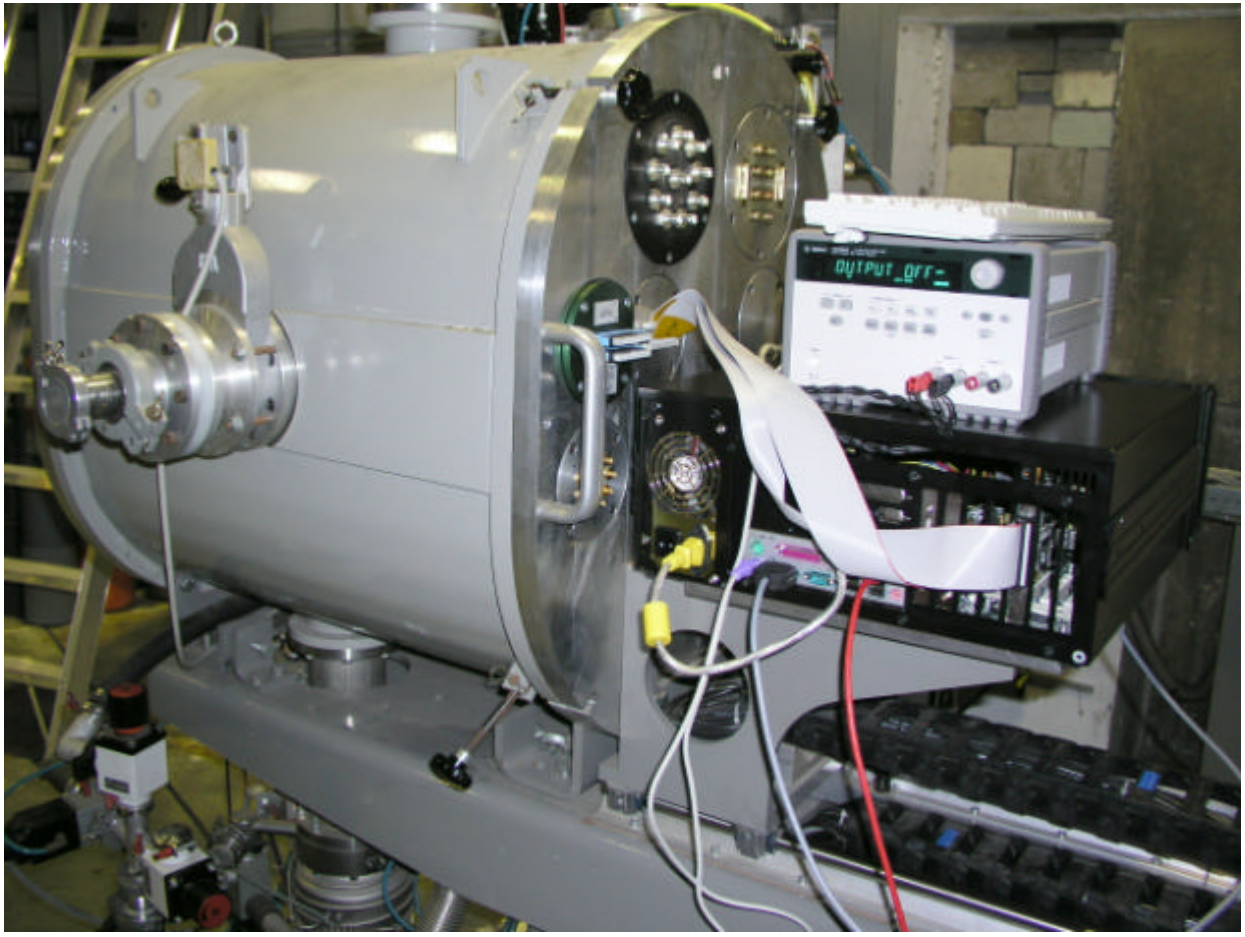
Derived Design Characteristics

- PC based System with special Plug-In Cards to implemement real time functions (Fast Test Unit)
- TID and SEE Test capabilities and requirements achievable with the same basic equipment
- Adaptable Device Control and Test Patterns implemented in Firmware within configurable high performance FPGA´s
- Remote control of in-situ tests supported via network
- Quick-Look data analysis to support in-situ tests

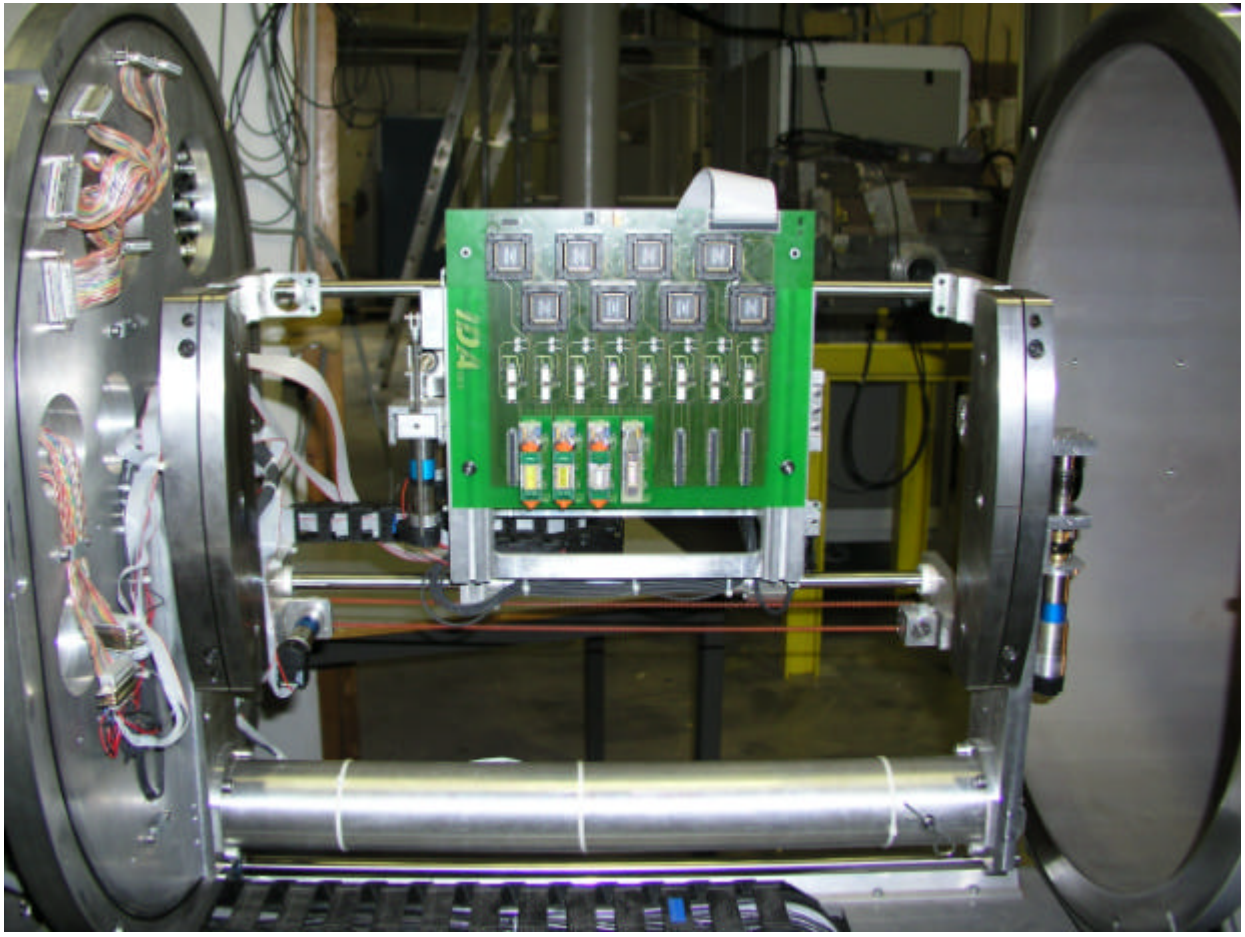
Block Diagram of In Situ Radiation Test Bed



Fast Test Unit



SEE Headstation with 4 DUT´s



Remote Control Unit

Performance Characteristics

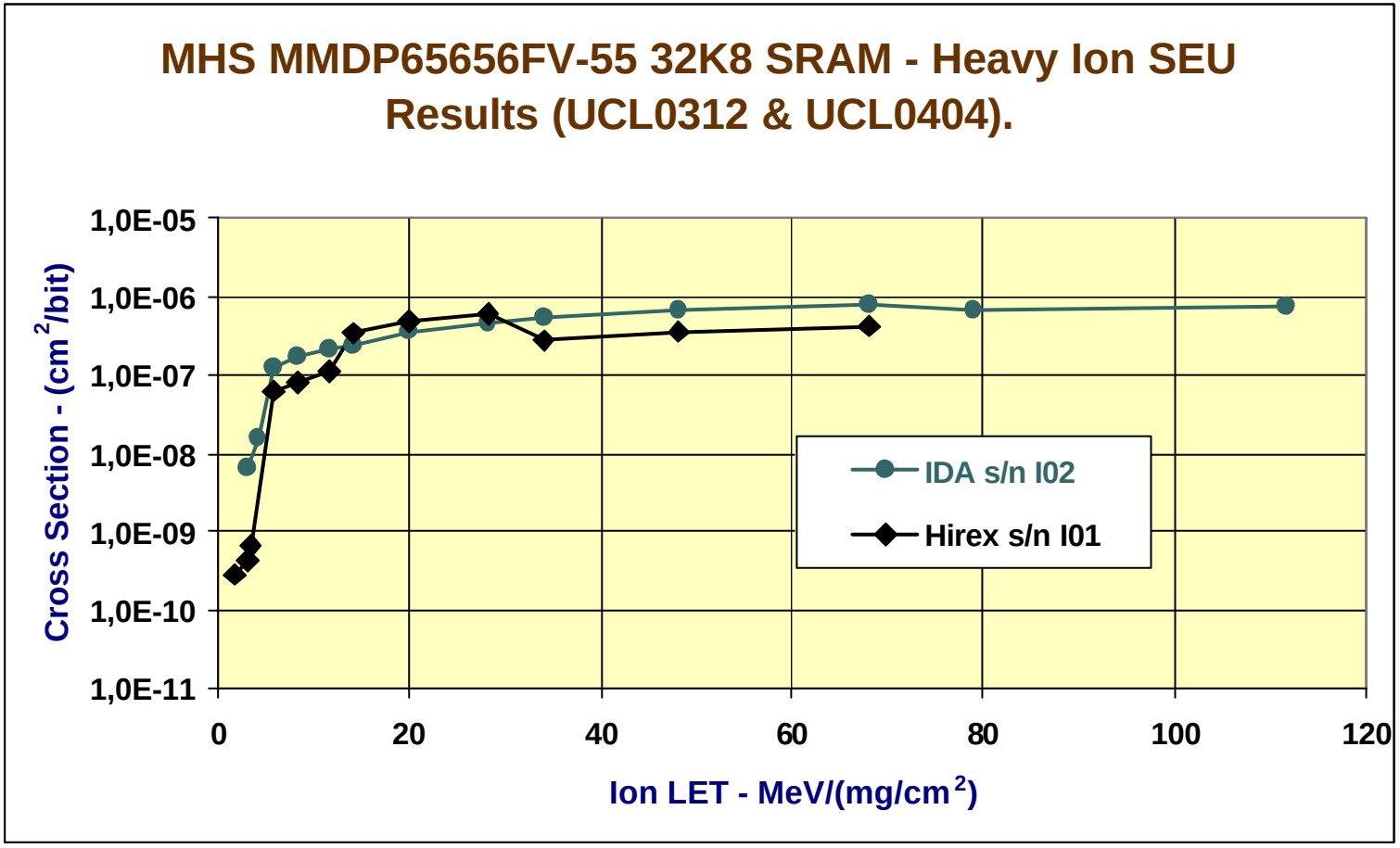
Address Pattern	Read Background, Write Background, Chessboard, Marching, MOVI,…
Data Pattern	Constant (128 bit), Counting (64 bit), Pseudo-Random(64 bit),…
Error Buffer	128k Error Records
Error Record Storage	limited to harddisk capacity
LU Detection	for both SEE-Test and TID-Tests, threshold adjustable
Current Measurement	1 mA resolution for SEE-Tests, 10µA resolution for TID-Tests
Devices	all kind of memory devices
Data Width	up to 16 Bit
Address Width	28 Bit static, 20 Bit (row) + 20 Bit (column) dynamic
Supply Voltage	2 – 6 Volts
Current	up to 200mA per device
Min. Cycle Time	currently 20 ns, 10ns in update version
Device Count	8 per Headstation, up to 4 Headstations connectable

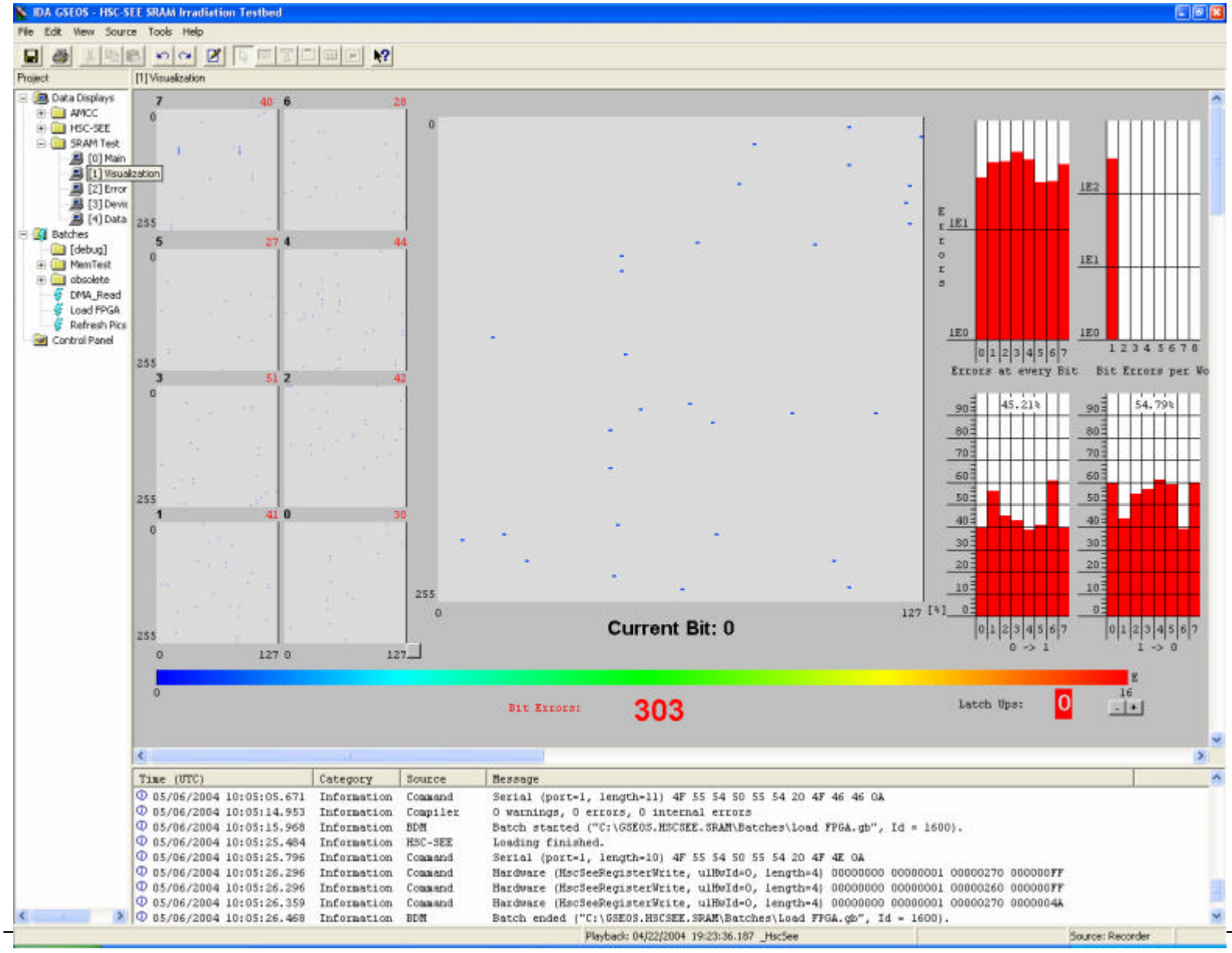
Distance Tester – Headstation	1,5m (SEE-Tests), 5m (TID-Tests)
Distance Tester – Operating PC	up to 100m (standard ethernet)

Test-Bed Verification

- Pre-Verification on System Level
  a) with Laser Beam Test Set up (at IDA)
  b) with Flash Memory Devices (at UCL)
- SEE-Test Verification on System Level
  – SEE Testing of SRAM devices (at UCL)
- TID-Test Verification
  – TID Testing of SRAM devices (to be performed at ESTEC)

SEE Test Results




IDA GSEOS - HSC-SEE SRAM Irradiation Testbed
File Edit View Source Tools Help
Project
[1] Visualization
Data Displays
AMCC
HSC-SEE
SRAM Test
[0] Main
[1] Visualization
[2] Error
[3] Devic
[4] Data
Batches
[debug]
MemTest
obsolete
DMA_Read
Load FPGA
Refresh Pics
Control Panel
Current Bit: 0
Errors at every Bit
Bit Errors per Wo
45.21%
54.79%
0 -> 1
1 -> 0
Bit Errors:
303
Latch Ups:
0
Time (UTC) Category Source Message
05/06/2004 10:05:05.671 Information Command Serial (port=1, length=11) 4F 55 54 50 55 54 20 4F 46 46 0A
05/06/2004 10:05:14.953 Information Compiler 0 warnings, 0 errors, 0 internal errors
05/06/2004 10:05:15.968 Information BDM Batch started ("C:\GSEOS.HSCSEE.SRAM\Batches\Load FPGA.gb", Id = 1600).
05/06/2004 10:05:25.484 Information HSC-SEE Loading finished.
05/06/2004 10:05:25.796 Information Command Serial (port=1, length=10) 4F 55 54 50 55 54 20 4F 4E 0A
05/06/2004 10:05:26.296 Information Command Hardware (HscSeeRegisterWrite, ulHwId=0, length=4) 00000000 00000001 00000270 000000FF
05/06/2004 10:05:26.296 Information Command Hardware (HscSeeRegisterWrite, ulHwId=0, length=4) 00000000 00000001 00000260 000000FF
05/06/2004 10:05:26.359 Information Command Hardware (HscSeeRegisterWrite, ulHwId=0, length=4) 00000000 00000001 00000270 0000004A
05/06/2004 10:05:26.468 Information BDM Batch ended ("C:\GSEOS.HSCSEE.SRAM\Batches\Load FPGA.gb", Id = 1600).
Playback: 04/22/2004 19:23:36.187 _HscSee
Source: Recorder

Summary

- Test Bed provides in-situ and real time SEE and TID Test capabilities for
  - Flash, SRAM (already implemented)
  - SDRAM, DDRAM (to be implemented soon)
  - Special devices (FIFO´s, DPRAM´s already implemented, others TBD)