Test Report

Total Ionisation Dose (TID) Test with a 2-2 Cascaded Delta-Sigma Modulator based on an AMS 0.35 µm process using a Co-60 Gamma-Ray Source

Revision List

Issue	Rev.	Date	Section	Change
D	0	30 Nov. 04		Document created
1	1	17 Dec. 04		Update after IWF/IIS team meeting
1	2	21 Dec. 04	3	Four ADC channels in chip

Related Documents

Test standard: ESCC Basic Specification 22900
Test procedure: IWF-MFA-TP-TID-001
Modulator description: Hartmann et al., A 102 dB dynamic range sigma-delta analog digital converter for wireless sensors

Test Personnel

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1 Introduction

Altogether four meaningful total dose test cycles were performed (@ ESTEC, Noordwijk) to obtain information on the radiation hardness of the Austriamicrosystems (AMS) 0.35 µm CSI/C35B3 CMOS process. The results of this test are the basis for further developments for the Magnetometer Front-end ASIC project (ESTEC/Contract No. 18391/04/NL/HB).
The device under test, a 2-2 cascaded 16-bit switched capacitor delta-sigma converter with 102 dB dynamic range, was designed by the Fraunhofer Institute for Integrated Circuits (IIS). It was manufactured on the 0.35 µm CMOS process provided by Austriamicrosystems. The chip was designed being adaptable to the demands of many sensor types with respect to dynamic range, bandwidth, SNDR and power consumption. During the development no attention was paid on the radiation hardening by design.

2 Device Information

SCC Component No.	N/A
Component Designation	integrated circuit, 2-2 delta-sigma converter, 16-bit
Specification	N/A
Acceptance	N/A
Sample Size	3.8 x 3.8 mm

Number of Samples	3
Project	Technical Assistance in the Development of an Application-Specific Integrated Circuit (ASIC) for Planetary Magnetometer ESTEC/Contract No. 18391/04/NL/HB
Family	Analog-to-Digital Converter
Group	Delta-Sigma
Package	JLCC68 (J-Leaded Chip Carriers – Ceramic)
Process	0.35 µm CMOS 2P3M (CSI)
Manufacturer Name	Austriamicrosystems (AMS)
Manufacturer Address	Austriamicrosystems AG Schloss Premstätten 8141 Premstätten AUSTRIA
Test House Name	Radiation Effects and Component Analysis Techniques Section
Test House Address	ESA/ESTEC Noordwijk Netherlands
Originator Name	Institut für Weltraumforschung (OeAW) Institut für Integrierte Schaltungen (Fraunhofer Gesellschaft)
Originator Telephone	+43/316/4120-566
Facility	TID Facility
Source	Co-60 (Energy 1.173 & 1.332 MeV photons)
Present Activity (Jan. 2004)	1460 Ci (5.4×10^{13} Bq)
Irradiation	Multiple
Dose Rate	70 rad/min
Irradiation Conditions	• Biased and unbiased In-Situ Test • VDD: +3.3 V • Temp.: room temp.

3 Test Configuration

A schematic of the test configuration is shown in Figure 3-1. It consists of the test board for the device under test (DUT), an FPGA board and the measuring equipment which is located outside of the irradiation chamber. The DUT is located on the right side of the PCB. The rest of the electronics is located on the left side where it could be shielded sufficiently. All cables which are connected to the test board are at least 4 m long. The separated FPGA board acts as a buffer and driver unit. A clock generator (1 MHz) and 5 supply voltages

VDDA	3.3 V	analogue supply voltage
VDDD	3.3 V	digital supply voltage
VREFN	1 V	negative reference voltage
VREFP	2 V	positive reference voltage
AGND	1.5 V	chip internal analogue ground

are necessary to power up the chip. VREFP, VREFN and AGND are generated on board using a 5 V power supply.
All currents of the above supply voltages as well as all voltages themselves were monitored by a 10-channel voltage measurement device. The currents were measured over a shunt resistor. To avoid any damage of the DUT and the test circuits, voltage regulators with automatic shut down mechanism (foldback, prepared to shut down at 5x the nominal value)

were included. All voltage and current measurements were collected over GPIB equipped instruments connected to a measurement PC. The digital output data produced by the delta-sigma converter/modulator were measured with a logic analyser.

The tested chip contains altogether four ADC channels (three with current input and one with voltage input including a multiplexer), whereas the voltage input channel was used for the evaluation during irradiation.
The voltage channel consists of an analogue part, a delta-sigma modulator realized by switched capacitor integrators and a digital part which includes an error cancellation logic with 5-bit output and a digital filter providing 16-bit output. The modulator is a cascade of 2 second-order modulators with single-bit quantization. The second modulator digitises the output of the second integrator of the first modulator.
Due to the fact that several external test pins are available, it was possible to measure the irradiation influence on the analogue (modulator) part separately from the combined system including the digital part with the digital filter.

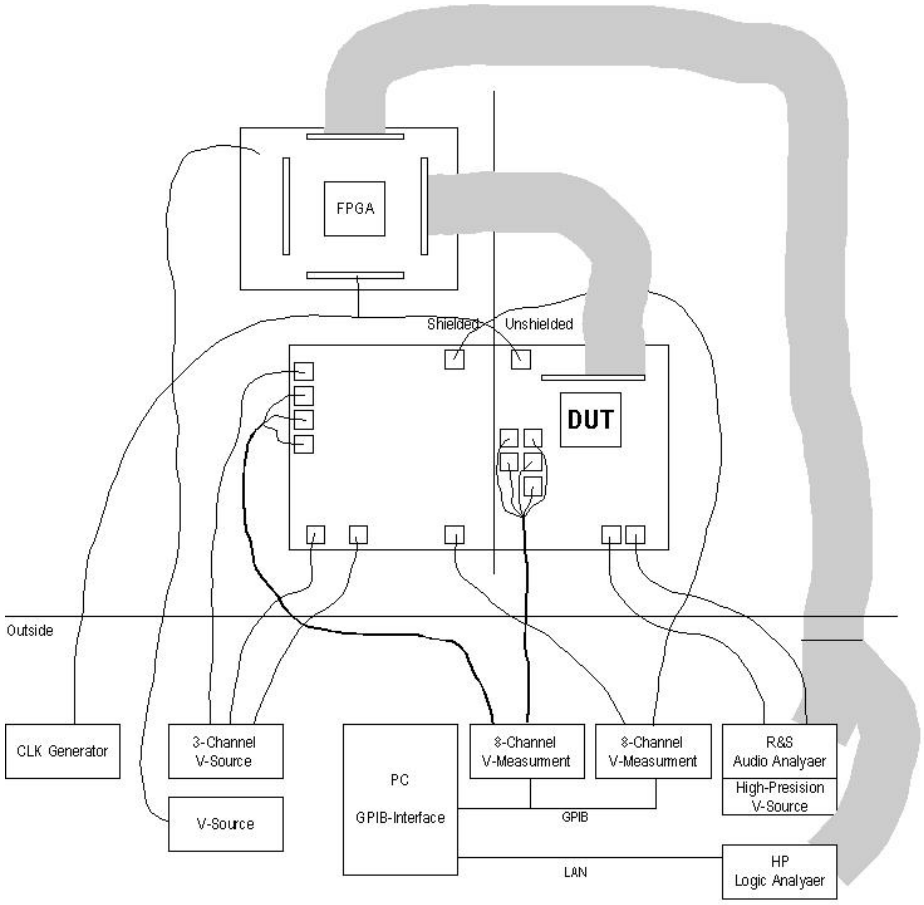

Figure 3-1 Test configuration

The output of the first modulator, which is a single-bit data stream as well as the 16-bit output of the digital filter, was captured by the logic analyzer. A post processing (off line) of the single-bit date was necessary to gain the quality information by calculating signal-to-noise ratio (SNR) and total harmonic distortion (THD). This was done by a software routine on the measurement PC. The 16-bit output of the digital filter was additionally fed to an audio analyser which provided an online FFT of the measured signal.

A separate signal generator was used to provide a sufficiently pure sine wave with up to 1 Vpp and 155 Hz as input signal for the converter.

The following chips were tested:

Device Name	**# of Test Run**	**Radiation Level**
ESA1	1 (biased)	28.6 krad
ESTEC4	2 (biased)	65 krad
	3 (biased)	60 krad
ESTEC5	4 (unbiased)	17.5 krad

As mentioned above, the delta-sigma chip consists of the modulator and a digital filter. Due to the fact, that the on-chip digital filter has never been tested before and only placed on the chip to gain information on interfering effects of digital signals (e.g. CLK) on the analogue delta-sigma circuitry, it was found out, that the 16-bit digital output was not representative for the performance of the delta-sigma converter. Therefore the 16-bit data were not recorded but nevertheless the digital supply current was monitored. This gives an idea about the behaviour of the digital part of the chip during irradiation.
All SNR and THD results are based on the single-bit output of the first delta-sigma modulator.
The data presented here below are only a part of all performed measurements, but the selected curves give a good overview of the chip performance during and after irradiation.

4 Test Results

4.1 Test Run #1 (ESA1) — Biased

Action performed	“Quick and Dirty Test” Irradiation of device until failure
Device name	ESA1
Device condition	biased
Electrical parameters to be tested	Voltages: VREFP, VREFN, AGND Currents: IDDA, IDDD, IREFP, IREFN, IAGND Output: 1-bit
Radiation level	28.6 krad
Dose rate	70rad/min

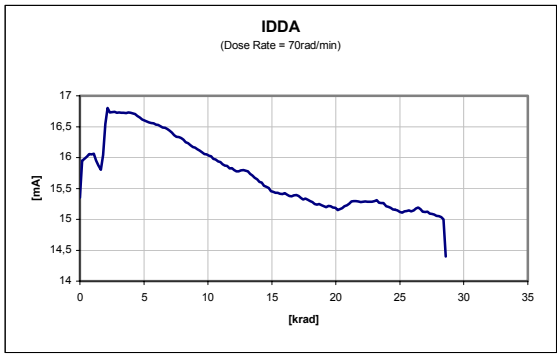

Figure 4-1 ESA1 IDDA

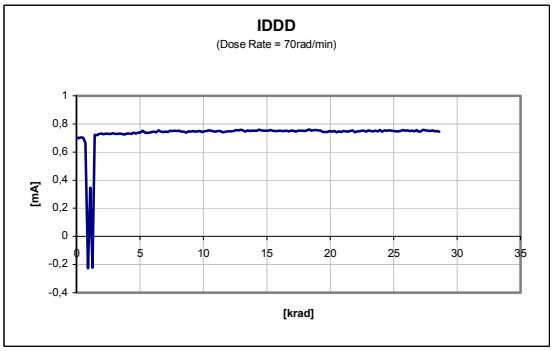

Figure 4-2 ESA1 IDDD

At the beginning of the irradiation an increase of the analogue current (see Figure 4-1) was observed. This trend stopped after approx. 2 krad and reversed its direction. At the end of the irradiation the analogue current decreased again in a very short time (current step). This was exactly when the radiation source was switched off. The analogue current consumption of approximately 14.25 mA remained constant for several hours (not shown in diagram). The digital current in Figure 4-2 shows a short drop to partly negative currents (about 1 mA) at the beginning of the irradiation. This burst could not be assigned to any special event (due to the very low supply current the current sensing circuit was very sensitive to environmental influences).

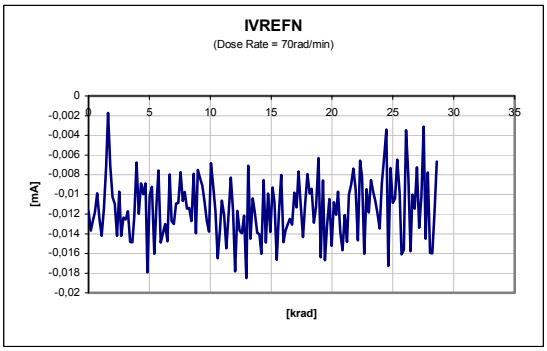

Figure 4-3 ESA1 IREFN

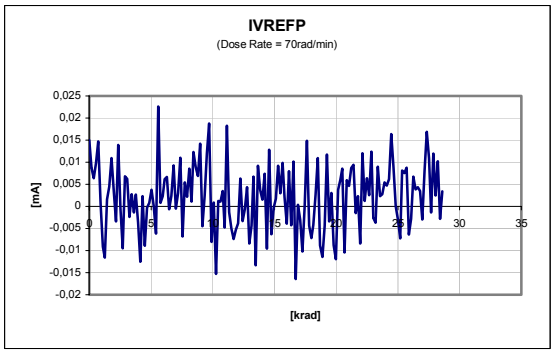

Figure 4-4 ESA1 IREFP

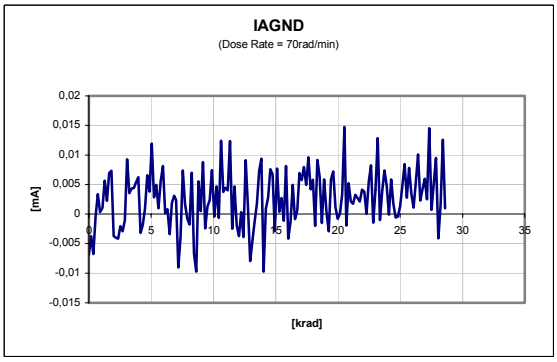

Figure 4-5 ESA1 IAGND

The reference currents (Figure 4-3, Figure 4-4 and Figure 4-5) stayed constant during the complete irradiation up to 28,6 krad. A maximum delta of 0,03 mA around the mean value of IREFN, IREFP and IAGND was observed.
The absolute value of the currents is not very accurate and has varied during the test. It is due the very low current value and the artificial offsetting in the current sensing circuit.

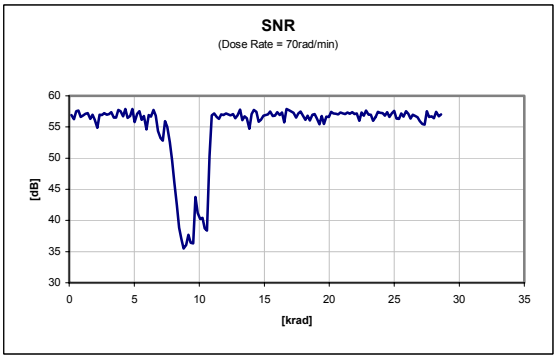

Figure 4-6 ESA1 SNR

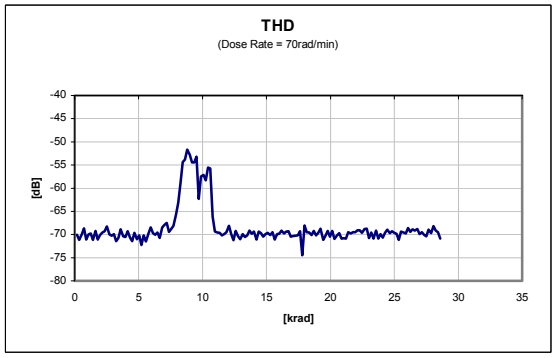

Figure 4-7 ESA1 THD

The device last out fully functioning until the end of the first irradiation test with a maximum total dose of 28.6 krad.

The nominal SNR of the analogue-to-digital conversion of one delta-sigma modulator is around 57 dB SNR (Figure 4-6). During the whole irradiation a striking decrease of conversion quality was observed from about 8 to 11 krad (SNR and THD). The test signal applied was 0.4 Vp and 155 Hz.
The intermediate decrease of conversion quality is probably not a measurement artefact. It seems that the chip was temporary influenced by irradiation. The SNR and THD signature cannot be assigned to any special event and no conjunction to other system parameters (currents and voltages) can be determined. It wasn't measured in a similar way during the following test cycles.

4.2 Test Run #2 and 3 (ESTEC4) — Biased

Action performed	Irradiation of device until failure, testing analogue part of the delta-sigma chip
Device name	ESTEC4
Device condition	biased
Electrical parameters to be tested	Voltages: VREFP, VREFN, AGND Currents: IDDA, IDDD, IREFP, IREFN, IAGND Output: 1-bit
Radiation level	125 krad
Dose rate	70rad/min

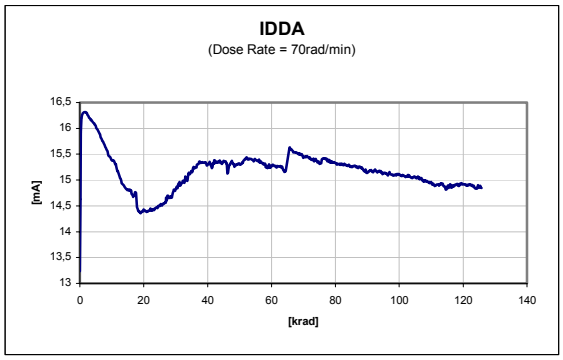

Figure 4-8 ESTEC4 IDDA

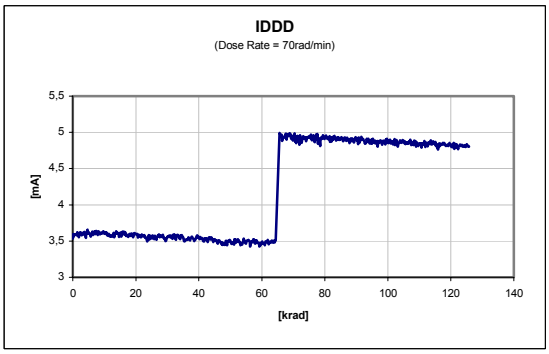

Figure 4-9 ESTEC4 IDDD

The goal of this test was to irradiate the chip until either thermal destruction or irreversible malfunction. At the end of the test at 125 krad the chip showed still the nominal performance, so that the limit load for this chip hasn't been reached yet. All diagrams are a combination of two irradiation tests under the same conditions from 0-65 krad (test #2) and from 65-125 krad (test #3) with an annealing time of 7.5 hours at room temperature (25°C) in between.
The IDDA in Figure 4-8 shows again a current increase at the beginning of the test which was observed in a similar way in the test before. But soon after it changed its direction and decreased after a short irradiation time to a level which was slightly more then the current at the beginning of the test with 14 mA. After 65 krad, as mentioned before, the irradiation was paused for 7.5 hours. By switching on the irradiation source again the same increasing and

dropping characteristics of the analogue current was visible. At the end of the test the analogue current consumption stabilised around 15 mA.
The IDDD (Figure 4-9) shows a marked jump of 1.4 mA at the beginning of the second test cycle. This signature might be caused by a changed resistance coupling of the pins to the socket. During the pause the chip was removed from the socket to provide some additional tests. There are no explicit current peaks and exceptional current increases visible during the whole test which shows that the digital part of the chip still was in good condition.

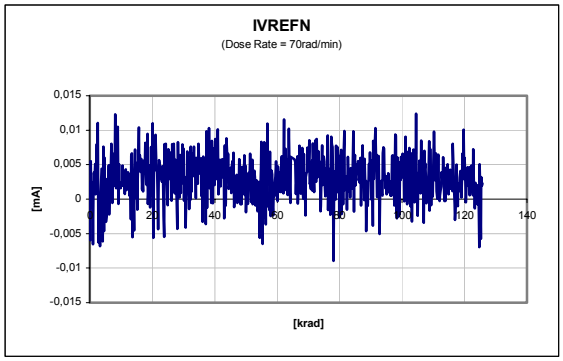

Figure 4-10 ESTEC4 IREFN

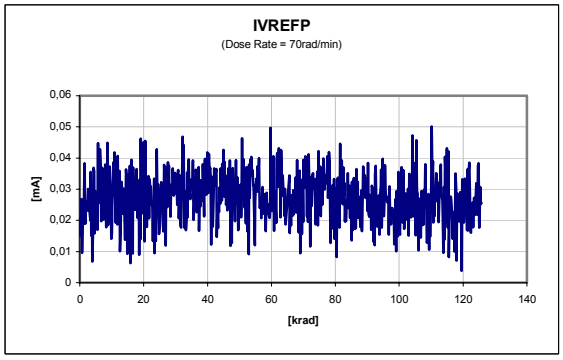

Figure 4-11 ESTEC4 IREFP

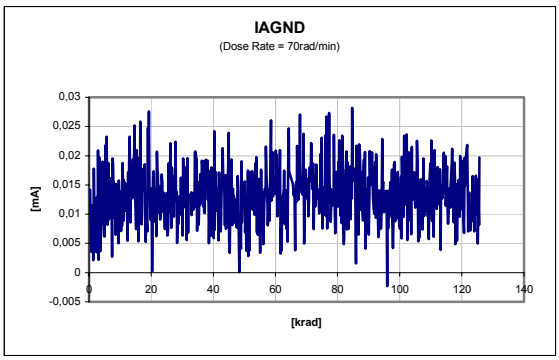

Figure 4-12 ESTEC4 IAGND

The reference currents (Figure 4-10, Figure 4-11 and Figure 4-12) stayed constant during the complete irradiation up to 125 krad. A maximum delta of 0,04 mA around the mean value of IREFP,IREFN and IAGND was observed. There are no changes in the nominal current value in comparison to other tested chips.
The absolute value of the currents is not very accurate and has varied from test to test. It is due the very low current value and the artificial offsetting in the current sensing circuit.

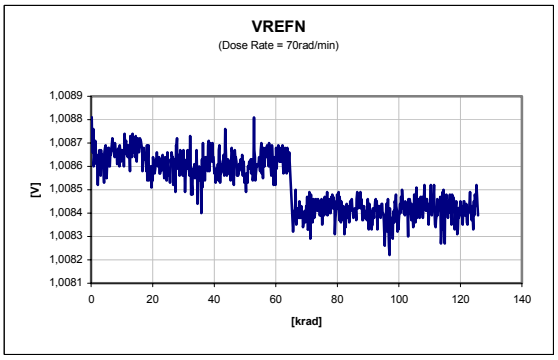

Figure 4-13 ESTEC4 VREFN

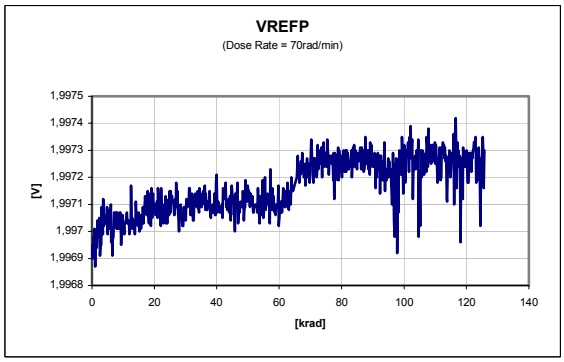

Figure 4-14 ESTEC4 VREFP

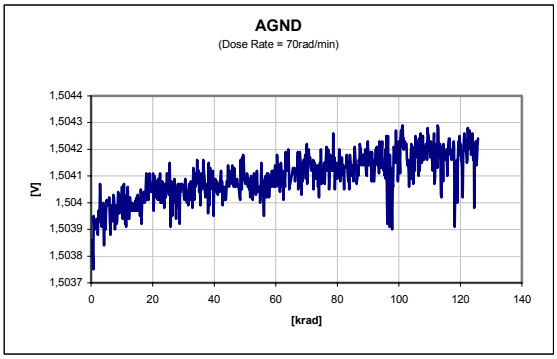

Figure 4-15 ESTEC4 AGND

The reference voltages VREFN and VREFP remained nearly constant during the separate irradiation periods. The AGND voltage seems to increase continuously over the accumulated dose. The maximum delta for all measured reference voltages is 0.5 mV even for AGND (see Figure 4-13, Figure 4-14 and Figure 4-15).

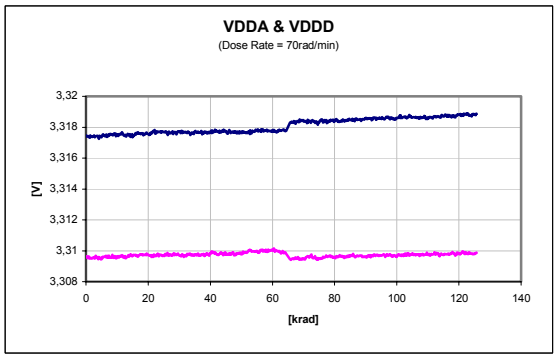

Figure 4-16 VDDA & VDDD

In Figure 4-16 VDDA (upper) curve and VDDD (lower) curve are depicted exemplary for all performed irradiation tests. A more or less linear increase could be observed over the full test cycle. Nevertheless, the current consumption signature shown in Figure 4-8 and Figure 4-9 include more information on the chip behaviour as the supply voltage curves (the voltages were generated in a radiation protected environment). The plot is only shown for the completeness of all performed measurements.

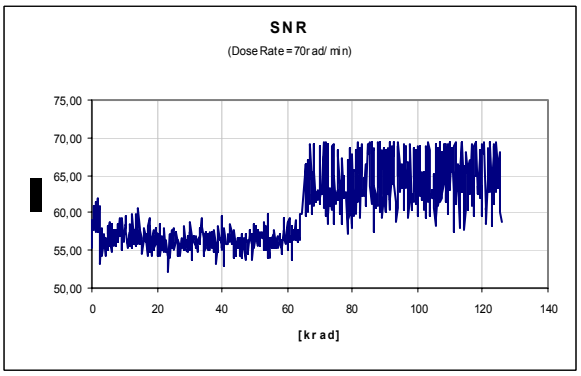

Figure 4-17 ESTEC4 SNR

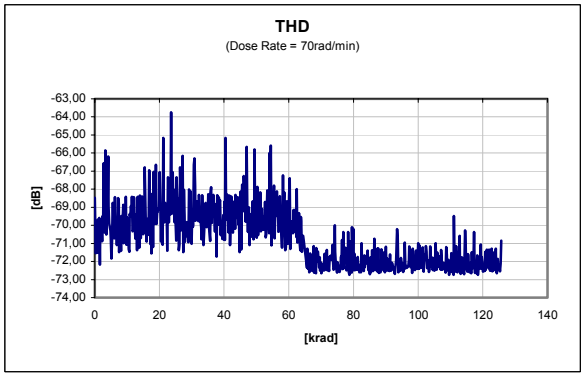

Figure 4-18 ESTEC4 THD

As mentioned before, the nominal SNR of the first 2-order delta-sigma modulator is around 57 dB. As shown in the Figure 4-17 there is a small drop of the SNR noticeable at the beginning of the test, which corresponds to the IDDA drop, but then the conversion stayed stable at 57 dB for the first 65 krad of total ionization dose. A striking SNR step is visible at 65 krad in Figure 4-17 which was caused by removal and re-installation of the same chip. This was necessary for additional measurements as mentioned before. Surprisingly, a marked SNR improvement from 56 to 64 dB can be observed as well. A drawback of the

phenomenon is an increased “SNR noise”, which is probably caused by an influence from the measurement equipment.
The THD diagram (Figure 4-18) shows a similar characteristic, with an increase of the conversion quality in the second irradiation period, but the harmonic distortion in the first part is much “noisier” then in the second. This behaviour is reversed to what was found in the SNR chart, where the first part of the diagram is much smoother then the second.

4.3 Test Run #4 (ESTEC5) — Unbiased

Action performed	Testing of the analogue part of the delta-sigma chip
Device name	ESTEC5
Device condition	unbiased
Electrical parameters to be tested	Voltages: VREFP, VREFN, AGND Currents: IDDA, IDDD, IREFP, IREFN, IAGND Output: 1-bit
Radiation level	17.5 krad
Dose rate	70rad/min

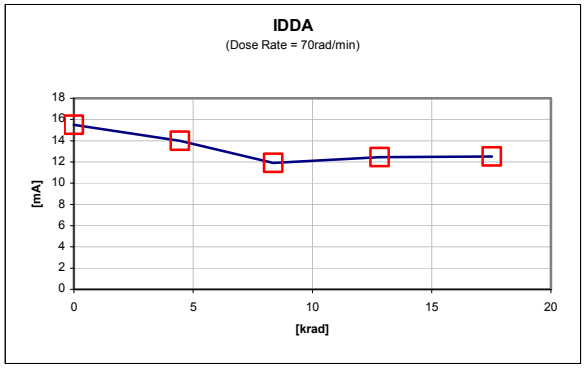

Figure 4-19 ESTEC5 IDDA

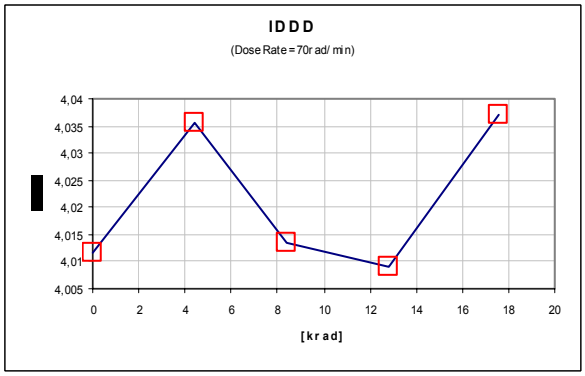

Figure 4-20 ESTEC5 IDDD

The goal of this unbiased test was to find out if the behaviour of the irradiated unbiased chip corresponds to that of the biased. The measurement setup provided a complete disconnection of the power lines, but because of set-up reasons the CLK signal remained active over the whole test cycle.
As the IDDA chart of Figure 4-19 shows, the decrease of the analogue current at the beginning of the irradiation is also visible in the unbiased test. The current stabilized after 10 krad and did not change until the end of the test at 17.5 krad. In comparison to the charts of prior tests, the current decrease of IDDA is larger. The decrease nearly doubled and did not last as long as in the 125 krad chart (Figure 4-8) for example. These differences and the lower nominal power consumption may derive from variations in the chip production.
IDDD (Figure 4-20) was unobtrusive during this test.

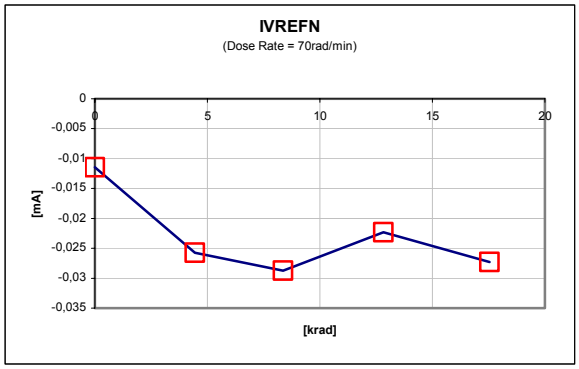

Figure 4-21 ESTEC5 IVREFN

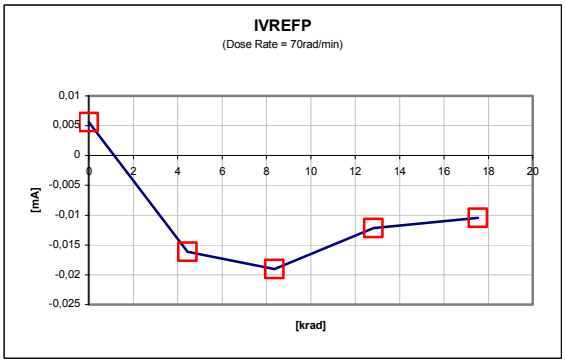

Figure 4-22 ESTEC5 IVREVP

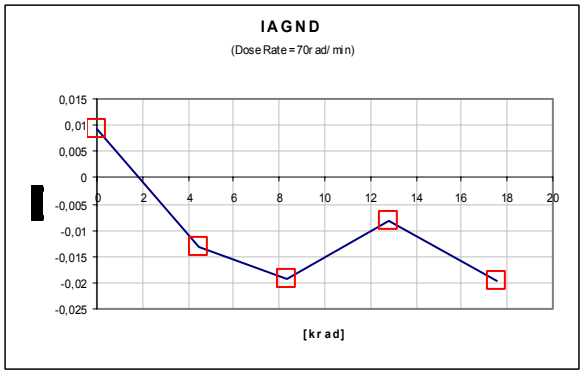

Figure 4-23 ESTEC5 IAGND

Figure 4-21, Figure 4-22 and Figure 4-23 shows the reference currents IREFN, IREFP and IAGND, which remained in a fair range. A small decrease of all currents over the total ionization test is noticeable. As mentioned before, the absolute value of the currents is not very accurate and has varied from test to test. It is due the very low current value and the artificial offsetting in the current sensing circuit.

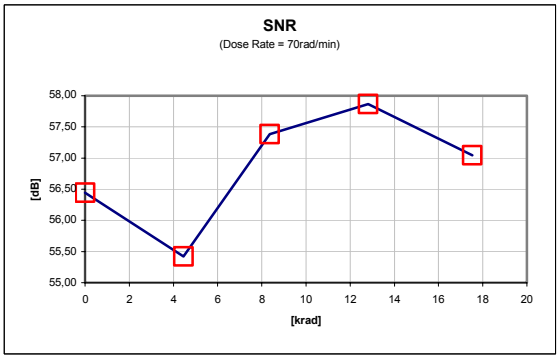

Figure 4-24 ESTEC5 SNR

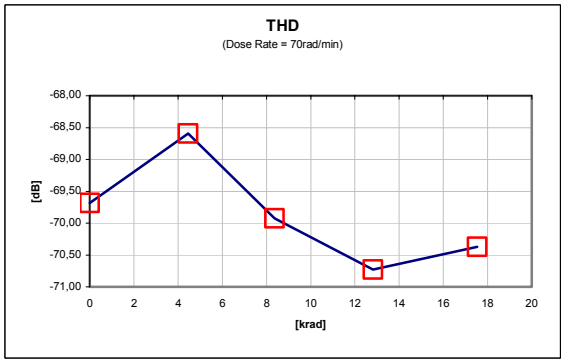

Figure 4-25 ESTEC5 THD

SNR (Figure 4-24) and THD (Figure 4-25) showed the performance as expected. The values remained in a fair range and correspond to measurements taken during prior tests.

5 Conclusion

A 0.35 µm CMOS process based delta-sigma converter/modulator designed by IIS has been irradiated biased and unbiased with a Co-60 gamma ray source. Several chip parameters were monitored as presented in chapter 4.

A full check of the analogue part of the chip was performed by measuring the analogue supply currents and reference voltages as well as the signal to noise ratio (SNR) and total harmonic distortion (THD) of the first of all together two cascaded second-order modulators.

It is different for the digital part of the chip. The 16-bit digital output was not representative for the performance of the delta-sigma converter due to a failure in the digital filter design. Therefore, the 16-bit data were not recorded and digital errors like bit flips and stuck bits could not be detected. A second way to check parts of the digital circuitry would have been the record of the 5-bit output of the error-cancellation logic of the modulator (this is the part of the modulator that combines the single-bit outputs of the two second-order modulators to a single 5-bit output signal). Due to an irradiation damage of the EEPROM used for the XILINX FPGA the 5-bit data could not be recorded. Nevertheless, the digital current consumption was monitored during all radiation tests which gives at least an idea of the behaviour of the digital part of the chip.

In general it can be said that it was not possible to destroy the chip or even change its behaviour in terms of power consumption and quality (SNR and THD) of the single-bit output data of the first modulator significantly (125 krad biased and 15 krad unbiased with 70 rad/min).

A repetitive characteristic was found in the IDDA curves at the beginning of each irradiation test. IDDA increased at the beginning of the test (low total dose) and decreased with accumulated dose. But this characteristic did not show any influence on the conversion quality. The digital current (IDDD) consumption was mostly stable and unobtrusive.

The following events in the test results stay open:

- Decrease of SNR and THD between 8 and 11 krad during the first test, which occurred only once.
- How strong was the influence of the 7.5 hour annealing at room temperature on the 125 krad measurement series, like the IDDA/IDDD current jumps and change of SNR/THD at the transition from test #2 to #3.
- The slight decrease of the reference currents (IVREFN etc.) during the unbiased test, which was not observed in a similar way during the biased tests.