An Overview of Radiation Single Event Effects Testing of Advanced Memory Components.

by

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Abstract

Historically, memory components have been used as technology drivers in the semiconductor industry. Consequently memory components have been and remain the most dynamic product segment in the area of digital integrated circuits. An abundance of different memory types exists and product life cycles tend to be short, in some instances with up to 2 die revisions per year. For space applications this presents a particular challenge in the area of radiation testing. Device complexity, performance, the diversity of architectures and the use of innovative micro-packaging concepts, pose many practical problems in the implementation of Single Event Effects (SEE) testing and analysis of test results. This paper aims to provide an overview of the current situation and describes the evolution of test approaches used or proposed for heavy ion SEE testing of advanced memory components.

1. Introduction

Heavy ion SEE responses in many types of commercially available memories have been studied over the years [1]-[3]. As memory technology and density changed, new and different types of responses were seen. However in general, SEE testing could be carried out on these memories in a conventional manner by removing the plastic packaging material on top of the die and hitting the device with different ion species and using tilting to increase the effective LET. Using dedicated memory test systems and having access to dedicated accelerator beam lines, low cost SEE testing could be carried out routinely.

At the time Dynamic Random Access Memories (DRAMs) changed to lower V_{CC} voltage and had memory capacities of 16-Mbit, some manufacturer started to use centre bonding which included a lead frame on top of the die [4]. These types of assemblies could not be prepared for heavy ion SEE testing in the conventional way (by plastic etching) as about 30 % of the die would be shadowed by a comparatively thick lead frame, see Figure 1 (X-ray of Hitachi 256-Mbit SDRAM). Lead frames or any other material on top of the die would influence the ion strike since most affordable accelerators have ion range limitations (ESA requirements; min. ion penetration in Si = 40 µm). So at that time, bare die procurement and special packaging was the only way out.

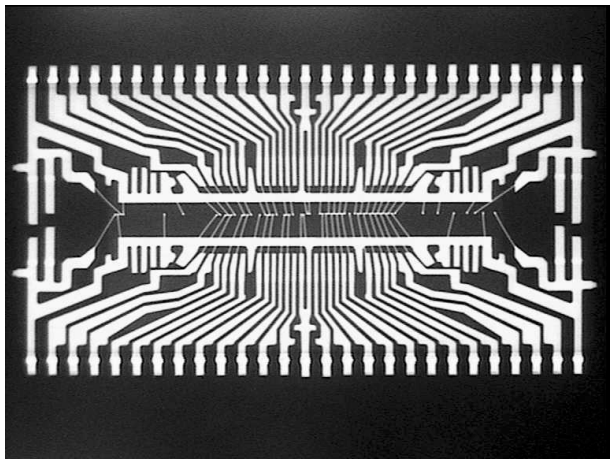

Figure 1. X-ray of Hitachi 54-pin TSOP package.

Today nearly all memories are assembled with central bonding, lead frames and a plastic package hardly larger than the memory die (TSOP package). Knowing that these products have a short life cycle and that the bare die procurement option is out, currently available memories have to be tested as they come if heavy ion SEE responses have to be characterised. So, will it still be possible to perform heavy ion SEE testing today? Will it still be possible to prepare these commercially available memories for testing? Will it still be possible to use the ions available at our accelerators? And at the end – will it still be possible to obtain reliable and correct SEE data? These questions and more specifically test approaches, test facilities and future SEE testing will be addressed in this paper.

2. Main Objectives

As just highlighted, the main objectives are to investigate new ways of performing heavy ion SEE testing on available memories and to verify obtained data. So initially, two different sample preparation methods were considered. The first method A) was to chemical etch the package and re-bond the bare die to a test board and B) to thin the back of the package/die to a die thickness of about 50 µm. Approach A) would allow irradiation from the front side (the old way of testing) whereas B) would require irradiation from the back side (new way of testing). These two approaches will allow a direct comparison of events created by Front and Back irradiation of identical memories. Unfortunately, both preparation methods are difficult to master and particularly the test sample preparation is very time consuming. However, the thinning approach has the advantage that the main assembly of the memory stays untouched but the thinning process itself – is not easy. Secondly, if irradiated from the back side the accelerator ion penetration becomes a major issue. So, what will be required from the accelerators if the back irradiation approach will be the preferred method in the future?

3. SDRAM Memories

In order to perform these experiments a large number of different advanced memory types were procured. Synchronous DRAMs, covering 64-Mbit, 128-Mbit and 256-Mbit, were etched/re-bonded and thinned, but the success rate was not very high. Out of 30 devices etched/re-bonded (from 9 different manufacturer/device types), only 3 parts could be rated as fully functional. However, later attempts improved the sample yield but in general a leakage current issue still needs to be solved.

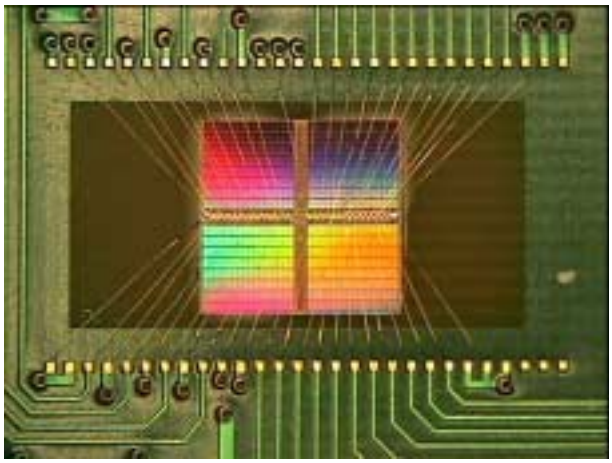

Figure 2. Etched/re-bonded Micron 128-Mbit SDRAM, MT48LC16M8A2.

For thinned devices the success rate was somewhat higher. Out of 14 devices, 8 could be rated as fully functional. So eventually, two sets of fully workable etched/re-bonded and thinned devices became available. One set from Micron, MT48LC16M8A2 128-Mbit and one set from Infineon, HYB39S256800CT-75 256-Mbit. Further thinned devices from Samsung, K4S640832D 64-Mbit, from Toshiba, TC59SM708 128-Mbit, from Hyundai HY57V56820 256-Mbit and from Hitachi, HM5225805 256-Mbit, also became available for testing. The etched/re-bonded Micron device can be seen in Figure 2 whereas a thinned Hyundai device can be seen in Figure 3.

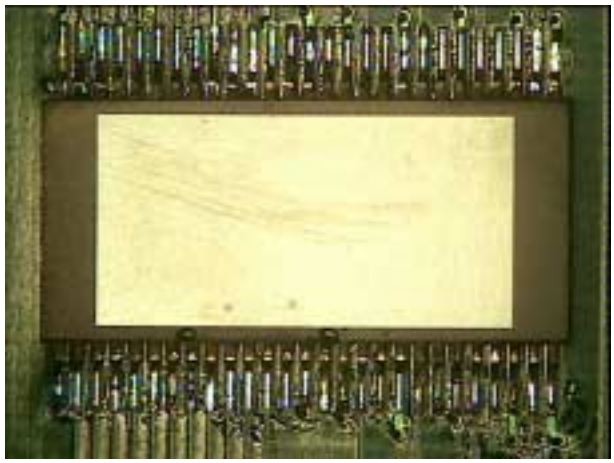

Figure 3. Thinned Hyundai, 256-Mbit SDRAM, HY57V56820, s/n #14.1.

4. Test Conditions

Both etched/re-bonded and thinned parts were further prepared for radiation SEE testing to be carried out on a Hirex test system dedicated to memory testing. This test system, based on a modular rack concept together with a generic memory test board, uses a 12MIPs on-board processor to control all functions and communications. Optimised for radiation accelerator SEE testing, the memory test board (dedicated per device) can be moved in and out of the beam within 100 ms. This function allows all critical steps like Device Under Test (DUT) initialisation, write and read operations to take place during periods when no particles hit the DUT. This feature eliminates dubious test conditions but requires particle count and test time corrections.

Other important test features are the used test pattern and test sequence. Testing with a 4 bits/14 words repetitive test pattern of one bank (out of 4 in a SDRAM) is carried out in either Static or Dynamic test mode. Here three basic test configurations were used; Static Auto-Refresh, Static Self-Refresh and Dynamic

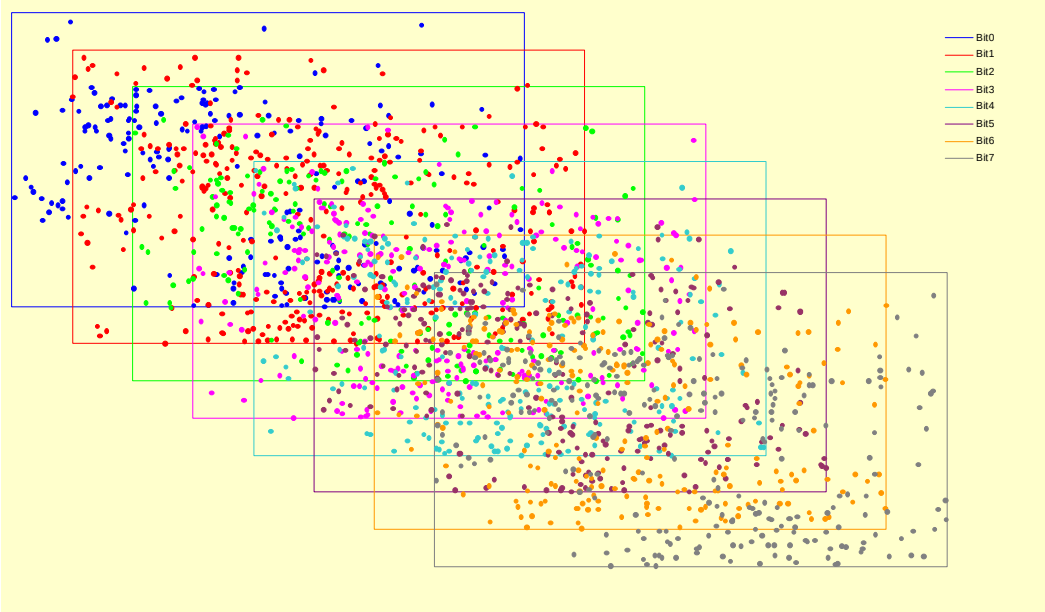

Figure 4. Random SEUs as observed in a Hyundai 256-Mbit SDRAM tested with Si-ions at JYFL.

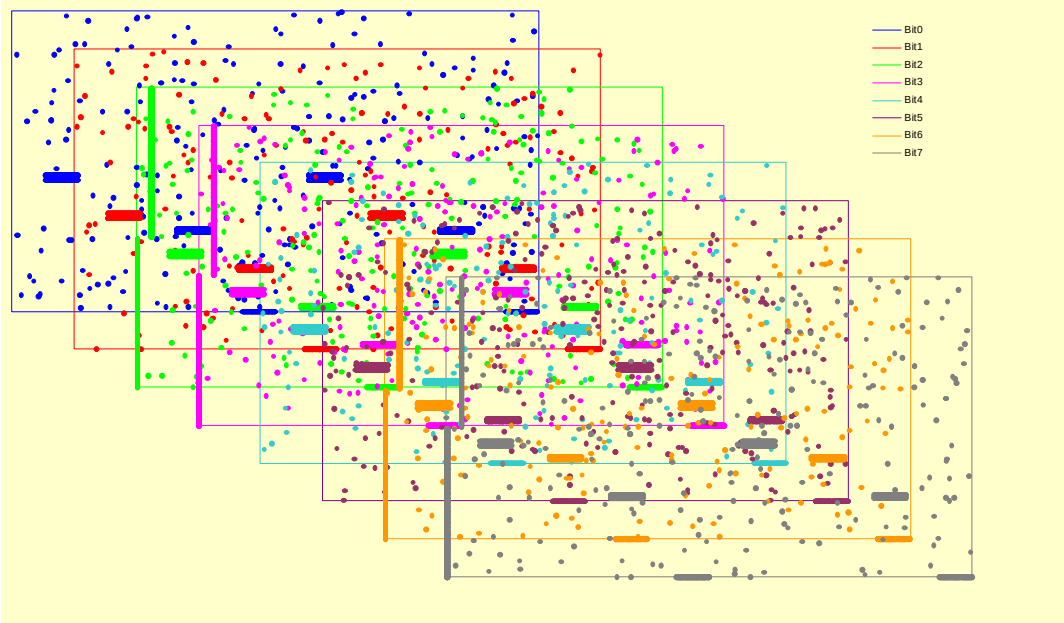

Figure 5. Row and column events as observed in a Toshiba 128-Mbit SDRAM tested with Fe-ions at JYFL.

modes. During beam exposure in Dynamic mode a continuous read-write sequence is performed whereas in Static mode the read-write check is carried out following a pre-set time or pre-set beam exposure time.

Finally the error reporting routines are of great importance as they have to log all types of events ranging from latch-up to stuck bits, and from single bit errors to block (column and row) events. However, if two large error events occur during two successive read cycles, a functional error signal is issued and the test stopped. Otherwise, any word in error with at least one bit flip detected is recorded as an error and information as cycle iteration number, word address and expected pattern stored. Post analysis of the test file allows for identification of bit flip transition (1 to 0/0 to 1) and the occurrence of Multiple Bit Upsets (MBU).

In order to validate the data obtained during a test run, a new error mapping analysis package has been developed. This analysis program, to be used at the accelerator at the end of each test run, plots a 3-dimentional mapping of the error events. The distribution of errors are displayed over 8-bits (8 planes) versus column/row addresses. Each dot (in different colours per plane) represents an event and should be

evenly distributed over the whole bank as shown in Figure 4. Column and row events, distorting the SEU counts, are easily recognised as shown in Figure 5. For this JYFL/Fe-ion run, the total number of recorded events 4201 had to be corrected to 1826 SEUs. Uneven distribution of events would point in the direction of faulty memory performance or beam homogeneity problems. So these validation checks are now performed routinely following each run at the accelerator. Corrupted or faulty test runs can now be repeated immediately so at the end of a test campaign, the obtained database is preliminary checked and most SEU, MBU and functional events verified.

5. Test Facilities

As highlighted earlier, irradiation from the backside requires high penetration ions so several test facilities were used and obtained SEE data compared. In addition to the Heavy-ion Irradiation Facility (HIF) at UCL, Louvan-La-Neuve, Belgium, another European accelerator facility at the University of Jyvaskyla, Finland, was used for the first time. The JYFL facility was evaluated by ESA for general usage while running a new ion cocktail never produced before. Finally the well-known heavy ion facility at Lawrence Berkeley National Laboratory (LBNL), the 88-inch cyclotron, Berkeley, USA, was used as a reference source. Detail description of these SEE test facilities can be found in the literature [5][6][7] whereas here, the used ion details will be highlighted. Of importance here is the ion penetration range in Silicon, which for UCL, Table 1a, show the lowest penetration range, from 42 to 80µm. The ions at JYFL, Table 1b, show a very improved

Table 1a. HIF, Belgium - ion details.

Ion Cocktail M/Q=4.94	Energy MeV	Range µm Si	LET MeV(mg/cm²)
$^{10}B^{2+}$	41	80	1.7
$^{15}N^{3+}$	62	64	2.97
$^{20}Ne^{4+}$	78	45	5.85
$^{40}Ar^{8+}$	150	42	14.1
$^{84}Kr^{17+}$	316	43	34.0
$^{132}Xe^{26+}$	459	43	55.9
UCL – Ion Cocktail #1 produced for ESA			

Table 1b. JYFL, Finland - ion details

Ion Cocktail M/Q=3.8	Energy MeV	Range µm Si	LET MeV(mg/cm²)
$^{15}N^{4+}$	140	211	2.0
$^{30}Si^{8+}$	280	127	7.0
$^{56}Fe^{15+}$	523	95	18.0
$^{82}Kr^{22+}$	766	93	29.0
JYFL – Ion Cocktail produced for ESA Oct. 2001.			

Table 1c. LBNL, USA - ion details.

Ion Cocktail M/Q=3.6	Energy MeV	Range µm Si	LET MeV(mg/cm²)
$^{18}O^{5+}$	184	228	2.19
$^{22}Ne^{6+}$	216	179	3.44
$^{29}Si^{8+}$	292	139	6.31
$^{40}Ar^{11+}$	400	129	9.88
$^{51}V^{14+}$	508	116	14.8
$^{65}Cu^{18+}$	659	108	21.6
$^{86}Kr^{24+}$	886	111	30.0
$^{136}Xe^{37+}$	1330	104	53.7
LBNL – Ions used/available February 2002			

penetration range compared to UCL ions, but not quite the same as at LBNL, Table 1c. However, ion penetration close to 100 µm in Si, should be sufficient for backside irradiation. Finally it should be noticed, that UCL could probably produce higher penetration ions today but at the time of utilisation, the HIF ion penetration requirement was > 40 µm. Likewise, the standard ion cocktail at JYFL covered an ion penetration range of 64 - 108 µm compared to the ESA requested and evaluated range of 93 – 210 µm.

6. Heavy ion Test Results

For these SDRAM studies, the first test campaign was carried out at JYFL using ions as detailed in Table 1b. Initially, etched/re-bonded and thinned devices from Micron (128-Mbit) and Infineon (256-Mbit) were assessed against the three basic test configurations: Static Self/Refresh (S/R), Static Auto/Refresh (A/R) and Dynamic. No noticeable differences could be observed between SEU results obtained from these three test modes. Examples of obtained SEU results, expressed as cross section per cm^2 per bit, are showed in Table 2. Results are presented for two ion LETs and covers both etched/re-bonded (Front irradiated) and thinned (Back irradiated) parts.

Table 2. Test mode comparison of SEU results presented as cross section cm^2/bit.

Micron Test Mode	Front #10.2	Front #10.3	Back #10.2
Static S/R	3.31E-10	3.52E-10	4.57E-10
Static A/R	3.31E-10	3.27E-10	4.65E-10
Dynamic A/R	3.44E-10	3.28E-10	4.66E-10
JYFL – Ion LET = 7.0 MeV/(mg/cm^2).			
Static S/R	2.65E-09		4.48E-09
Static A/R	2.52E-09		4.90E-09
Dynamic A/R	2.53E-09		4.85E-09
JYFL – Ion LET = 18.0 MeV/(mg/cm^2).			

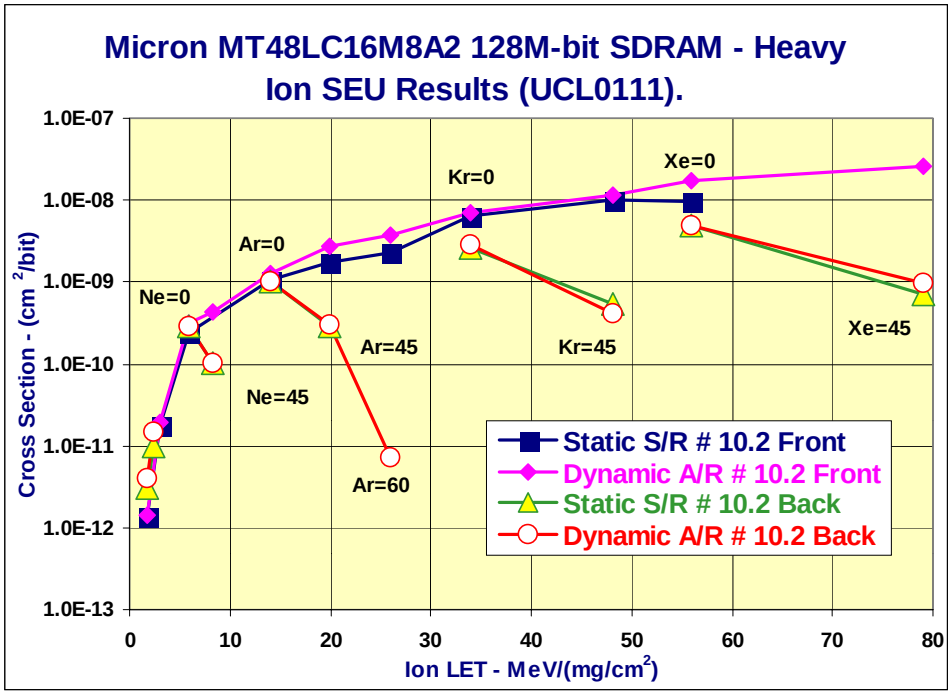

Figure 6. Micron MT40008LC16M8 Front and Back irradiated SEU results from the HIF, Belgium (not LET corrected).

Further Micron MT40008LC16M8 test mode comparison results from the HIF, are shown in Figure 6. Static Self/Refresh and Dynamic Auto/Refresh SEU results compares well for all 6-ion species available. Also presented in the same graph are the SEU results for the thinned device irradiated from the Back. Using the same Static and Dynamic test modes, SEU results can again be rated to be very consistent, however now, the overall curve shows signs of an ion penetration problem. Results obtained with ions at normal incidence start to fall off at higher LETs. The Krypton point at a LET = 34.0 MeV/(mg/cm^2) and Xenon point at a LET = 55.9 MeV/(mg/cm^2) have the lowest ion range in Si, a range of about 43 µm. At tilted angles of 45° or higher, the ion penetration problem is clearly apparent. Also Argon ions at a LET = 14.1 MeV/(mg/cm^2) and Neon ions at a LET = 5.85 MeV/(mg/cm^2) show clear signs of ion penetration limitations.

In reality Back-side irradiated SEU results have to be LET corrected in respect to ion penetration depth. Here, none of the presented Back-side SEU results will be shown corrected due to uncertainty concerning the exact thickness. It is certainly possible to measure this accurately, and it will be done at a later point in time, but for the time being, all workable thinned devices are in use for testing. LET corrections for the Back-side results in Figure 6 would, if we consider a penetration depth of 40 µm, move the Neon ion point from a LET of 5.85 MeV/(mg/cm^2) to a LET value around 8-9 MeV/(mg/cm^2). The Krypton ion point at a LET of 34.0 MeV/(mg/cm^2) would move towards a LET of 20 MeV/(mg/cm^2), thus significant corrections need to be applied if we use ions with limited range in Silicon. Corrections required for the same depth but using a Krypton beam at JYFL or LBNL would only result in a slightly higher LET value. So in order to present Back-side SEU results at the correct LET, the exact DUT thickness need to be known.

Using the same tester and the same Micron MT40008LC16M8 devices as used and tested at the HIF, SEU results from the JYFL facility can be seen in Figure 7. The HIF Static and Dynamic SEU results, Front irradiated, are used as a reference. JYFL SEU results, Front irradiated, compares well for the two ions initially available, Silicon and Iron. Both Static and Dynamic data can be rated as lying directly on top of the HIF results. Further comparison of SEU results obtained from the Back (Static/Dynamic) shows excellent correlation. Even tilted results show no sign of ion penetration problems but unfortunately, the final tests with Krypton ions could not be carried out due to accelerator problems. Anyway, both Front and Back irradiated results were very consistent and compares well with Front irradiated HIF results. Comparison would even improve if LET corrections were carried out. Presented SEU results, for both Silicon and Iron ions, would in reality be moved towards slightly higher LET values.

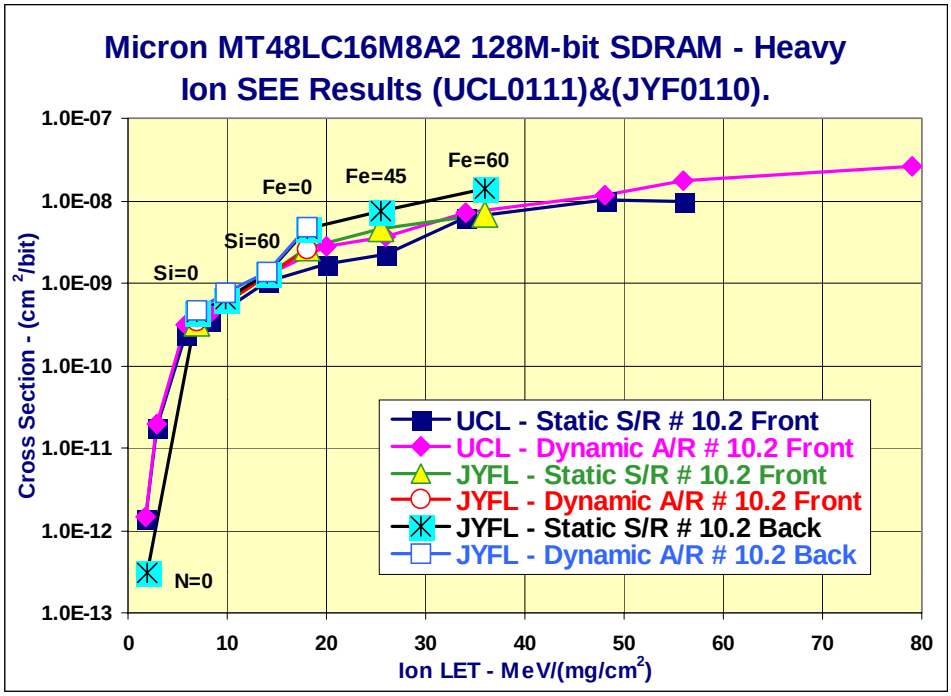

Figure 7. Micron MT40008LC16M8 Front and Back irradiated SEU results from the HIF, Belgium and JYFL, Finland (not LET corrected).

The same tester and the same Micron MT40008LC16M8 devices as used and tested at the HIF and at JYFL, were once more used at the LBNL facility, USA. This time, both the HIF and the JYFL Static SEU results, Front irradiated, were used as a reference as shown in Figure 8. Further, LBNL SEU results, both Front and Back irradiated, are also presented in the same graph for Static testing. At LBNL, 7 different ion species were used during perpendicular DUT exposure. Unfortunately at high LET testing, the DUT often show functionality errors which results in poor SEU data or even loss of data. So SEU results at the highest LET value were not obtained with Xenon ions but with Copper ions and having the DUT exposed at 60°. At this LET point it is interesting to note that both Front and Back SEU results fall well on top of one another. This point in the direction that the ion used has sufficient penetration range, thus validating the tilting concept as well. So overall, good correlation exists between the Front SEU data taken at all three test sites. The Back SEU data set from LBNL also compares well even though some lower results can be seen in the middle of the curve.

7. Discussions and Conclusions

As stated earlier, ESA has successfully performed cost effective heavy ion SEE testing on commercially available memories for many years. However, testing today requires different sample preparation methods and more energetic ions as addressed in this paper. As also shown, heavy ion SEE testing of advanced memories can be carried but not as easily as in the past. Sample preparation is now a key issue, which has to be optimized. Irradiation of parts from the Front-side is still the preferred way of testing but as experienced, not the most successful approach in the sample preparation phase. The Back-side thinning approach and Back-side irradiation is possible and have been validated here and by other groups [8][9]. Obtained SEU data compares well with Front irradiated data, if the DUT has been thinned sufficiently for the ions available. The advantage of having the DUT main assembly untouched has to be balanced against the thinning exercise and possible higher ion penetration requirements.

At accelerators used by ESA (HIF and JYFL), more ion species and more energetic ions will be needed if Back-side irradiation has to be performed routinely. The concept of tilting the DUT during a Back-side irradiation still needs to be further characterized. Also further attention needs to be placed on the LET corrections required in respect to the ion penetration range. So in order to progress and address these issues, ESA has initialized a new series of preparation and test programs covering the following detailed tasks:

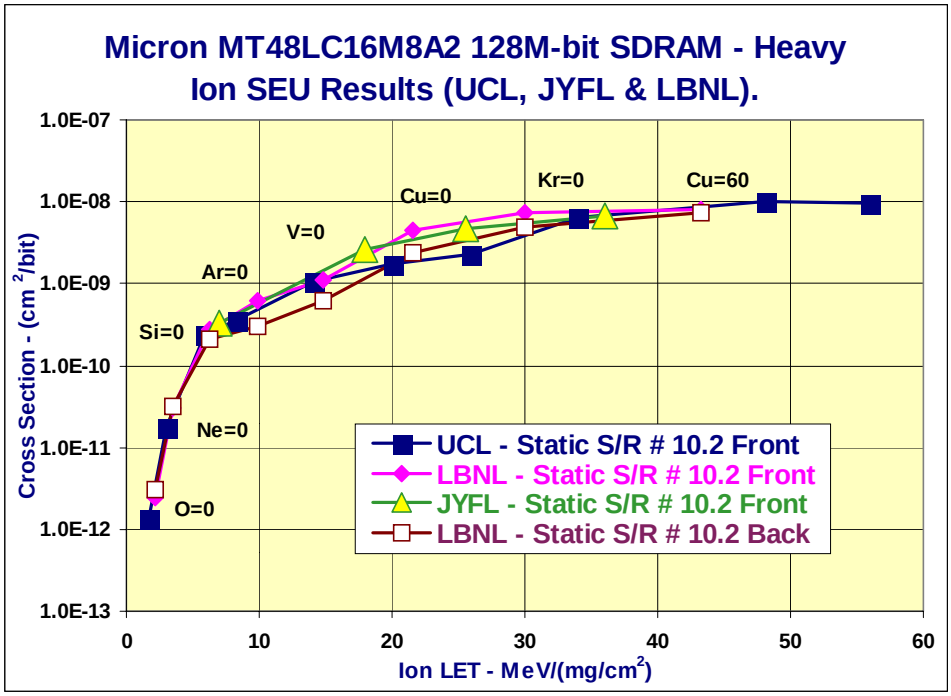

Figure 8. Micron MT40008LC16M8 Front and Back irradiated SEU results from the HIF, Belgium, from JYFL, Finland and LBNL, USA (not LET corrected).

1) To perform failure analysis of parts failing the etch/re-bonding preparation method.
2) To prepare new parts using improved etch/re-bonding approaches.
3) To prepare new parts using improved thinning techniques.
4) To develop higher charge state beams at the HIF.
5) To develop metal ion beams with intermediate LET at the HIF.
6) To develop additional ions for the JYFL ion cocktail.
7) To upgrade the JYFL heavy ion facility in general.
8) To start a new evaluation program combining all of the above tasks.

Finally it should be stressed that the data presented here, primarily on the Micron MT40008LC16M8 128-Mbit SDRAM, only have been analysed and presented in respect to SEUs. Many other events like stuck bits, block events, loss of functionality and column/row events have not been reported here. These events do exist in the obtained database but have been considered unimportant in this context. Contrary, the SEUs have been analysed in detail where the error mapping analysis package has proved its value. In addition to the 3-D error mapping display as presented here, a table format also list all parameters and events obtained during each run and for the entire test campaign.

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9. References

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