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EUROPEAN SPACE AGENCY CONTRACT REPORT

The work described in this report was done under ESA contract. Responsibility for the contents resides with the author or organisation that prepared it.

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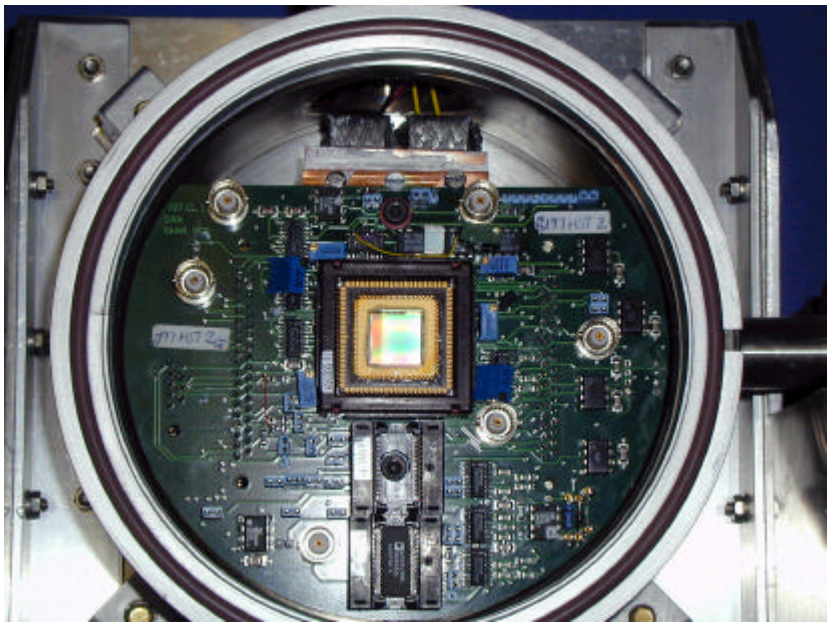
Final Report
Radiation Testing of 2-D Imaging Detectors and ADCs for Attitude Sensors

ESTEC Contract Reference: CCN No. 3 to Contract 12227/96/NL/SB
Sira Electro-Optics Limited Reference: A/1330/00/19



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Prepared for ESA, ESTEC

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Date: 30 June 2000

CONTENTS

SUMMARY

Three separate, but linked, studies have been undertaken in the area of radiation effects on attitude sensors. These studies relate to:

- Degradation of CCD charge transfer efficiency and the effect on the accuracy of star position measurements
- Radiation evaluation of a CMOS active pixel sensor (APS) - a candidate for use on future missions
- Radiation evaluation of two high-speed, low power, 12-bit ADCs (candidates for use on star trackers and other imaging missions).

The rationale for these studies and the main results achieved are outlined below.

CCD Measurements

CCD-based attitude sensors (star trackers) have been used on many spacecraft in low Earth orbit (LEO) and also on several 'scientific' missions such as ROSAT, ISO and XMM. Although these missions (particularly the scientific missions) can be demanding in performance, the radiation environment is not usually severe enough to have a major impact on functionality. Enough is known about CCD radiation effects to make performance predictions for these missions (although there is always a need for evaluation of new device types and often for lot acceptance radiation tests on flight parts). There are, however increasing needs for attitude sensors to operate in more demanding orbits: for example, geostationary orbit (GEO) and some satellite constellation orbits ~ 1400 km altitude ('big LEO'). In these orbits the proton-induced loss in CCD charge transfer efficiency (CTE) is of significant concern since it distorts the star images and leads to errors in centroid position measurements. In this study the proton-induced CTI is studied in detail for two CCD types and is related to direct measurements of star centroid errors. The CCDs were EEV (now called Marconi Applied Technologies) n-channel devices (types CCD47-20 and CCD02-06 with 13 μm x 13 μm and 22 μm x 22 μm pixels, respectively).

It is well known that CCD imagers are susceptible to loss in CTE due to trapping states introduced by displacement damage. The nature of the trap capture and emission processes are also well known, although only the dominant trap (the E-center) has been characterized in detail. The effect on an image depends on the size of the charge packets to be transferred (the signal) and on the background charge (the 'fat zero'). It also depends on the relative values of the transfer rate (and the 'dwell time' within a pixel) and the trap capture and emission times – the latter being temperature sensitive. Hence CTE is by no means a fixed parameter. It depends on the application: both the operating conditions and the nature of the images.

The majority of previous investigations have concentrated on 'astronomical' applications which involve low temperature operation, low backgrounds and slow readout rates. Star trackers and remote sensing instruments operate at near-room temperature (usually –40° C to +20° C) at higher clocking rates and use frame transfer CCDs. In a frame transfer CCD signal collected in the image region of the device is quickly transferred into a storage region (which is shielded from light) by parallel transfers at line move times of a few microseconds. During readout each line in the storage region is moved into a horizontal readout register and then moved one pixel at a time through the output amplifier: a process that typically takes on order of 1 ms. This difference in line move times during frame transfer and readout results in differences in CTE depending on where it is measured in the image. This is because pixels at the top of an image experience mainly fast line moves during the frame transfer, pixels at the bottom of an image, which are furthest from the readout register, experience the same number of frame transfer moves and, in addition, the same number of moves during readout. (Recall that CTE is defined as the fractional charge loss per pixel transfer, averaged over *all* the transfers.) The dwell time effect can itself depend on signal and background.

The experimental CTI results found in this study illustrate the complex dependencies on signal, background, temperature and clocking. The measurements also show the difference in CTI for the two line move speeds (frame transfer and readout) as a function of signal size. The effect of the smaller pixel size of the CCD47-20 was also measured. There was a decrease in the CTI damage approximately of the same size as the reduction in pixel area, though there were also differences in the dependence on signal size and background.

Measurements of the errors in the centroid positions of artificial star images can be large when the background is low – even after only 4 krad(Si) of 10 MeV protons (equivalent to 1.8×10^9 p/cm^2). Provision of a 'fat zero' background is the most effective way of improving accuracy. Use of 'windowed' readout (where only a small, e.g. 8 x 8 array of pixels is digitized and the remaining pixels are 'dumped' at a fast rate) is also beneficial. Use of both these techniques is recommended for CCDs which will experience environments equivalent to 10 MeV fluences in excess of 10^{10} p/cm^2 (or a displacement damage dose of greater than 0.8×10^8 MeV.cm^2/g).

APS Measurements

CMOS active pixel sensors offer an alternative to CCDs for applications where moderate noise performance (~50 electrons rms) is acceptable. They offer a distinct advantage in high proton fluence orbits, since pixels can be directly addressed so that charge does not need to be transferred through the device, as in a CCD. Displacement damage-induced charge trapping effects (CTE loss) are therefore not observed.

The devices tested in this study were the current version of the CMOS active pixel sensor developed for ESA's 'Attitude Sensor Concepts for Small Satellites' (ASCoSS) study. This development is on-going and the present results are based on the current version of the device which has 515 x 512 25 μm x 25 μm pixels. The imager has been designed and manufactured by IMEC, Belgium. A special feature is that a high fill factor (~ 85%) has been achieved by the

ability to collect charge from the volume of silicon below the gain and switching transistors located within each pixel[1].

The device can operate with reduced integration time (setable in multiples of the line readout time) and with direct addressing of regions of interest. Double sampling of the signal before and after read removes most of the Fixed Pattern Noise (pixel-to-pixel non-uniformity caused by transistor offsets, etc.) so as to achieve a level of ~ 200 electrons rms. There is the option of using either an on-chip 8-bit ADC or an external ADC. An external 12-bit ADC was used for the detailed characterisation of the imaging performance, but the performance of the on-chip ADC was also assessed.

The sensor is fabricated using the 0.7 µm twin well p substrate process of Alcatel Microelectronics (AµE) and uses photodiodes rather than photogates as the sensing element. The photodiodes are formed by the n-well/p substrate junction of the standard CMOS process. Co-60 tests on photodiode test structures have previously been reported by the manufacturer, along with measurements on new photodiode architectures designed for increased radiation tolerance[2]. This study complements that work by concentrating on complete devices and including proton and heavy ion tests.

As with most current generation CMOS devices, significant total dose effects are not expected in the thin gate oxides for the radiation levels experienced in the low dose rate space environment. This was confirmed by measurements of clock threshold voltages which changed at rates of only a few mV per krad(Si).

However the turn-on of parasitic structures can cause large increases in dark current and supply current. Previous IMEC results indeed suggested that edge-leakage effects are present with this version of the ASCoSS device. Based on these results, it had been thought that the sensors would fail after a few krad(Si). In fact it turned out that there was significant post-irradiation annealing of thermal dark current and of power supply currents so that there is the likelihood that the devices will survive to at least 20 krad(Si) in a low dose rate space environment. It is possible that previous IMEC devices failed due to high power supply currents occurring immediately after irradiation and with the remaining devices there were not enough statistics to provide an adequate characterisation.

The present results indicate no significant bias dependence to the ionization effects and no significant change in full well capacity, fixed pattern noise or PRNU. However a large decrease in responsivity was seen immediately after proton irradiation, although this annealed after 14 months storage at room temperature. The change may be either a displacement damage effect (reduction in carrier lifetime) or an ionization damage effect (change in drift field), though the experimental results tend to favour the latter explanation. These effects are not seen in CCDs

[1] G. Meynants, B. Dierickx and D. Scheffer, "CMOS Active Pixel Image Sensor with CCD Performance", Proc SPIE vol. 3410, pp 68-76, 1998

[2] J. Bogaerts and B. Dierickx, "Total Dose Effects on CMOS Active Pixel Sensors", Proc SPIE, Photonics West, San Jose, 24 Jan 2000.

(which show no significant change in response at these radiation levels). Further work will be needed to establish a definite mechanism and this may not be worthwhile at this stage since the design of the sensor is being updated to incorporate an enclosed (gate-all-around) photodiode. However the results show that responsivity is an important parameter to measure in all future APS studies.

The other effect of the proton irradiation was to produce dark current spikes. The influence on dark current was studied in detail and found to be similar to that in CCDs, though not as severe (the size of the largest dark current spikes was not as large as in CCDs). However the amplitude of Random Telegraph Signal (RTS) fluctuations was similar to that found in previous CCD studies. (The fluctuations tending to be a larger fraction of the total spike amplitude.)

The on-chip ADC was observed to exhibit latch-up, but not the rest of the sensor (up to a LET of 28 MeV/ mg cm^2).

ADCs

There is a general need for spacecraft systems to use advances in analog-to-digital converter (ADC) technology. In particular, imaging systems such as star trackers and remote sensing instruments require 12 or 14-bit ADCs that have a low power consumption, fast conversion rates (> 1 M sample per second (MSPS)) and good radiation tolerance. To take specific examples, Sira required similar ADCs for general star tracker applications and for the Compact High Resolution Imaging Spectrometer (CHRIS)[3] on ESA's PRogramme for On- Board Autonomy (PROBA) microsatellite mission.

This study reports on an evaluation of two commercial ADCs, the Analog Devices AD9223 and the Linear Technology LTC1415. The AD9223 is one of a family of three devices with a pipelined architecture and output error correction logic. The others are the 9221 (1 MSPS) and the 9220 (10 MSPS). All have the option of using a programmable on-chip voltage reference. Power consumption for the AD 9223 is typically 100 mW. Either single-ended or differential inputs can be used. The 10 MSPS version has previously been total dose tested at high dose rate (71 rad(Si)/s) by Turflinger et al[4]. Effects depended on the input bias condition. Failures were seen at 35 krad (Si) due to differential non-linearity (DNL) and voltage reference changes, but the devices recovered on annealing. The LTC1415 is a slower device (1.25 MSPS) but also has low power consumption (55 mW) and an on-chip voltage reference. Ultra-low power 'nap' and 'sleep' modes are available. Devices were characterized before and after cobalt60 irradiation for integral and differential non-linearity (INL and DNL), noise, power consumption and clock threshold voltage shifts.

[3] M. A. Cutter, D. R. Lobb and R. A. Cockshott, "Compact High Resolution Imaging Spectrometer (CHRIS)", Acta Astronautica, 1999

[4] T. Turflinger, M. V. Davey and J. P. Bings, "Radiation effects in Analog-to-Digital Converters", IEEE Radiation Effects Data Workshop, pp 6-12, 1996.

Both devices appear suitable for low dose rate environments up to at least 20 krad(Si) and probably 60 krad(Si), although the LTC1415 showed marginal performance after a rebound test at 66 krad(Si). Because of its higher conversion rate (3 MSPS, rather than 1.25 MSPS for the LTC1415), the Analog Devices part was selected for use on CHRIS, even though the single event latch-up (SEL) found during the heavy ion tests necessitated the use of in-flight protection circuitry to limit the device current. Although some of the biased AD9223 devices showed large power supply current and changes in DNL ('stuck bits') after 20 krad(Si), these effects annealed out so that all devices were fully functional after 66 krad(Si). For the LTC1415 devices the effects were also small except that the two unbiased devices showed small changes in DNL after baking (after 66 krad) and the biased devices showed changes (~ 20 LSB) in offset after annealing. With both devices the delay time between data and clock increased slightly with irradiation and would probably exceed their manufacturers' allowed limit at higher doses. There were no significant changes in clock voltage thresholds, indicating the use of thin gate oxides. These results are similar to those seen in recent tests of 14 bit ADCs. The AD9243 (14-bit, low power) ADC has been found to show similar total dose behaviour (increase in supply current which anneals)[5,6] and to exhibit latch up[5]. The LTC1414 (14-bit, low power) showed little change and no SEL (tested up to 68 MeV/mg/cm^2)[5].

[5] F. –X. Guerre and J. –F. Pascal, "Radiation Pre-Screening of High Resolution High-Speed ADCs" presented at The ESA ESTEC QCA Final presentation Day, 26 January 2000, record available at http://www.estec.esa.nl/qcswww/tos_qca/

[6] G. Tomasch, R. Harboe-Sorensen, R. Muller and T. Tzscheetz, "Co-60 Total Dose Test of 14- and 16-bit ADCs, presented at The ESA ESTEC QCA Final presentation Day, 19 January 1999.

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1. INTRODUCTION AND SCOPE

This report is prepared under CCN No. 3 to Contract 12227/96/NL/SB and considers radiation effects on three technologies of particular relevance for attitude sensors:

- 512 x 512 pixel CMOS active pixel sensors (APS) arrays manufactured by IMEC, Belgium as part of ESA's ASCoSS programme (Contract 12227/96/NL/SB). In this report these will be termed the 'ASCoSS Sensors'.
- 12-bit low power, high speed ADCs (types AD9223 and LTC1415)
- EEV (now called Marconi Applied Technologies) n-channel CCDs (types CCD47-20 and CCD02-06 with 13 μm x 13 μm and 22 μm x 22 μm pixels, respectively)

IMEC's IBIS 1 sensor has been radiation tested by IMEC (see IMEC report P43999-IM-RP-97011) and this device has a similar pixel structure to the ASCoSS chip. However the full ASCoSS chip has not previously been studied. In this work they were subjected to cobalt60 gamma rays, 10 MeV protons and heavy ion testing (for latch-up). Since the ASCoSS chip is in the early stages of being re-designed by IMEC to improve the radiation tolerance, the purpose of the investigations was to provide inputs to this re-design process – however the radiation data is now available should the present ASCoSS sensors be incorporated into a flight instrument.

The ADCs were irradiated with Cobalt60 gamma rays and heavy ion latch-up testing with a view to determining their general suitability for space use (and in particular to their use on the CHRIS instrument on ESA's PROBA satellite). Testing of the ADCs was carried out bearing in mind the requirements for imaging systems: the waveforms to be digitised usually have flat 'video' and 'reset' levels so that parameters such as 'total harmonic distortion', 'signal-to-noise and distortion (SINAD)', 'effective number of bits (ENOB)' etc. are not applicable.

The n-channel CCDs were studied in order to gain further understanding of the effect of proton-induced CTE damage on the accuracy of star centroiding.

2. TEST OBJECTS

2.1 ASCOSS CMOS IMAGERS

The ASCoSS imager chip was specially designed by IMEC for a demonstrator star tracker for the ESTEC project 'Attitude Sensor Concepts for Small Satellites'. The sensor chip is described in detail in IMEC document P43318-IM-RP-97012, 'Image Sensor Specification' 29-Feb 1998, issue 3.0. Figures 2.1-1 and 2.1-2 show a block diagram and a photograph of the sensor. An active pixel sensor (APS) is a matrix of photocells (in this case photodiodes) which can be addressed by switching the pixels in turn to the connecting lines via transistors. This allows for a

variety of readout patterns. For example, blocks of cells can be addressed (so called "windowing" operation) without having to spend time sequentially clocking out and "dumping" the other lines and pixels as in a CCD. In the case of the ASCoSS sensor, readout is done by "one-hot" shift registers along the horizontal and vertical edges of the chip, into which pulses are loaded which travel along, switching on the various rows and columns in turn. (There are three shift registers: one for line readout, one for line reset, and one for column readout selection). By separating the pulses which read and reset the pixels, the time for which the pixels collect signal (the integration time, which fixes the optical sensitivity) can be varied and made different from the overall refresh time of the image (the frame time, which fixes the update rate of the sensor).

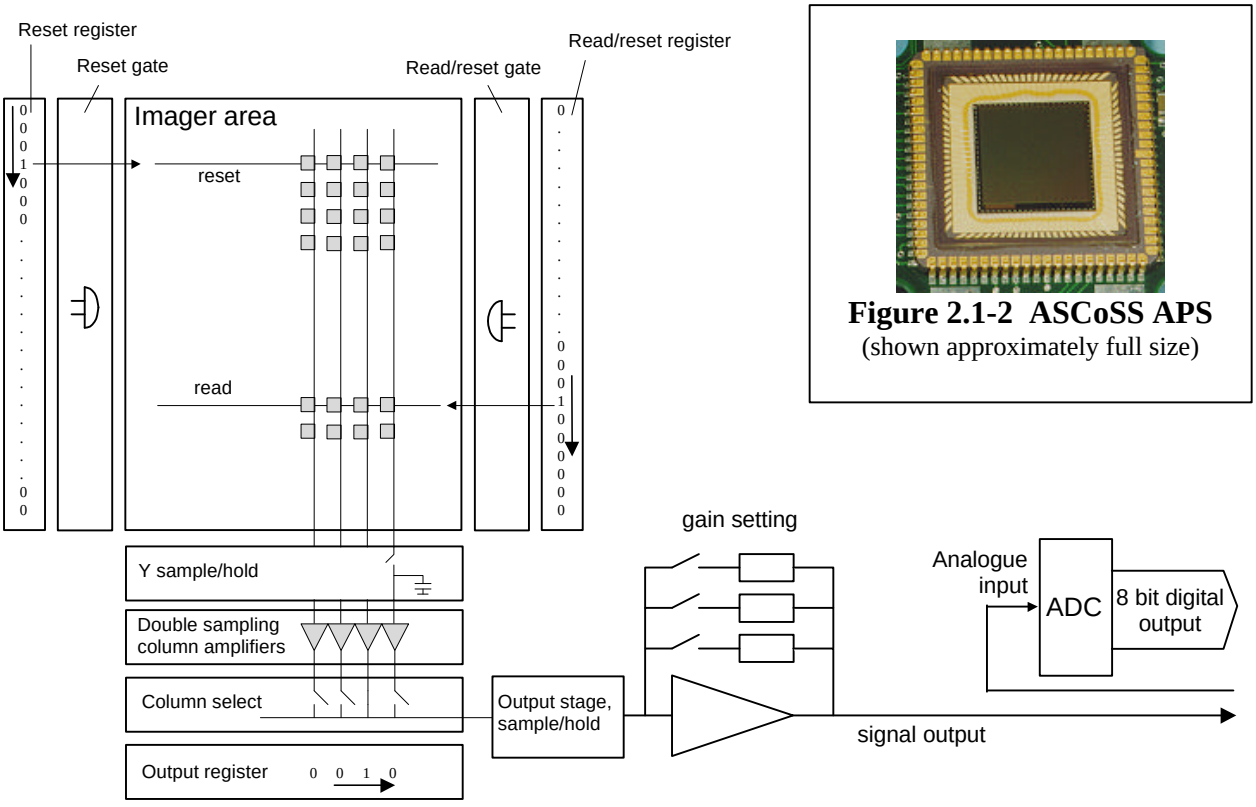

Figure 2.1-2 ASCoSS APS
(shown approximately full size)

Figure 2.1-1 ASCoSS APS schematic

The sensor format is given in the following table. The imager area contains an array of 512 by 512 pixels with 25 μm pixel pitch. The pixels are horizontally interconnected by a reset line and a readout select line. Vertically all pixel outputs of a column are simultaneously connected to the column amplifier but only the pixels whose row is selected for readout can feed a signal to their respective column amplifiers.

Sensor format specification

Technology	MIETEC 0.7µm analogue CMOS
Pixel architecture	Integrating active pixel sensor with 3 transistors per pixel
Format	512 by 512 pixels
Pixel pitch	25 µm
Die size	14.6 mm by 14.3 mm

A number of signal processing options were implemented on-chip, namely:

- a second row-reset register, allowing variable integration time via flexible clock sequences;
- double sampling of the signal before and after read, to remove most of the Fixed Pattern Noise (pixel-to-pixel non-uniformity caused by transistor offsets, etc.);
- an 8-bit ADC, resulting in digital pixel signals being given directly from the detector;
- variable gain amplifier with gains of 1, 2, 4, and 8 in front of the ADC, to improve the effective ADC resolution on small signals.

The pixel design is based on a 3-transistor active pixel architecture (figure 2.1-3). During the integration time the capacitance of the photo-diode (D1) serves as an integrator for the photo-current: the photo-current discharges the pre-charged capacitance. A source follower (T2) continually senses the voltage over the capacitance. During read-out a selector switch (T3) connects the sensed voltage to a column amplifier that further processes the signal. After read-out the reset transistor (T1) restores the charge on the capacitance to its reset level and the pixel is ready for the next integration period. The photo-diode capacitance is 8fF. This low value allows an internal charge-to-voltage conversion factor of 20µV/e-. The external or effective conversion factor is only 9µV/e- because the voltage amplification in the subsequent source followers is lower than 1.

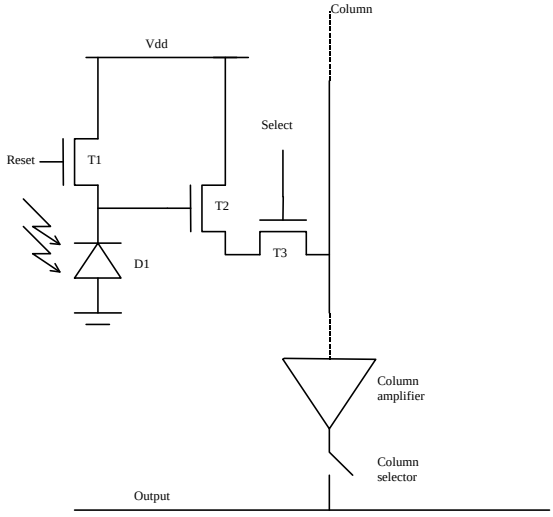

Figure 2.1-3: Electrical circuit for a pixel

Pixel integration time is not simultaneous for each line in the imager: Figure 2.1-4 shows that line A is reset and read out before line B. Both lines have an equal, but not simultaneous integration time. The stare time of each line is equal to the total image time but they are not simultaneous.

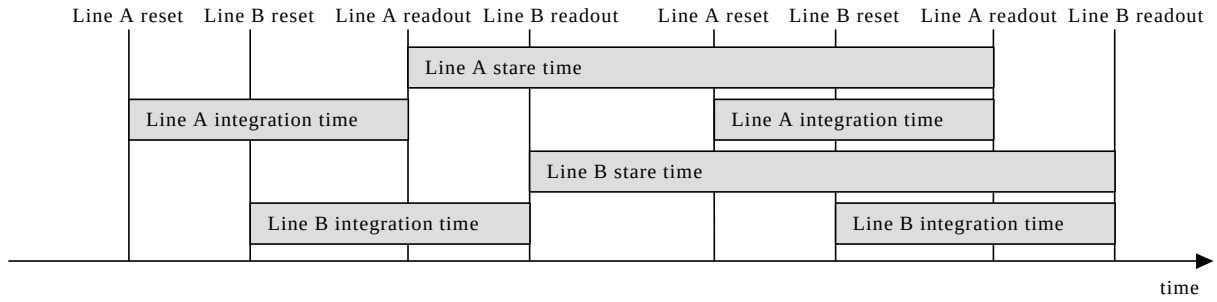

Figure 2.1-4: Integration time vs. stare time

The integration time can be varied by applying an appropriate delay between the start of the read of the reset-shift registers.. It can be set in line-time steps from a full frame time down to 1/512 of a frame time. Exposure longer than the nominal frame time is only possible by lowering the clock speed or by insertion of delays between the reset and the readout of a frame.

Details of the readout and reset sequence are given in P43318-IM-RP-97012 (referenced above). Several clock signals are needed as summarised below:

Signal	Restriction
Clk_yrst, clk_yrd,clk_xrd	Max clock frequency: 50 MHz Remark: after a sync two dummy clock pulses are required to initialise the shift register.
Sync_xrd, sync_yrd, sync_yrst	Minimum pulse width : 125 ns
S1	Minimal pulse duration: 1µs Pulse start minimal 2 µs after falling edge of clk_yrd
/S2/	Pulse duration > pulse duration of S1
/S3/	Must be on during readout sequence
Reset_l, reset_r	Minimal pulse width: 1 µs

The main performance parameters for the sensor chip are given below:

Property	Value in sensor specification
Fill factor	> 85%
Dark signal	6900 electrons/pixel/sec (25°C)
CVF	8.45 µV/electron
Saturation Voltage	1.2 V
Saturation signal	142,000 e^-/pixel
Readout noise	80 e^-/pixel
FPN (max)	5,000 electrons/pixel
Linearity	< 1% up to 80% saturation

Speed specifications

Frame rate	10 frames per second
Average pixel rate	2.88 Mps at 10Hz frame rate.
Maximum pixel rate (unity gain)	10 Mps
Maximum shift register clock frequency (horz. And vert.)	50 MHz (raw shift register clocking rate, without readout or reset functionality)
Output stage unity gain bandwidth	105 MHz
Integration time (10Hz frame rate)	Variable between 0.2 ms and 100 ms in 0.2 ms line time steps.

The devices were supplied in ceramic packages with glass windows which could be removed by heating using a hot air blower.

The devices were all from the same production batch and were labelled on the underside with a device number of the form x/y , this was abbreviated to xy for Sira identification (e.g. device #3/5 became device #35).

The devices were allocated as follows (device #55 was damaged during window removal and not used):

device number	**irradiation condition**
62, 63	10 MeV protons, unbiased
34, 35	latch-up test, heavy ions
25, 43, 44, 54	Cobalt 60, biased
84, 75	Cobalt 60, unbiased
65, 74	spare

2.2 ADCS

2.2.1 AD9223AR

The AD 9223 is one of a family of low power 12-bit converters and can operate up to 3 MSPS. The other members are the AD9221 (1.25 MSPS) and the AD9220 (10 MSPS). The device has a programmable on-chip reference but an external reference can also be used. Single-ended or differential inputs can be employed. Figure 2.2-1 shows a block diagram of the device.

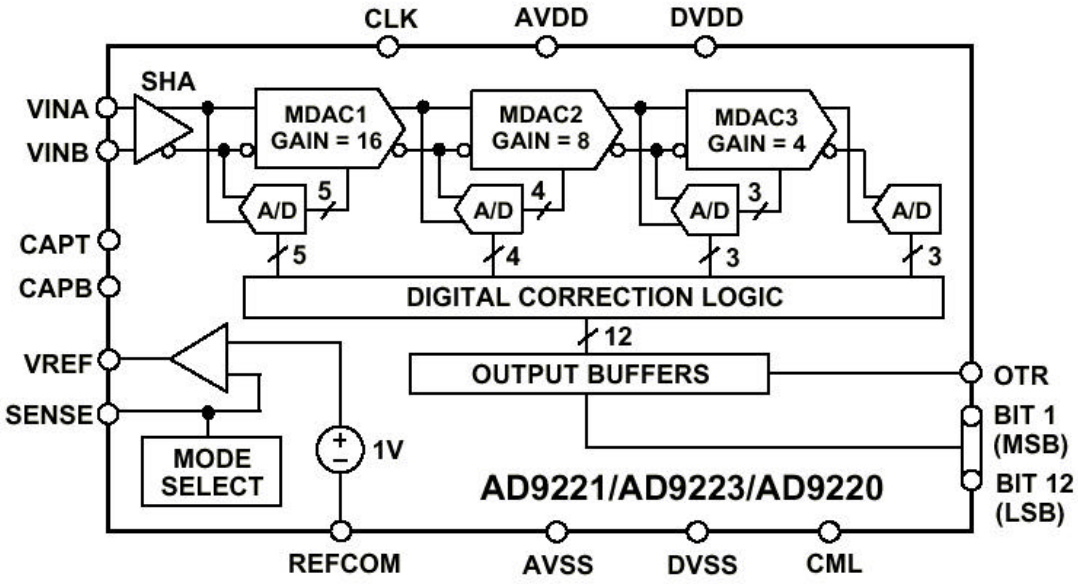

Figure 2.2-1 Block diagram of the AD9223

Typical performance is as follows:

Maximum conversion rate	3 MHz
Integral non-linearity	±0.5 LSB typical
Differential non-linearity	±0.3 LSB typical
Supply current:	
analogue V_{DD}	26 mA (max) 20 mA (typical)
digital V_{DD}	0.5 mA (max) 0.02 mA (typical)

The cobalt60 irradiated devices were from batch A63155.1, date code 9702 (devices from this batch were also used for Sira's CHRIS instrument on ESA's PROBA satellite). The devices were in plastic surface mount packages and did not originally have individual serial numbers.

They were engraved at Sira with an identification number (1,2,3 ...) and allocated as follows:

device number	irradiation condition
1,2	unbiased
3,4	static bias on both inputs
5,6	static bias on one input dynamic (ramp on the other)
7,8	dynamic bias on both inputs
9,10	spare

Another (single) device from the above batch was used for latch-up testing (designated device #2 at the time but not the same device as cobalt60 #2 mentioned above) and two devices (# 1 and 3, again, not the same as cobalt60 #s 1 and 3) were from another batch (AG3710.1, date code 9644).

All three AD9223 devices were de-lidded by ESTEC prior to the heavy ion latch-up tests

2.2.2 LTC1415CSW

The LTC1415 is a 700ns 12-bit converter and can operate up to 1.25 MSPS. The device has a programmable on-chip reference but an external reference can also be used. Single-ended or differential inputs can be employed. Two power shut-down modes ('nap' and 'sleep') provide flexibility for low power systems. Figure 2.2-2 shows a block diagram of the device.

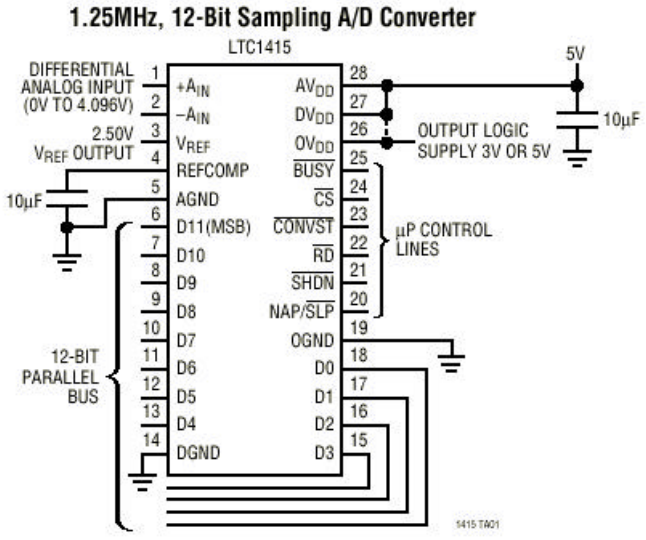

Figure 2.2-2 Block diagram of the LTC1415

Typical performance is as follows:

Maximum conversion rate	1.25 MHz
Integral non-linearity	±0.35 LSB typical
Differential non-linearity	±0.25 LSB typical
Supply current (VDD = 5 V):	
	20 mA (max) 11 mA (typical)
nap mode	2.3 mA (max) 1.5 mA (typical)
sleep mode	1 µA (typical)

The devices had date code 9627K and did not have individual serial numbers. They were in plastic surface mount packages. One was de-lidded by ESTEC for heavy ion latch-up tests (another LTC1415 device was destroyed during de-lidding) and the remainder were engraved with an identification number (1,2,3 ...) and allocated as follows (the latch-up test device was not engraved):

device number	irradiation condition
1,2	unbiased
3,4	static bias on both inputs
5,6	static bias on one input dynamic (ramp on the other)
7,8	dynamic bias on both inputs
9,10,11	spare

2.3 CCDS

Both the EEV CCD47-20 and CCD02-06 devices to be studied operate in frame transfer mode and have 3-phase electrodes.

The CCD47-20 has 1024x1024 image region pixels with pixel size 13 µm x 13 µm without any supplementary buried channel. The CCDs have an electrode structure for advanced inverted mode operation (AIMO). This means that the image and store sections can only be clocked in the forward direction. Other features are:

- no store shield deposited on the CCD. To form a store shield black tape is put on the glass window
- dump gate
- non-antibloomed
- split readout register. The two halves of the CCD were readout through separate amplifiers

The device type numbers are

- CCD47-20-2-231A, grade 2 device, first choice for all tests
  - Serial number (batch - wafer- die) 7271-2-3
- CCD47-20-5-231A, grade 5, spare
  - Serial number (batch - wafer- die) 7271-2-1

Both devices are from the same wafer.

The CCD47-20 was operated with a line move time of 4 μs (the minimum for this device) and a pixel time of 875ns (minimum time for line moves during readout, including 'overscanned' pixels = 0.48 ms).

The CCD02-06 has 288x385 image region pixels with pixel size 22 μm x 22 μm without any supplementary buried channel. The device type numbers are (both grade 2 image quality, with type number CCD02-06-2-954)

- A0723-51
- A3945-6

The devices were from different production batches. One CCD (AO723-51) has an electrode structure for standard inverted mode operation (IMO). This means that the image and store sections can be clocked in both the forward and backward directions. The other CCD (A3945-6) has an advanced inverted mode structure (similar to that of the CCD47-20 devices). It was originally thought that both were IMO devices but apparently there was some confusion at the manufacturer at the time of ordering. Both CCD02 devices have:

- a single readout register (and amplifier)
- no dump gate.
- no store shield deposited on the CCD. To form a store shield black tape is put on the glass window
- non-antibloomed structure

For highest speed operation the CCD02-06 was operated with a minimum line move time (during frame transfer) of 2.25 μs and a pixel time of 875ns (minimum time for line moves during readout, including 'overscanned' pixels = 0.37 ms). However to compare results with those for the CCD47-20 and to investigate likely performance for large format 22 μm x 22 μm pixel advanced IMO devices (e.g. the proposed EEV CCD55), the time for line moves during frame transfer was increased to 6.75 μs for some measurements and the line move time during readout was also increased by 'overscanning' a greater number of pixels so that the line length had a total of 1000 pixels (each read in 875ns).

3. TEST EQUIPMENT AND PROCEDURES

3.1 ASCOSS IMAGERS AND ADCS (CHARACTERISATION)

Figure 3-1 is a block diagram of the set-up used for characterisation of individual ASCoSS imagers and ADCs. The characterisation board has zero insertion pressure (ZIP) sockets, one for each type of device as well as current and voltage monitors on bias supplies also there are 6 BNC test points. For testing the ASCoSS chips over a range of temperatures the board can be mounted inside an evacuated cryostat with a heatsink fitted inside the ASCoSS ZIP socket and connecting to a liquid nitrogen cooled cold finger.

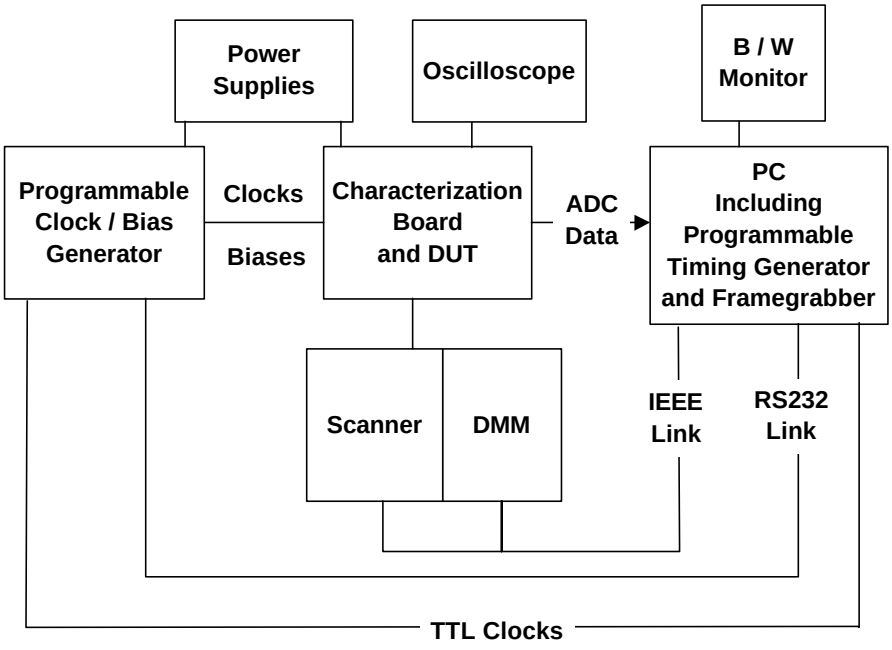

Figure 3-1 Block diagram of the characterisation system for ADCs and ASCoSS sensors

3.1.1 Characterisation board

A layout diagram for the characterisation board is shown in figure 3-2. The board can be set-up in various configurations using Links. These are used for example to switch between:

- bias voltages (ASCoSS or ADC) to be monitored
- external or internal voltage reference (for the ADCs)
- external (12-bit) or internal (8-bit) ADC for digitising the ASCoSS video output
- test input signal for the ADCs (ramp, external input, clock waveform from the timing generator, DC level or video output from the ASCoSS chip)

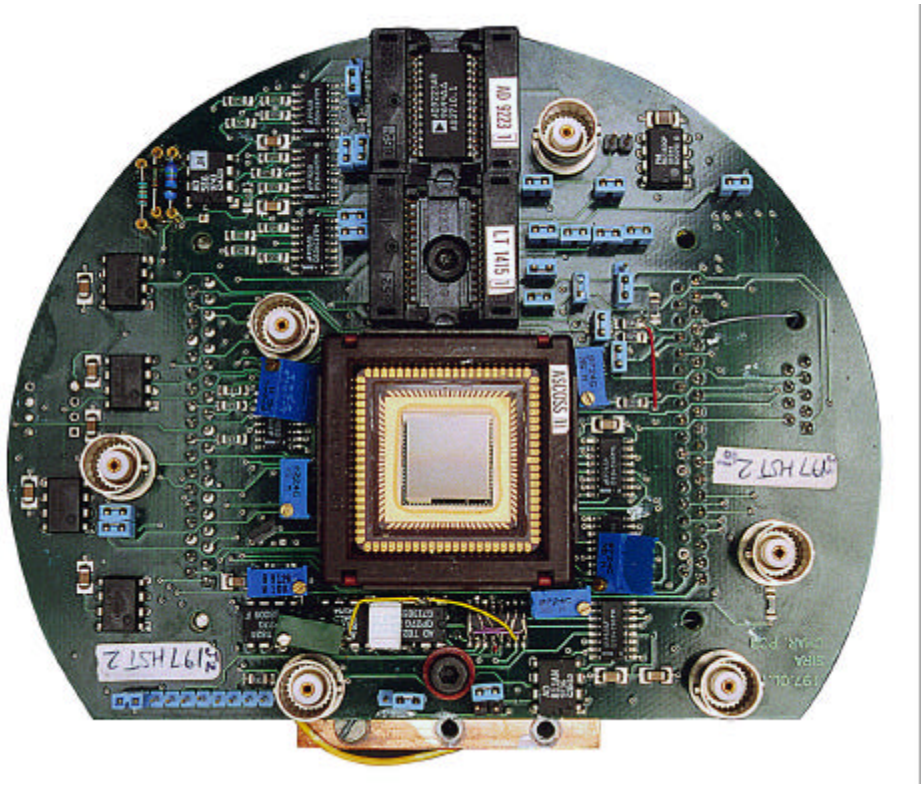

Figure 3-2 Photograph of the characterisation board for ADCs and ASCoSS sensors

Supply voltages and currents are monitored using a Keithley Model 2000 DMM with 2000-Scan 10 channel scanner and plus an auxiliary Keithley Model 705 scanner. This gives the ability to switch the DMM to measure up to 4 power supply voltages and currents and to monitor 12 bias voltages. These are relayed to the PC via an IEEE interface.

A typical output from the DMM, when the ASCoSS chip is being operated, is given below:

	Vdd1 (analogue ADC supply)	Vdd2 (digital ADC supply)	Vdd3 (analogue supply to pixel array)	Vdd4 (Vdd supply to sensor)
Current (mA)	36.345574	0.705711	2.393826	10.916250
Voltage (V)	4.992090	4.99694	4.99038	4.998060

rdadc	2.504897	bias for analogue part of ADC, connected via variable resistor to ground (alternatively this line can be linked to monitor ADC reference)
raadc	1.151087	bias for digital part of ADC, connected via variable resistor to Vdd1
vhadc	3.166130	high reference voltage of ADC
vladc	1.759740	low reference voltage of ADC
nbias	2.683336	output column source follower bias, connected via variable resistor to Vdd3

pbias2	3.623269	column source follower bias, connected via variable resistor to ground
obias	2.907608	output amplifier bias, connected via variable resistor to Vdd3
pbias1	2.721234	column amplifier bias, connected via variable resistor to ground
knbias	0.908969	column source follower bias, connected via variable resistor to Vdd3
dcv	0.000014	reference voltage for output amplifier, connected via a variable resistor to Vdd4 (set to 0 V)
vref	1.501342	reference voltage for column amplifiers, connected via a variable resistor to Vdd4
abgnd	1.001144	antiblooming ground, connected via a variable resistor to Vdd4

The characterisation board is supplied with TTL clocks from the programmable timing generator. The timing pattern can be varied so as to accommodate the particular clock patterns needed for each device and for operation of the ramp input signal generator. Within the timing file for each device there are also several switchable sequences for different operating modes. For example the integral and differential linearity ADC measurements require different ramp speeds for the input signal generator.

The timing waveforms are not supplied directly to the device under test (DUT) but via a programmable voltage generator. This allows both clock high and low levels to be varied under computer control. This is needed for measurement of the impact flatband voltage shifts. The programmable timing and clock/bias generators and other parts of the system are described in further detail below. Digitised data is passed directly to a framegrabber in the PC and processed using custom image analysis and commercial spreadsheet software.

The bias voltages used for the ASCoSS sensor (rdadc, raadc,….abgnd) are selected so as to optimise the analogue performance of the sensor (e.g. to match the video output to the internal ADC input) and are set up using potentiometers on the characterisation board (or via resistors to Vdd1,2,3,4 or ground). It is not proposed to change them during the testing, unless performance degradation requires them to be re-optimised.

For the characterisations the ADCs are used in single-ended (rather than differential) input condition. One input has the (variable) input signal the other input is static biased (at the manufacturer's recommended voltage level).

3.1.2 Programmable bias/clock generator

This unit contains 12- and 8-bit DACs for setting of bias and clock voltages (respectively). These are loaded via a Dallas DS5000 microcontoller (in the unit) and an RS232 interface to the PC. In these tests only the clock voltage high and low voltages are used since the supply voltages to the ADCs and ASCoSS sensors are a constant 5 V.

3.1.3 Programmable timing generator

The Timing Generator produces TTL level clock waveforms for the camera unit. It consists of a series of RAM-controlled sequencers. The number and frequency of pulses in a train and the grouping together of different trains to form the overall pulse sequence for the multiplexer are variable. Sequences are generated by typing user-friendly high level statements on the host computer to generate a file containing the sequence information. This file is then down-loaded to the RAM in the Timing Generator via the parallel printer port.

Because the pulse trains are variable, it is simple to generate the sequences necessary for driving a variety of arrays and for variation of integration time etc.

The Timing Generator operates at clock rates of up to 64 MHz. There are 23 separate output lines, thus allowing for control of external circuitry such as clamps, sample and holds and ADCs, as well as clocking the test objects.

In general it is possible to store several different complete sequences in the timing generator at any one time, though the number depends on their complexity. Hence the operator can switch sequences without reloading from the host computer. This is particularly useful for example when changing integration times.

3.1.4 Power supply

A set of bench power supplies are used for providing power to the characterisation board (±12V) and the programmable bias/clock generator (±15 V).

3.1.5 Computer and Framegrabber

This is a Pentium computer with 15 Mbyte RAM and 1.2 Gbyte hard disk with CD ROM writer. Slotted into the ISA-bus is a VS100 framegrabber/image memory card manufactured by Imaging Technology Inc. This is capable of capturing normal CCIR video signals or non-CCIR variable scan rate pictures up to a pixel rate of 10 MHz. The image memory is 1024 x 1024 x 12 bits deep. A 512 x 512 window of this memory can be output to the display at any one time. The variable scan rate pictures can be input either as digital data up to 12 bits deep (as in this case), or as an analogue signal to be digitised with an internal ADC. The internal ADC digitises to 8 bits.

3.1.6 Test Software

Sira has written system-level software that acts as an interpreter for the VS100 image memory board functions and allows these functions to be selected in a user-friendly manner and assembled together to form sequences for automated testing or data analysis.

Examples of functions available with simple commands are:

* image acquisition (either continuously or as single frames)
* pan and zoom
* image scaling and off-setting
* display of a cursor on the image display and readout of a matrix of pixel values on the computer console.
* cursor movement from keyboard or mouse
    - selection of points, lines, columns or areas of interest by keyed commands or by mouse
* calculation of mean and standard deviation of areas of interest and display of histograms. Also dumping of this data to a file
* recording of intensity profiles across slices through images
* detection of pixels above or below a set threshold (e.g. for analysis of image non-uniformity)
* adding or averaging successive images to reduce random noise
* addition, subtraction, division or multiplication by previously stored images
* statistical analysis of values from one pixel (or a group of pixels) from successive frames for noise analysis
* saving of image data, either in VS100 or standard TIF (tagged image file) format
* operations on input and output look-up tables (LUTs)
* loading of bias and clock supply voltages into the microcontroller memory in the camera head

Examples of operations are:

* definition of sequences or regions of interest and recording of mean, standard deviation etc.
* measurement of output signal as a function of bias or clock voltages
* interaction with the programmable timing generator so as to form linearity plots by successive changes in integration time and recording of image values from a specified region of interest.

3.2 ASCOSS IMAGER AND ADCS – OPERATION DURING IRRADIATION

A separate 'dose' board is used for mounting and biasing the devices whilst they are being irradiated during the cobalt 60 and heavy ion latch-up tests. This board is illustrated in figure 3-3. it is designed to fit in the standard frame used at the HIF (LLN) and PIF (PSI). There are six ZIP sockets for ASCoSS devices and 6 for each type of ADC. For latch-up tests the DUT is mounted on the centre line of the board (because of beam constraints at the irradiation facility). For cobalt 60 tests, all the devices at the top of the board are exposed simultaneously. The lower section of the board is used for drive/interface circuits which are shielded by the wall of lead bricks during the irradiation so as to reduce the dose which they experience. Voltages/currents can be continuously monitored during irradiation as for the characterisation board. For latch-up testing, the monitoring of the V_{DD} supply currents (and voltages) to each biased device is the only measurement (figure 3-3 shows the device bias conditions and monitor channel numbers). There are current limit circuits for the V_{DD} supplies to prevent damage to the devices in the event of latch-up. The current limit = 60 mA (approximately 3x the normal operating current). A scanning file will automatically step through the measurements with a user-defined repetition rate (minimum time to scan through the set of measurements = 30s). The scanning program signals a warning if the current limit is exceeded so that the latch-up can be recorded and the device reset (by power off/on).

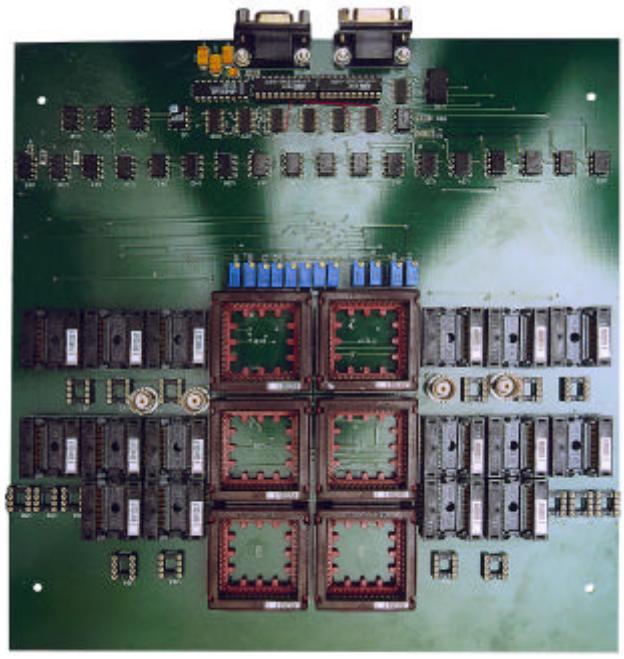

Figure 3-3 Photograph of the board used for supplying bias during cobalt60 and heavy ion irradiations

3.3 CLOCK/BIAS CONDITIONS DURING IRRADIATION

The 'dose' board internally generates the clock waveform needed to simultaneously clock the three device types. The (biased) ASCoSS chip is operated with simple continuous clocking which continually flushes charge out of the device (so as to mimic the dynamic bias condition in real use).

During irradiation there were:

- 4 ASCoSS devices dynamic biased (clocked)
- 2 ASCoSS devices unbiased (pins grounded)

For the ADCs, 6 devices of each type were irradiated simultaneously:

- unbiased (pins grounded)
- 2 operating (i.e. clocked) with both inputs static biased. In the case of the AD9223 both inputs were connected to the internal references voltage (V_{ref} is the recommended voltage for the non-signal pin used in single-ended operation and V_{ref} is also a convenient stable DC bias for the 'signal' pin).. In the case of the LTC1415 one input was connected to the internal reference voltage (via the REFCOMP Pin), the other to 0V (the recommended voltage for the non-signal pin used in single-ended operation).
- 2 clocked with one input static biased (as for the non-signal pin used in single ended operation), the other input dynamic biased.
- 2 clocked with both inputs dynamic biased (to mimic operation in differential input mode).

3.4 CCDS

Figure 3-4 shows a block diagram of the CCD characterisation system. This is based around the Sira Universal camera, which is a programmable bias/clock generator similar to that used for ASCoSS/ADC testing but with a wider range (and number) of voltages. In principle the Universal camera could have been used for ASCoSS/ADC testing but the unit actually used for that purpose was available and more suited to driving CMOS circuits. The functions of the other blocks are as described in section 3.2 above.

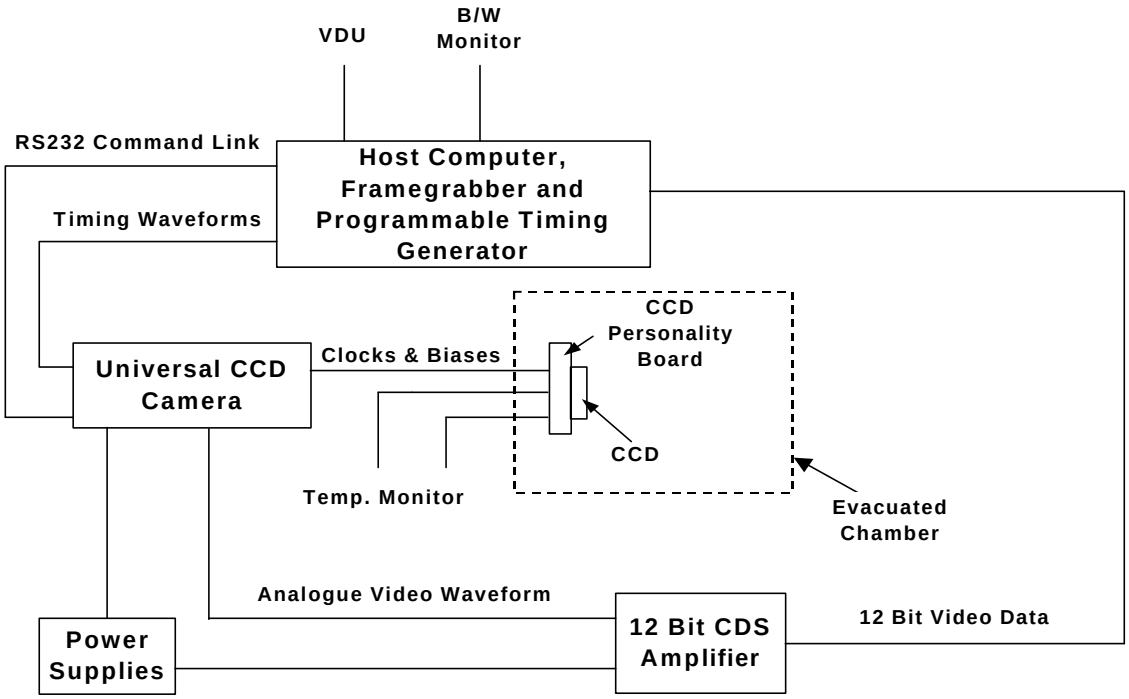

Figure 3-4 Block diagram of CCD test system

3.4.1 Sira Universal camera

The Sira Universal CCD Camera is a programmable bias and clock generator, which can be configured for driving any (or at least all known) types of CCD (as well as other types of solid state sensor array). CCDs are accommodated on separate personality (or daughter) boards, which plug into the 37-way D-type connectors on the camera backplane. The backplane also has a 9-way connector for relay of temperature monitoring signals from the daughter board to the front panel of the camera. The electronics unit contains the following PCBs:

- Video/controller

  This contains a Dallas DS5000 microcontroller (for loading of voltage configuration data through an RS232 interface), a high speed video amplifier and relays for switching between 4 different CCD output sources. The video amplifier has 9 programmable gain settings (x0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4 and 8).

- Bias board

  This has 8 12-bit programmable supplies. 4 of the biases have a high current capability (10 mA). All can have their currents monitored via a 3-pin miniature DIN connector.

- Area clock boards (2 off)

  For image and storage region (i.e. area) clocks. Each of the two boards has 4 clock drivers with separately programmable high and low levels. These can be set anywhere in the range -20 V to +20 V with 12-bit precision, provided that the clock swing (difference between high and low levels) is no more than 20 V. Each clock level can also be switched to an alternate voltage during the clock sequence. The slopes of the clock waveforms are also programmable.

- Line Clock boards (2 off)

  For readout register clocks. Each of the two boards has 4 clock drivers with separately programmable high and low levels and slopes. These can be set with 12-bit precision.

The Dallas microcontroller (on the Video board) is used to load values into the 12-bit DACs from a program 'unicam.exe' in the host AT computer and is then sent into 'sleep mode' with its internal clock turned off, so as to reduce pick-up. During operation the 'unicam' program can be used to change voltages and to perform other operations. For example:-

Command:-

unicam vod 12.5	sets the V voltage to be 12.5 V
unicam on/off	turns the camera on and off (with biases switched in a controlled sequence)
unicam mon vrd	allows current monitoring on the Vrd line
unicam gain 3	sets the gain of the camera to setting 3 (corresponding to x2)
unicam video 3	sets the output video channel (out of maximum choice of 4, channel 2 being 0 V)

3.4.2 CCD biases during irradiation

In this study, the interest in CCD irradiation is in displacement damage effects (in particular, CTE degradation). This is known not to have a significant bias dependence and so the proton irradiations were conducted with the devices unbiased (pins shorted using anti-static foam).

4. RADIATION HISTORIES

4.1 PROTON IRRADIATIONS

The proton irradiations were carried out on 7 December 1998 using a 10 MeV beam from the Tanned Van de Graaff accelerator at AEA Technology, Harwell. A dedicated beam line was available. This employed scatter foils (100 μm of gold) to produce a uniform beam (better than ±5%) over the sample area. The devices under test were mounted anti-static foam and irradiated unbiased, at normal incidence.

Beam monitoring was performed with a surface barrier detector positioned at an angle of 45 degrees to the beam axis, in a side-arm of the beam line, adjacent to the scatter foil. Before the test run this was calibrated against a Faraday cup (placed upstream from the chamber). Fluence measurements are considered to be accurate to better than ±5%. The beam flux was adjusted such that a typical exposure was 100 seconds.

The CCDs were masked using strips of aluminium, 1.5 mm thick, so that vertical bands (in the column direction) could be selectively irradiated (the penetration depth of 10 MeV protons in aluminium is ~ 600 μm). The fluence regions are shown in figure 4-1. For the CCD02-06 devices the right output amplifier is not present and the 2 krad step was omitted

The fluence regions corresponded to total doses of 0,2,4,10 and 30 krad (a fluence of 1.8 x $10^9$10 MeV protons /cm^2 corresponds to 1 krad(Si) total ionizing dose). For convenience, proton fluences will be expressed in this report in units of krad(Si) using this conversion factor, although strictly speaking, CTI being a displacement damage effect should always be related to proton fluence rather than total ionizing dose.

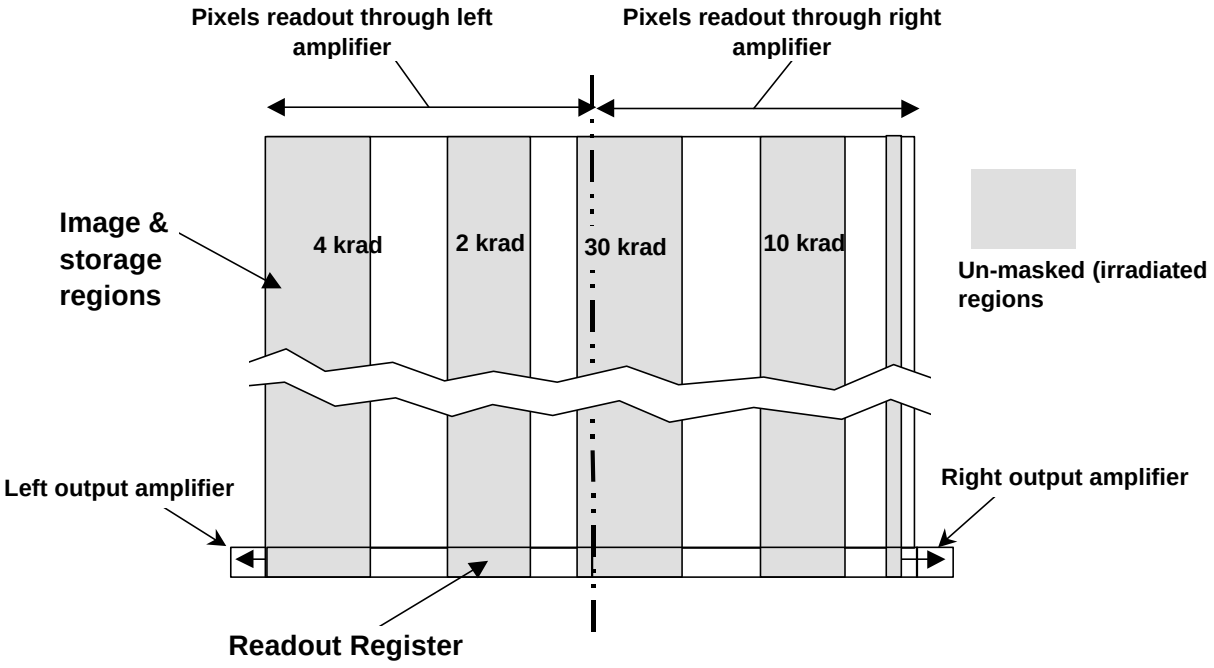

Figure 4-1 Dose regions on the two CCD47-20 devices. For the CCD02-06 devices the right output amplifier is not present and the 2 krad step was omitted.

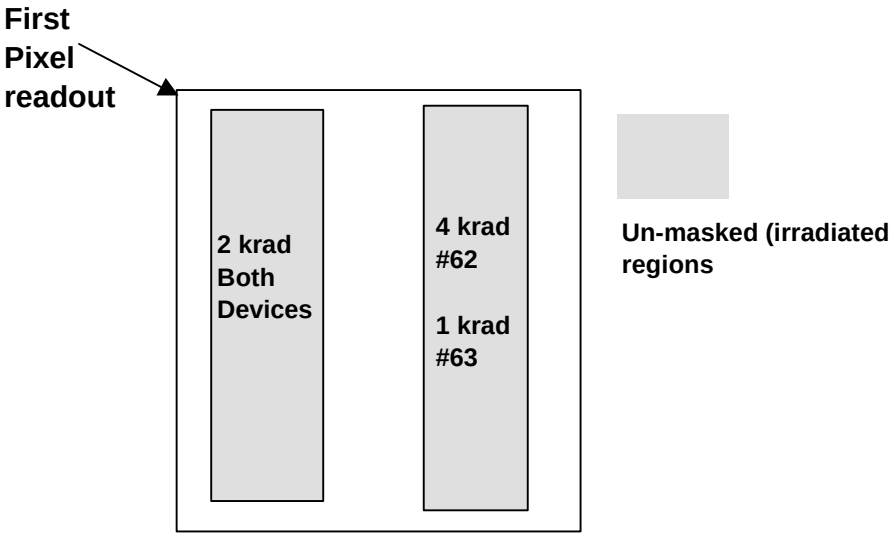

Figure 4-2 Dose regions on the ASCoSS devices

The ASCoSS imagers were masked so that the edges of the die, which contain the shift registers and ADC, were not irradiated. The masking is shown in figure 4-2. Device # 62 received 2 krad and 4 krad. Device #63 received 1 krad and 2 krad.

4.2 HEAVY ION LATCH-UP TESTS

Latch-up testing was performed at the Heavy Ion Facility (HIF) at Louvain-La-Neuve (Belgium) on 11 June 1999 with the assistance of ESTEC. The test equipment allowed the monitoring of individual device voltage supplies. When a latch-up event occurred the voltage supply was dropped so that the current was limited to 60mA. The value to which the supply voltage dropped could be read from the data log file. A power off/on cycle always recovered normal operation.

Two de-lidded of each ASCoSS and AD9223 device and one LTC1415 were tested (the CCDs were not latch-up tested). The following beams were used (but not all on each device, details for specific devices are given in sections 5 and 6):

$^{40}Ar^{8+}$ ions, (energy 150 MeV),	60° incidence	**LET 28.2 MeV/mg/cm^2**
$^{40}Ar^{8+}$ ions, (energy 150 MeV),	normal incidence	**LET 14.1 MeV/mg/cm^2**
$^{40}Ar^{8+}$ ions, (energy 150 MeV),	45° incidence	**LET 19.9 MeV/mg/cm^2**
$^{20}Ne^{4+}$ ions, (energy 78 MeV),	60° incidence	**LET 5.85 x 2= 11.7 MeV/mg/cm^2**

4.3 COBALT 60 IRRADIATIONS

The cobalt 60 irradiations were performed at ESTEC during the period 21-24 September 1999. Devices were mounted on the dose board during irradiation and biased as appropriate. Individual

devices were inserted into the characterisation board for testing after each dose step. Because of the detailed nature of the post irradiation tests, it was not possible to complete these within one hour of each irradiation, however it was determined that post irradiation annealing was slow enough that the results were not significantly affected by the measurement time. The dose rate used during the irradiations was in the range 0.26 to 2.6 krad(Si)/hr. The following dose steps were performed:

Devices irradiated	Dose step Krad(Si)	Exposure time hours	Dose rate krad(Si)/hour	Total accumulated dose on ASCoSS devices	Total accumulated dose on ADCs
All ASCoSS	2.0	0.77	2.6	2.0	-
All	4.0	15.1	0.26	6.0	4.0
All, except ASCoSS #s 43, 54, 75	15.2	15.8	0.96	21.2	19.2
ADCs, except #s 6 and 7 (both types)	47.0	18.1	2.6	-	66.2

The dose was measured in krad(water) using an ionization counter calibrated at ESTEC. Values were multiplied by a factor 0.91 to convert to krad(Si). The dose values are believed to be accurate to ~ 5%.

The irradiations were performed at ambient room temperature.

Not all devices were given the full irradiation dose. ASCoSS devices #s 43, 54 and 75 were removed after 6 krad and were not given the final 15.2 krad dose step and ADCs #6 and #7 (both types) were removed after 19.2 krad and were not given the final 47 krad dose step.

After the irradiations and immediate post-irradiation measurements the devices were returned to Sira, where further post-irradiation and annealing measurements were made. Annealing took place for 168 hrs at room temperature and a further 168 hrs at 100 °C , with bias supplied (as during irradiation) by the bias board (i.e. devices not biased during irradiation were not biased during annealing). All the ADCs, but only ASCoSS devices #25 and 84 were annealed.

5. ASCOSS CMOS IMAGER RESULTS

5.1 SIGNAL CONVERSION GAIN

In the ASCoSS imagers (as in a CCD) the generated charge (either from photon absorption or from thermal generation) is dumped onto the capacitance of the pixel amplifier during readout

and hence is converted to an output voltage. This voltage was then digitised, either by the on-chip 8-bit ADC or by an off chip AD9223 12-bit ADC. For detailed performance measurements the off chip (12-bit) ADC was usually used. In order to convert digitised signal values to detected charge in electrons it is necessary to know the conversion gain (in electrons/ADC unit or ADU) for the system. In general there are a variety of ways that this can be measured experimentally but none of these were found to be applicable in this case:

X-ray calibration is a common technique with CCDs (point events are generated corresponding to signals of 6000 electrons/event), however it was found that events could not be observed with the ASCoSS devices – probably because point events are only generated within the pixel depletion region and this occupies only a small fraction of the pixel area. Events from the remainder of the pixel volume are spread out by diffusion and could not be observed above the read noise.

- The mean-variance technique can be used with any imager. The method relies on the square root (Poisson) relation between noise on the signal and signal value (both in electrons), however it does not work reliably in the presence of electrical pick-up and could not be used in this case.

- In CCDs it is possible to measure both the digitised signal and the current flowing into the reset drain of the output amplifier (which gives the total number of electrons collected within the integration time). The reset drain connection is not available with the ASCoSS chip.

Hence calibration can only be made by calculation using the design values for the pixel amplifier capacitance and gain (from IMEC) and the gain of the off-chip electronics.

Since none of the above methods were applicable, the IMEC design data was used. This gives an on-chip charge to voltage conversion factor (CVF) of 8.5 μV/electron and a full well capacity of 1.2 V (corresponding to 142,000 electrons). It was also known that the 12-bit ADC full range (4096 bits) is 5.00 V and the off-chip gain was 3.2. These values give an output CVF of 8.5*3.2 = 27.2 μV/electron at the ADC corresponding to

$$\underline{\text{conversion gain} = 45 \text{ electrons /ADU}}$$

This gives a full well signal of 142,000 / 45 = 3155 ADU which was as observed (within device to device variations).

A check to confirm that the above value is reasonable was made using an ^{241}Am alpha particle source. This gives alpha particles with energy 5.47 MeV. An ASCoSS chip was de-lidded and operated in a vacuum with the source (a disc 16 mm in diameter) mounted a few mm from the front surface. The initial (start-of-track) energy loss for the alphas in silicon is 232 keV/μm (from the TRIM code). The energy loss will increase as the particles slow down. The smallest events will be for normal incidence and the event size for a 17 mm epitaxial layer is estimated to be 7.3 x 10^5 electrons. The average event size will be larger than this because many of the tracks will be slanting – the source is 16 mm diameter and is mounted ~ 3mm in front of the CCD. On

the other hand, the maximum energy that can be deposited is the full energy of the particles: i.e. 5.47 MeV (corresponding to events of 1.52 x 10^6 electrons). The average event must there fore be between the two values and will be taken as 1 x 10^6 electrons, which corresponds to tracks close to 45° to the normal.

The recorded images showed easily detected alpha events. These were spread over several pixels because of charge diffusion in the silicon (as mentioned above). Hence the peak signal/pixel was reduced to close to the full well capacity. Results for device #62 are shown in figure 5.1-1 below. It is seen that pixel signals extend up to the full well capacity but there is no 'pile-up' at the maximum signal – which would indicate saturation. Hence it is thought that, though the average event size may be somewhat reduced due to saturation effects, the value should not be far in error. This average event size was estimated by calculating the average signal in an image, subtracting the dark level (in this case about 300 ADU) and dividing by the number of events. This was done for several images and the average event size was found to be 24,900 ADU. This gives a conversion gain of ~ 1 x 10^6 / 24,900 = 40 electrons/ADU which is close to the value calculated above. Figure 5.1-2 shows some typical alpha events.

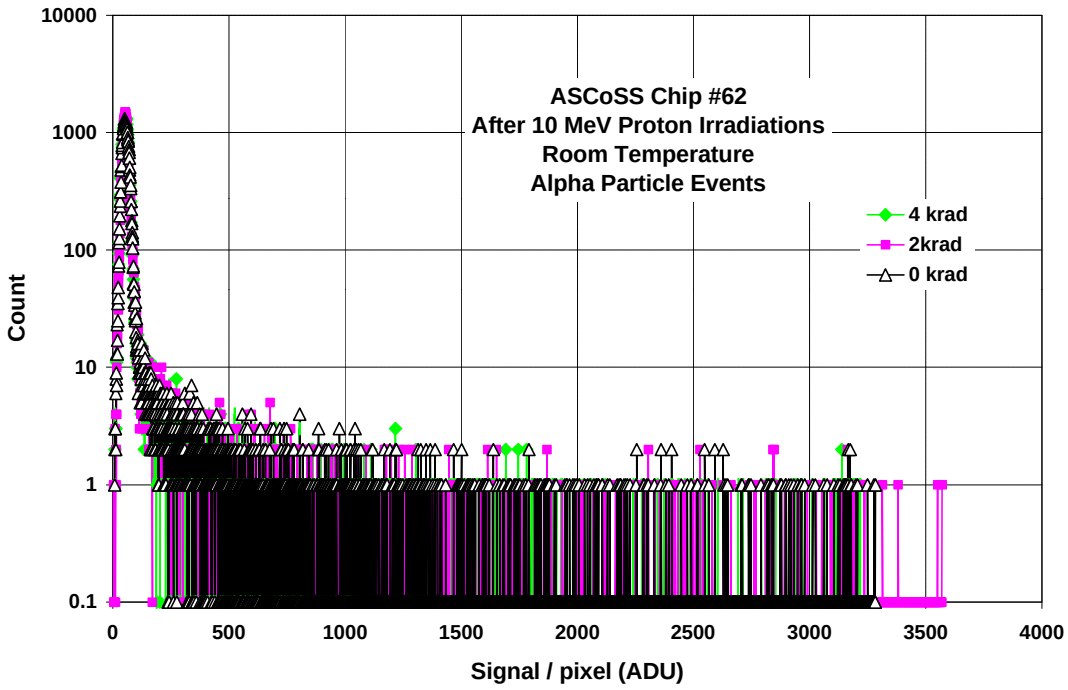

Figure 5.1-1 Histograms of pixel signals for images obtained during alpha particle bombardment (dark level subtracted). The three plots correspond to regions of the device given 0, 2 and 4 krad 10 MeV proton irradiation.

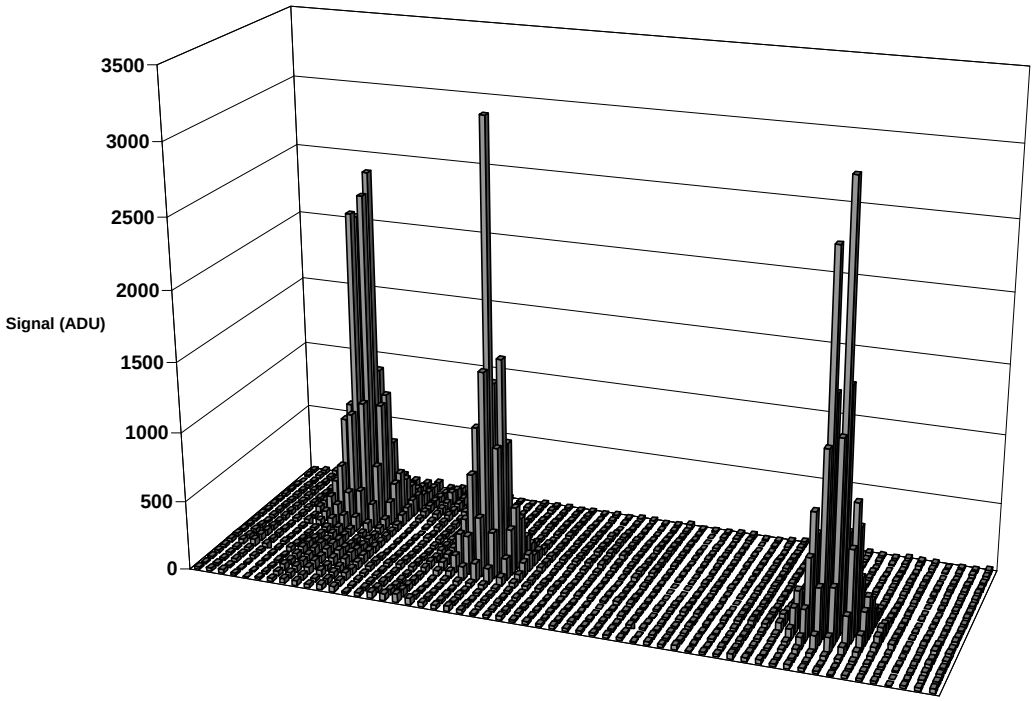

Figure 5.1-2 Alpha particle events

5.2 DARK SIGNAL MEASUREMENTS

With APS devices it is important that dark signal measurements take into account both 'fixed pattern noise' (FPN) and thermal dark signal. As is usual, we define FPN as the dark signal non-uniformity arising from 'electronic' effects such as feedthrough of clocks from the horizontal and vertical address lines. This feedthrough produces negligible non-uniformity in CCDs (though it can produce a constant offset) and so is usually neglected. In APS devices, however, it can be a significant component.

The FPN non-uniformity does not usually depend on integration time and varies only slowly (if at all, with temperature). Hence the 'thermal' and 'electronic' components of dark signal can be separated: the dark signal at low temperature and short integration times should be a good representation of the electronic FPN. This was indeed found to be the case with the ASCoSS chips. In the regime were the thermal dark signal is small (because of low temperature and short integration times), the non-uniformity was still significant but was found to be essentially independent of temperature and integration time. Figure 5.2-1 shows three dark signal maps from a small region of device #62. Two of the maps were obtained at 10 °C and –9.0 °C and the third (right hand block) gives the difference (offset by 70 ADU for clarity). It can be seen that the difference image has a lower non-uniformity than either of the originals: indicating that the originals are correlated. There is still some non-uniformity in the difference image however so the FPN is probably not entirely independent of temperature. There is a 'grid' pattern in the fixed pattern noise which can be seen in the images by eye but the FPN for full frame images is in fact quite low. The RMS non-uniformity was of the order of 5 ADU (or 230 electrons).

This is still large enough that accurate analysis of thermal dark current requires subtraction of FPN at each temperature (we have seen that there is a small change with FPN with temperature so it is best to take an FPN image at each temperature). Subtraction would also be necessary in a star tracker application if the lowest noise is required. The ASCoSS chips have a special feature to allow this. Short integrations (down to 1/512 of the full frame readout time) can be performed by resetting a line of pixels just before they are readout (see section 2.1). In this way a true 'dark' image can be obtained even when viewing a star filed. In fact subtraction of this dark frame will also subtract out thermal dark spikes. However the present chip implementation contains a design error which results in a high fixed pattern noise when short integrations are used and the FPN for different integrations is not correlated (though, as figure 5.2-2 shows, this higher FPN is still fairly constant with temperature and for varying integration times *longer* than the full frame read time).

In the analysis of thermal dark current non-uniformity it was found to be important *not* to use a short integration exposure to subtract FPN but to use a full readout time image (obtained at reduced temperature so that it did not contain thermal dark signal). Further illustration of FPN subtraction effects will be given below.

The FPN was found not to change significantly with proton radiation – remaining at ~ 5-6 ADU after 4 krad 10 MeV protons (7.2 x 10^9 p/cm^2). There was also no evidence of any significant change after cobalt60 irradiation (up to the maximum total dose of 21 krad(Si)).

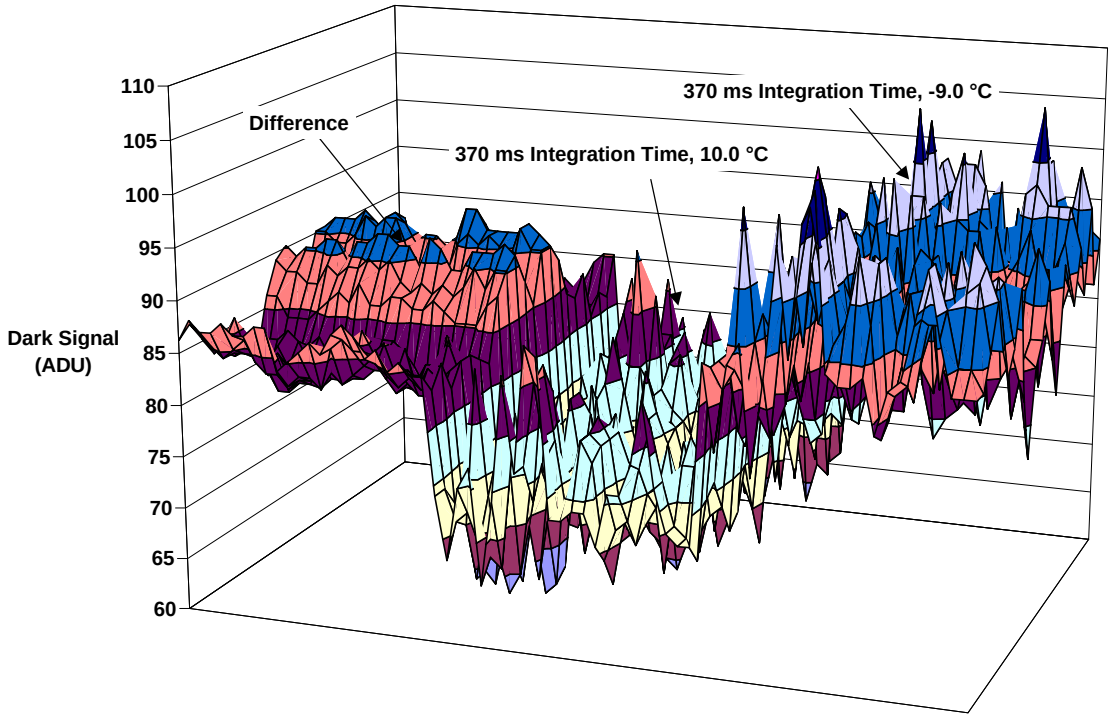

Figure 5.2-1 Fixed pattern noise for a typical block of pixels on a typical ASCoSS chip (#62) *NOT using short integration time mode.* The difference image has lower non-uniformity, showing that the FPN changes little with temperature

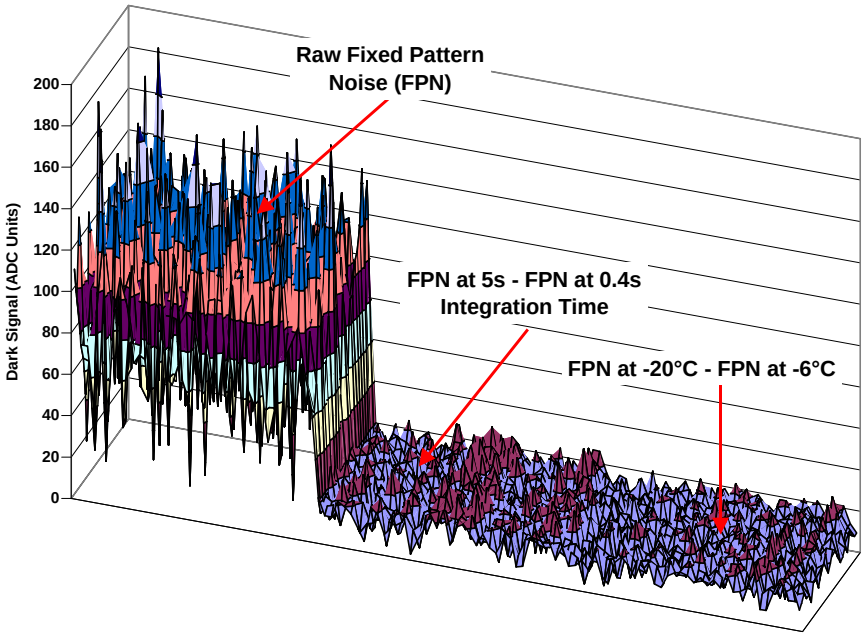

Figure 5.2-2 Fixed pattern noise for a typical block of pixels on a typical ASCoSS chip (#63) *using short integration time mode*, so the FPN is higher than in figure 5.2-1. The difference image has lower non-uniformity, showing that the FPN changes little with temperature

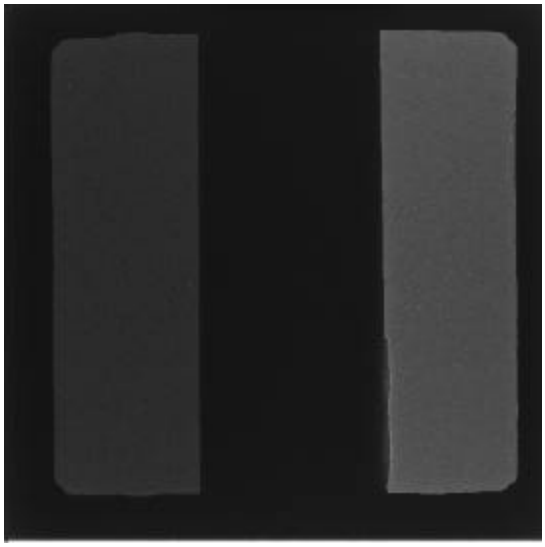

Figure 5.2-3 Dark image from chip #62. The dose regions (from left to right) are 2 krad, 0 krad and 4 krad 10 MeV protons, the periphery of the chip was masked and received 0 krad.

Now we turn to the analysis of thermal dark signal. The proton irradiated devices were characterised after approximately 6 months storage, unbiased at room temperature and so reflect performance after long-term annealing. Averages of 16 images were recorded for a variety of temperatures. The images show increases in mean dark level (due to total ionizing dose) and dark current spikes due to displacement damage. Figure 5.2-3 shows a typical image. The spikes are localised to single pixels (unlike optical or alpha particle events which are spread over several pixels, as discussed above). This indicates that the dark signal is created within the depletion region of a diode (as expected – only defects which occur in the depletion region will be active in generating dark current). Figure 5.2-4 shows typical dark current spikes and figure 5.2-5 shows a histogram of dark current density values at -20°C (with fixed pattern noise subtracted).

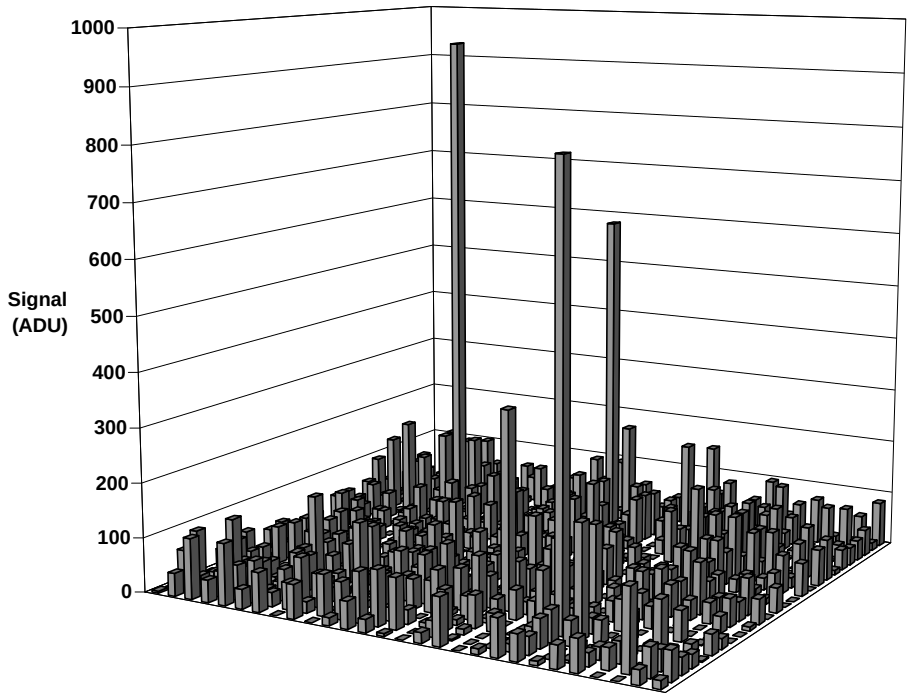

Figure 5.2-4 Typical proton-induced dark current spikes for an ASCoSS chip after 1.8 x 10^9 p/cm^2 (#63, 1 krad). Unlike photon or alpha particle signals (c.f. figure 5.1-1) the proton spikes tend to be localised to a single pixel

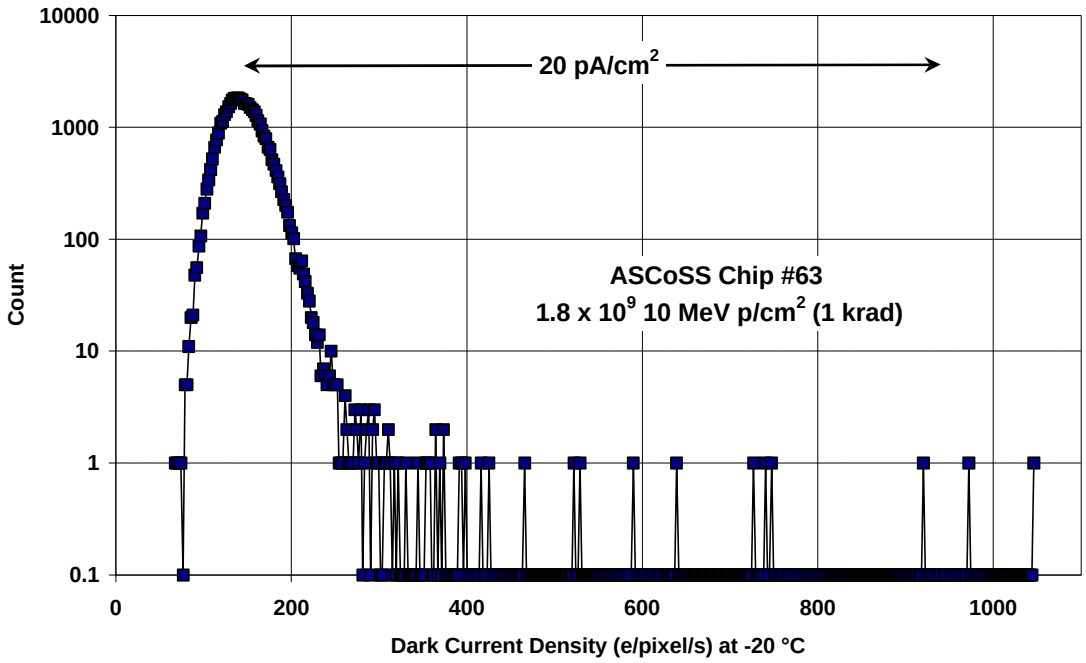

Figure 5.2-5 Histogram of dark charge density at –20 °C after 1 krad 10 MeV protons

Note that, as with CCDs, proton spikes can be seen even after low proton fluences. Increasing the fluence tends to broaden the main peak and will also tend to increase the number of large spikes, however at the fluences used there are only a few large spikes in each dose region. Figure 5.2-6 shows histograms at 10 °C for all the dose regions on both devices: 0, 1, 2 and 4 krad. The number of large spikes is similar to that found previously for CCDs. The amplitude of the largest spikes is also similar, though perhaps somewhat less (one or two thousand electrons/pixel/s at –20 °C rather than two to four thousand electrons/pixel/s for a typical n-channel CCD at the same temperature).

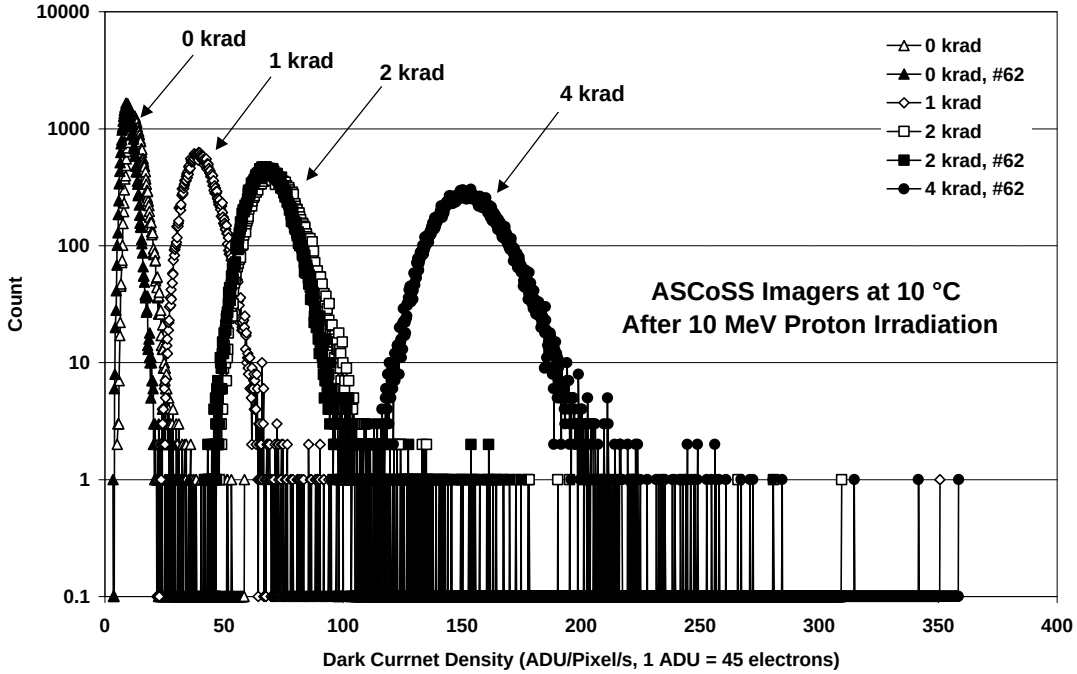

Figure 5.2-6 Histograms of dark current density at 10 °C
Filled circles are for device #62, open circles are for device #63.

It was found that the proton induced dark current for the ASCoSS chip varied with temperature in much the same way as it does for a CCD. That is:

- the width of the main peak scales with temperature in the normal way for silicon: with an activation energy of ~ 0.63 eV. This is illustrated in figure 5.2-7, which shows dark current histograms obtained at three temperatures (10.0, -9.0 and –20.3 °C) all scaled to the value that would be obtained at 10 °C, assuming an activation energy of 0.63 eV. There is a good super-position of the plots, indicating that this assumption is correct.

- there is a tendency for the brightest spikes to vary more slowly with temperature. Figure 5.2-8 shows the spike size as a function of temperature for the brightest spikes in device #63. Figure 5.2-9 shows the corresponding activation energy as a function of spike size. The brighter spikes tend to have a slightly lower activation energy. This behaviour is indicative of field-enhanced emission.

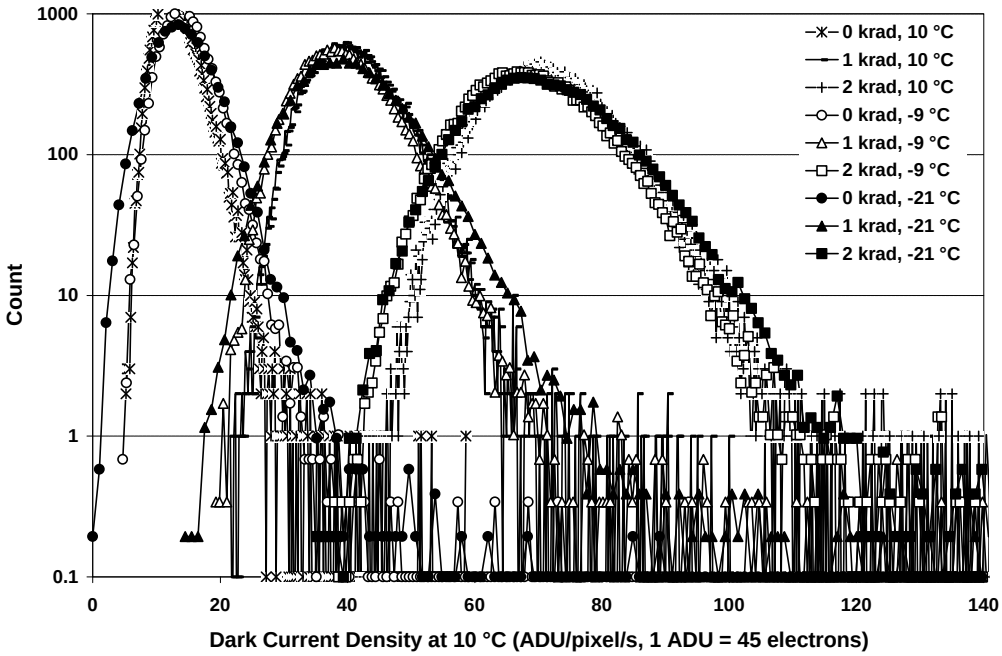

Figure 5.2-7 Histograms of dark current density obtained at three temperatures (10.0, -9.0 and –20.3 °C) all scaled to the value that would be obtained at 10 C, assuming an activation energy of 0.63 eV. There is a good super-position of the plots, indicating that this assumption is correct.

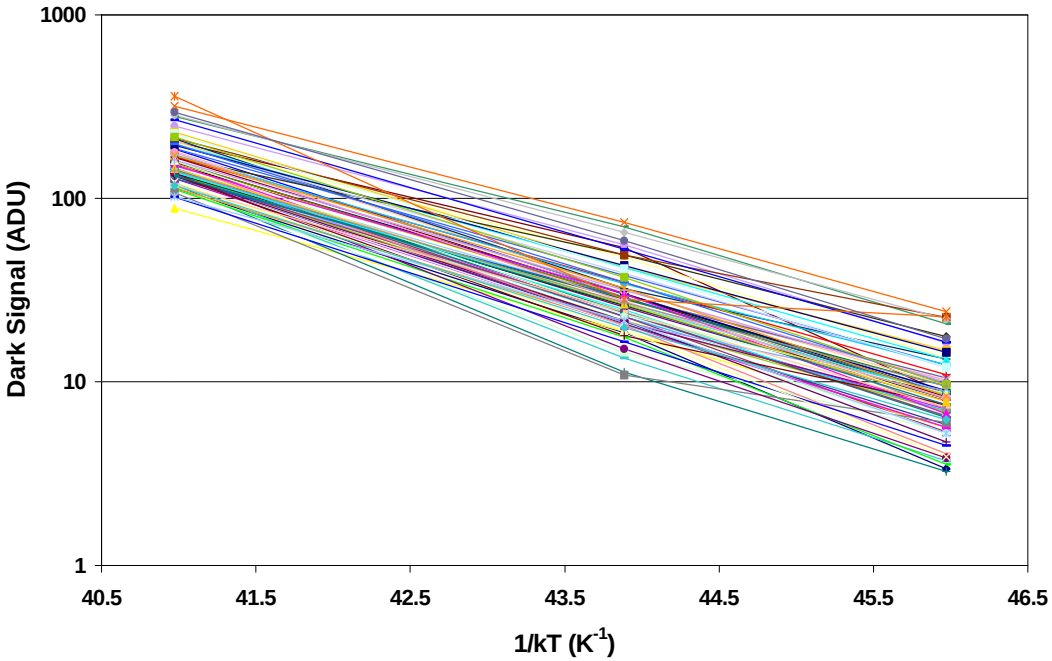

Figure 5.2-8 Spike size as a function of temperature for the brightest spikes in device #63.

Note that if short integration times are used to derive the fixed pattern frame to be subtracted then this leads to a much wider histogram, whose RMS value does not change much with temperature and the scaling shown in figure 5.2-7 does not work (c.f. figure 5.2-10).

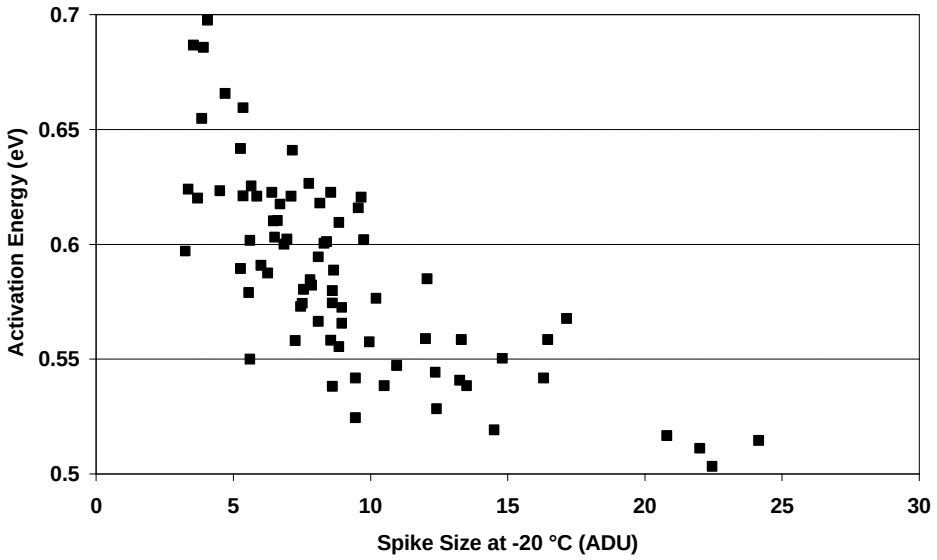

Figure 5.2-9 Activation energy as a function of spike size from the data of figure 5.2-8.

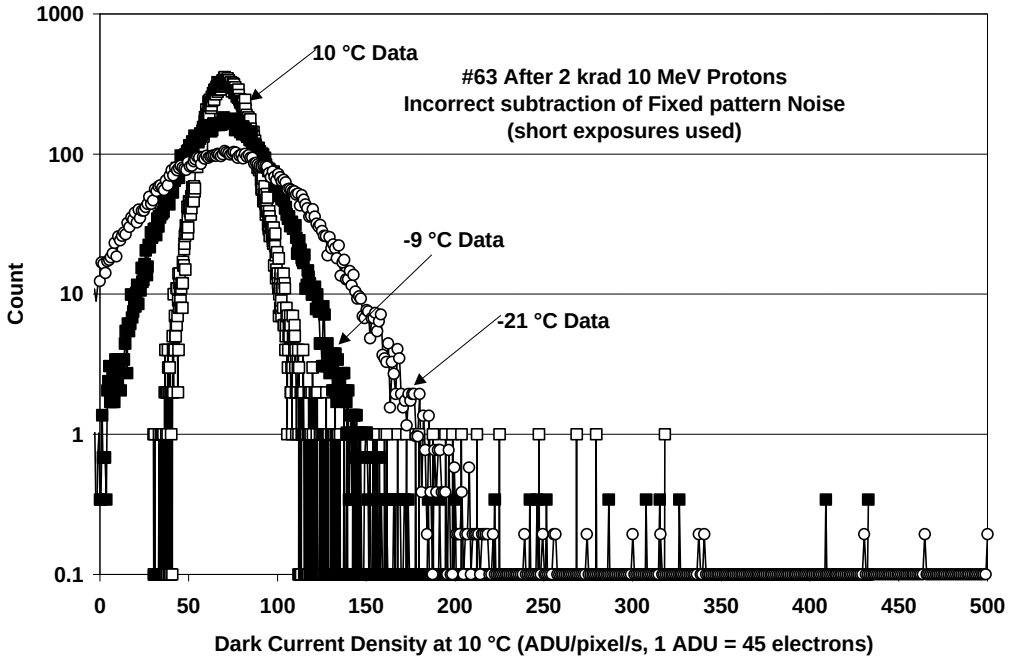

Figure 5.2-10 Histograms of dark current density obtained at three temperatures(10.0, -9.0 and –20.3 °C) all scaled to the value that would be obtained at 10 C, assuming an activation energy of 0.63 eV. There is a *poor* super-position of the plots because one-line-time (i.e.) short exposures were used to derive the fixed pattern image that was subtracted.

It can be seen that some of the spikes plotted in figure 5.2-8 behave in an erratic way. Further investigation of these pixels showed that, in the same way as in CCDs, these pixels show ***random telegraph behaviour***. Figure 5.2-11 shows typical plots obtained at 35°C. Note that the plots show true dark signals in ADU, they have not been shifted in offset. Some of the pixels show large percentage fluctuations, unlike the CCD case where the RTS amplitudes are at most ~ 10% of the spike size.

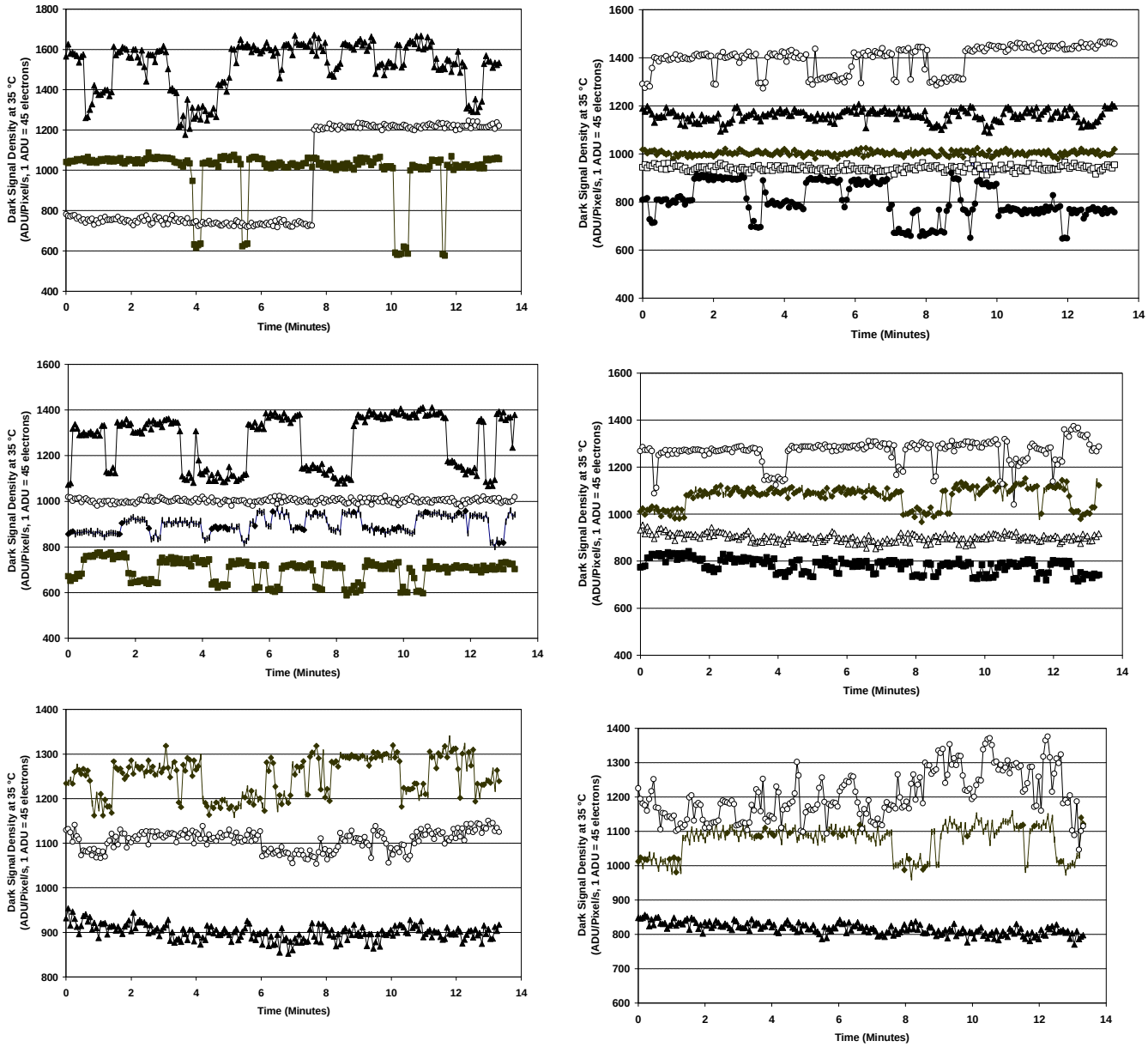

Figure 5.2-11 Plots of random telegraph signals from ASCoSS device #63 obtained at 35 °C. Note that the plots show true dark signals in ADU, they have not been shifted in offset.

In contrast to the dark current spikes produced by protons, the dark current induced by cobalt60 gamma ray irradiation is much more uniform. In some cases some 'shading' of the dark current was noticed: the dark signal tending to be higher near the top and bottom of the image, but otherwise the dark images were uniform with RMS values in the range 1.3 to 3.8 % before and after irradiation and after annealing, with most RMS values being ~ 2%.

Figure 5.2-12 shows the evolution of the mean dark current level (at 25°C) with total ionizing dose and annealing. It is seen that the dark current increases moderately at low doses but then shows a large increase, but this then anneals slowly at room temperature and almost completely after 1 week at 100°C. The eventual value is not far removed from the level extrapolated from the proton-irradiated devices measured after 6 months storage at room temperature. The bias condition during irradiation (and annealing) does not seem to have any significant effect on the behaviour.

Figure 5.2-13 shows that the mean dark current level (in this case, measured before annealing) changes with temperature in the normal way for silicon (with an activation energy ~ 0.63 eV). Hence the dark current seems to be thermal in origin. If it were due to leakage currents then it would not be expected to show such a strong change with temperature.

It is speculated that the large dark current increase occurring above ~ 6 krad may be due to flatband shifts causing inversion of the surface and an increase in the depleted area (and hence in surface dark current). The flatband shift then anneals and so the dark current decreases.

The annealing behaviour indicates that mean dark current shifts will not be severe for the low dose rate space environment (where long-term annealing will occur). In any case, cooling of the device is effective in suppressing the dark current.

Note that these results do not agree with previous results from IMEC on other CMOS imagers, presumably because of differences in the pixel design.

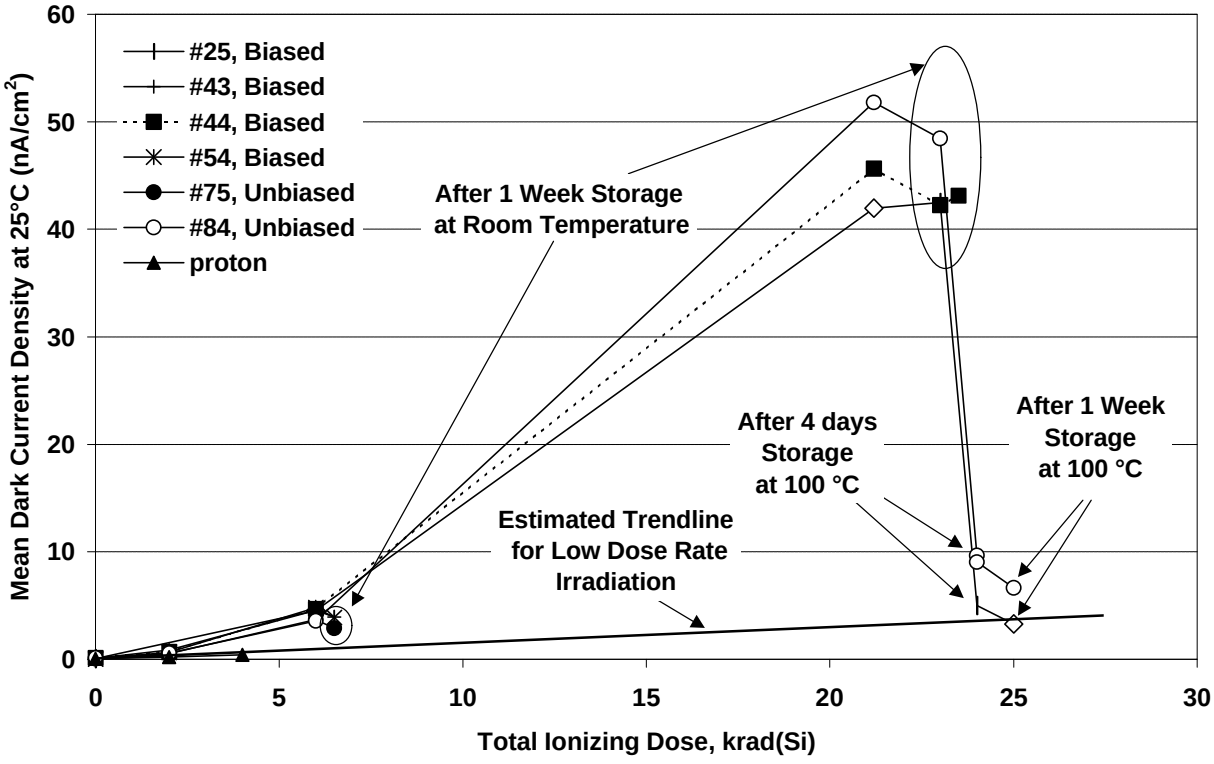

Figure 5.2-12 Evolution of the mean dark current level (at 25 °C) with total ionizing dose and annealing

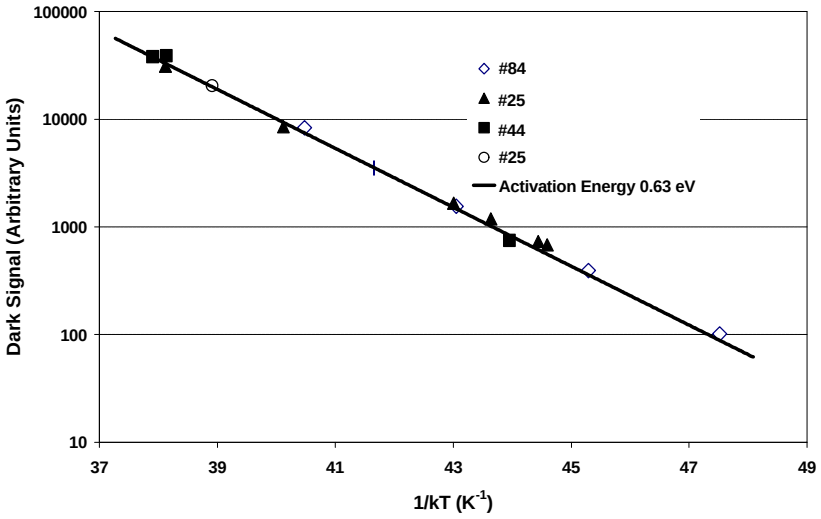

Figure 5.2-13 Variation in mean dark charge level with temperature

5.3 POWER SUPPLY CURRENTS

Section 3.1.1 gives a list of the bias supply currents and voltages that could be monitored. The bias voltages are supplied via resistors so any changes would indicate a change in the current being drawn on a particular pin. During the irradiations only the sum of the two ADC supply and the two sensor currents were monitored (sum of Vdd1 and Vdd2 currents and the sum of Vdd3 and Vdd4 currents) but for post irradiation measurements, all the individual supplies were measured. Figure 5.3-1 shows the evolution of the summed supply currents during and after irradiation (only the biased devices were monitored), figures 5.3-2 to 5.3-4 show the individual power supply currents and figures 5.3-5 to 5.3-7 the supply voltages.

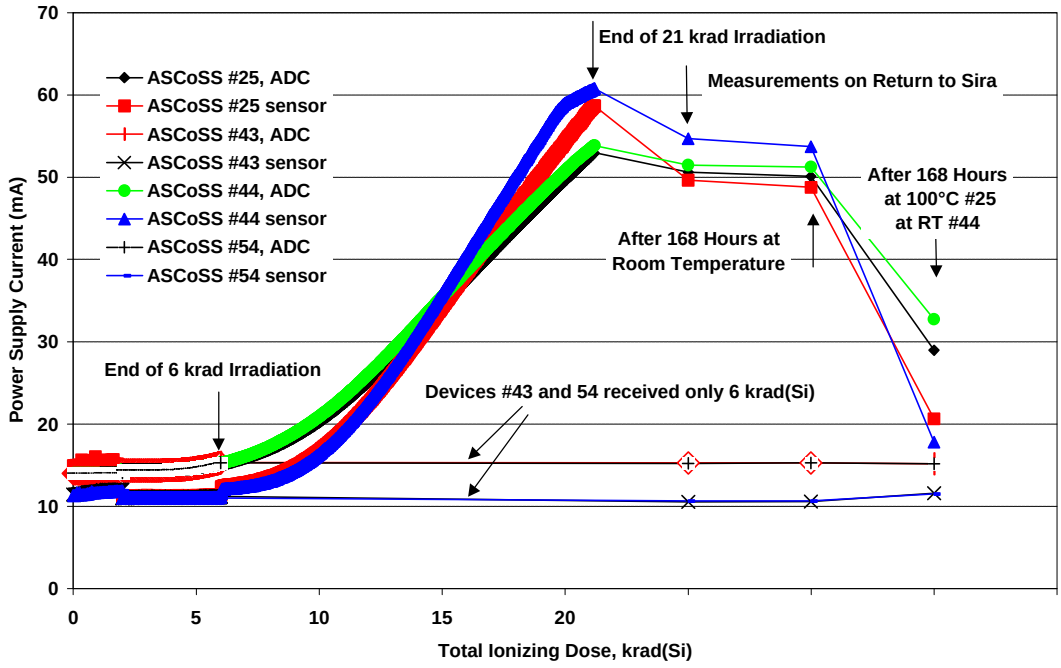

Figure 5.3-1 Evolution of the summed supply currents during and after irradiation (only the biased devices were monitored)

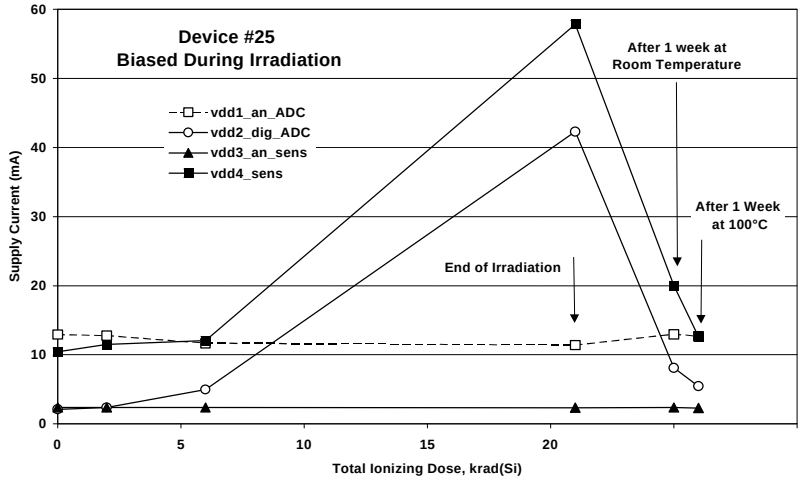

Figure 5.3-2 Power supply currents for device #25, biased during irradiation

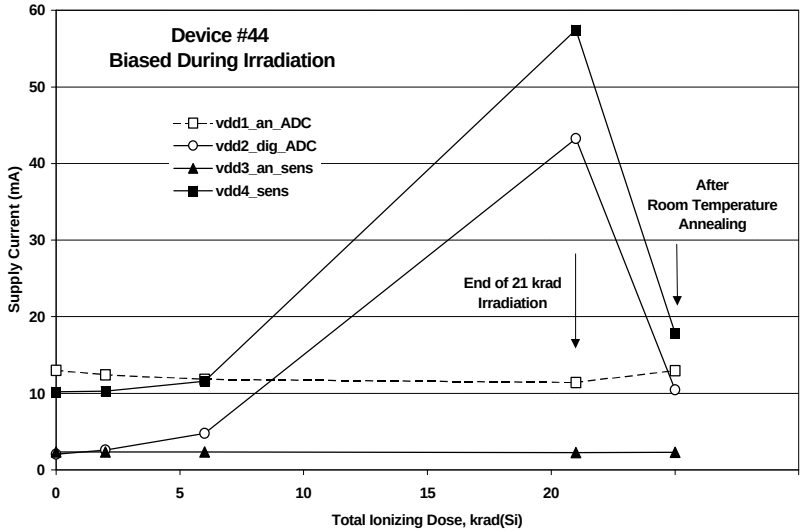

Figure 5.3-3 Power supply currents for device #44, biased during irradiation, not baked at 100°C

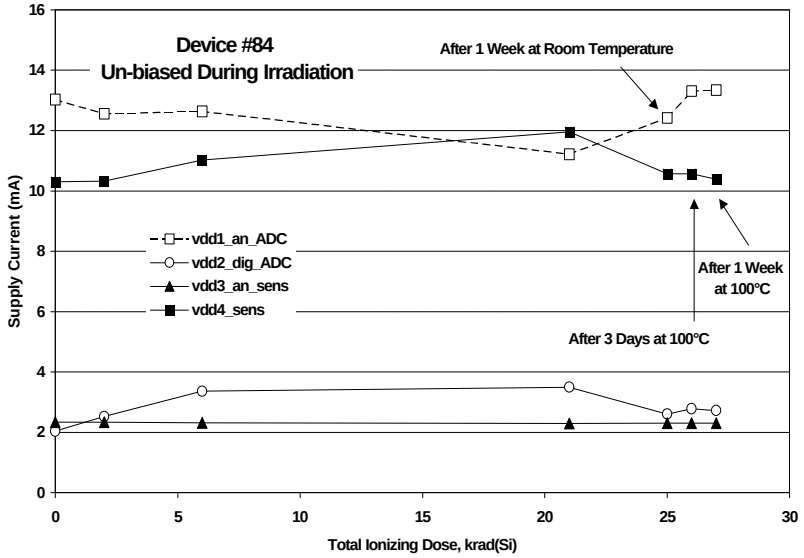

Figure 5.3-4 Power supply currents for device #84, un-biased during irradiation

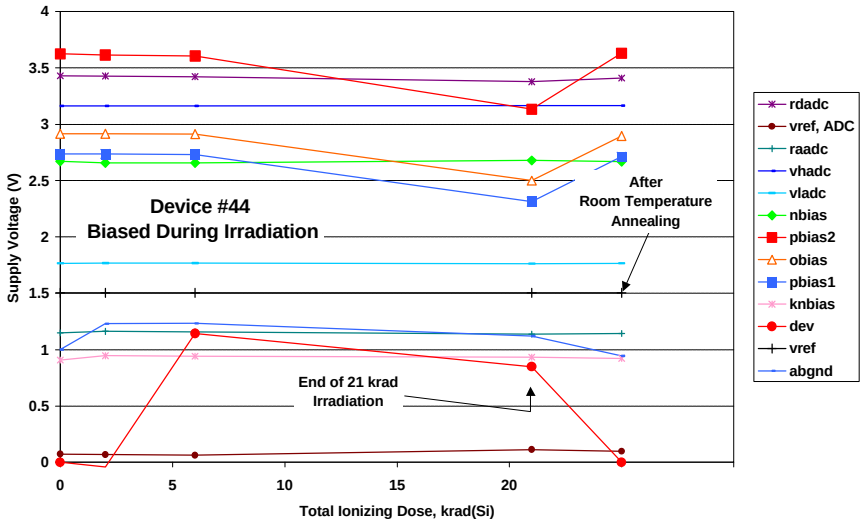

Figure 5.3-5 Supply voltages for device #25, biased during irradiation

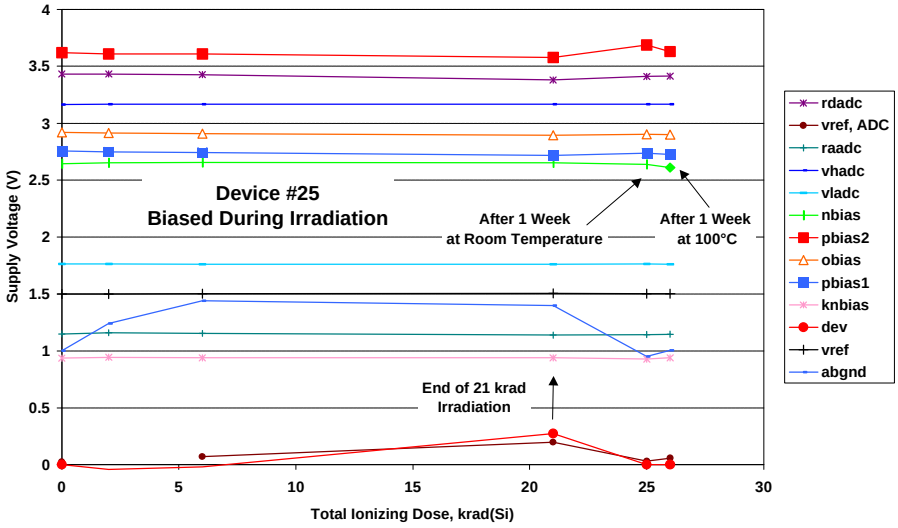

Figure 5.3-6 Supply voltages for device #44, biased during irradiation, not baked at 100°C

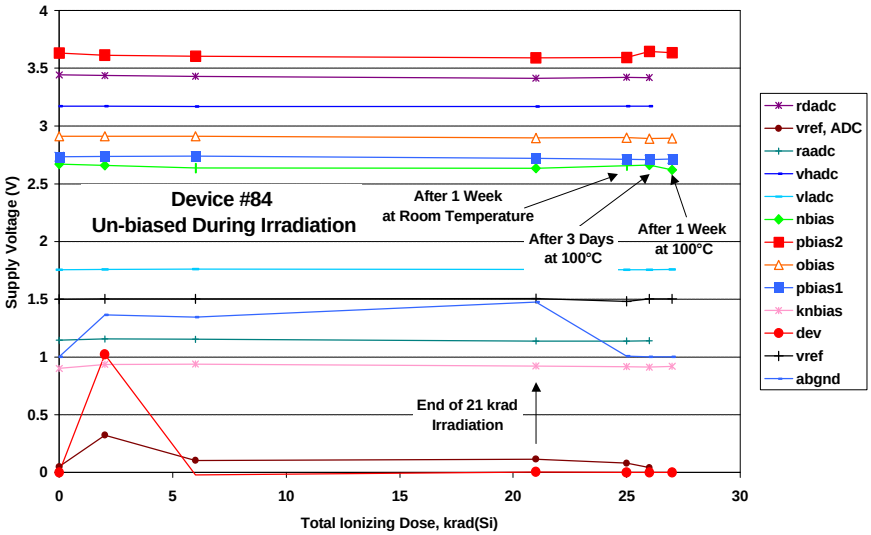

Figure 5.3-7 Supply voltages for device #84, un-biased during irradiation

Several conclusions can be made:

- There is a sharp increase in the Vdd1 (digital ADC) and Vdd4 (sensor) supplies after 6 krad(Si) for biased devices (but not the un-biased). This results in an increase of the summed currents (monitored by the dose board). At the end of the 21 krad irradiation the currents were so high that the current limit to the board was nearly exceeded (it can be seen that the summed Vdd3 and 4 sensor currents, in figure 5.3-1, flatten off at the end of the irradiation because the power supply is just starting to 'fold back'). This level of current was high enough that significant heating of the device occurred during operation. Higher radiation doses without a current limit could potentially cause device damage: this may have happened with the earlier IMEC tests on IBIS 1 devices.

- There is significant post-irradiation annealing, with the currents returning close to their pre-irradiation levels. However the annealing occurs at a somewhat variable rate: device #44 annealed with room temperature storage, whereas #25 needed a bake at 100°C.

- The bias supplies were not greatly affected by the irradiation. There were some small changes in particular supplies but these annealed out. The ADC reference voltage (a critical parameter) remained unchanged.

It is possible that parasitic leakage paths (e.g. in a field oxide) are being turned on just above 6 krad(Si) and that this causes the increase in current. Annealing of this flatband shift would result in a sharp return to normal current levels.

5.4 FLATBAND VOLTAGE SHIFT

Changes in flat band shift for the gate oxides were monitored by varying the ADC CLOCK, ADC CLOCK_XRD and ADC SYNC_XRD signals. These supply the three different types of input gate structure used on the device. The changes induced by the cobalt60 irradiation were small (of the order of 0.2 V or less after 21 krad(Si)) and in any case annealed after storage. The largest (and clearest) results were for the ADC CLOCK_XRD clock high threshold and the ADC SYNC_XRD clock low threshold and these are given in figures 5.4-1 and 5.4-2. The shifts before annealing were 15 and 10 mV/krad(Si) respectively. The ADC CLOCK high and low thresholds showed smaller and more erratic changes (probably affected by measurement errors). The ADC CLOCK_XRD clock low threshold and the ADC SYNC_XRD clock high threshold showed even smaller (and essentially negligible) changes with radiation.

The effects on the gate oxides can therefore be considered to be insignificant.

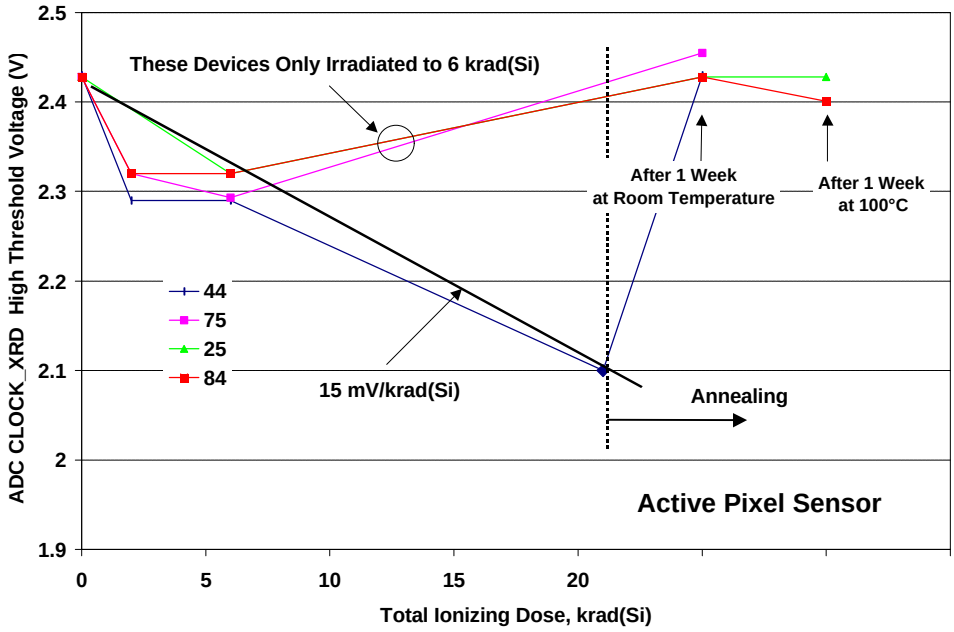

Figure 5.4-1 ADC CLOCK_XRD clock high threshold shifts

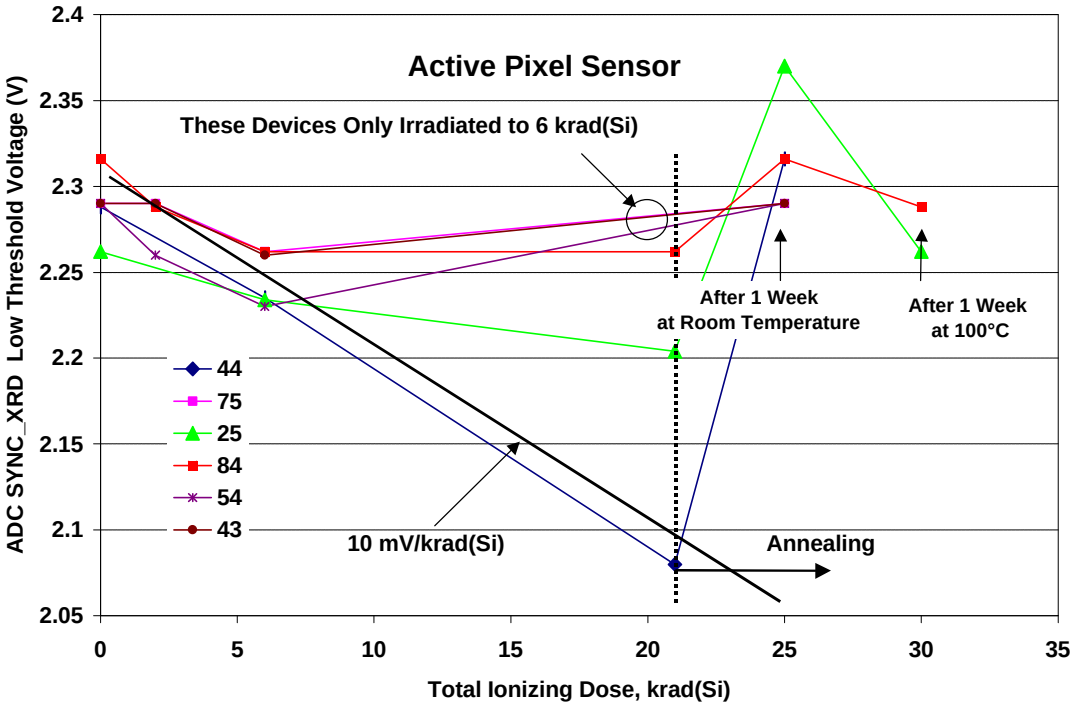

Figure 5.4-1 ADC SYNC_XRD clock low threshold shifts

5.5 BRIGHT FIELD MEASUREMENTS

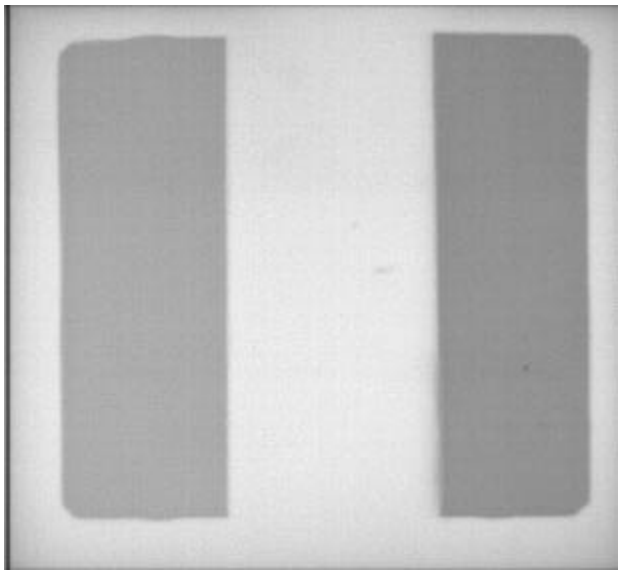

Figure 5.5-1 Bright field image from a proton damaged chip after 7.5 months storage unbiased at room temperature

Bright field measurements were made on both proton and cobalt60 irradiated devices. Quick-look measurements were made immediately after irradiation, after 7.5 months storage, unbiased at room temperature and after 14 months storage (under the same conditions). Figure 5.5-1 shows a bright field image from a proton irradiated chip (#62) after 7.5 months storage. The temperature and integration time were chosen such that the thermal dark signal was small compared with the photo-signal. It can be seen that the signal in the proton damage regions is *reduced*. Figure 5.5-2 shows the average response for the different dose regions on each proton damaged chip (normalised to 1 for the un-irradiated regions). The loss in response is large for the immediate and 7.5 month measurement but has annealed (and in fact turned into a small responsivity *gain* after 14 months). The initial loss can be modelled using an exponential relation with a 1/e fluence of 1.5 x 10^{10} p/cm^2. This loss could be due to either a reduction in quantum efficiency or a reduction in voltage gain. The former seems more likely since the alpha particle results, shown in figure 5.1-1, do not show any reduction in the peak pixel signal for the proton-irradiated regions (though, as mentioned in section 5.1, these results are not entirely conclusive since the peak signals were close to saturation).

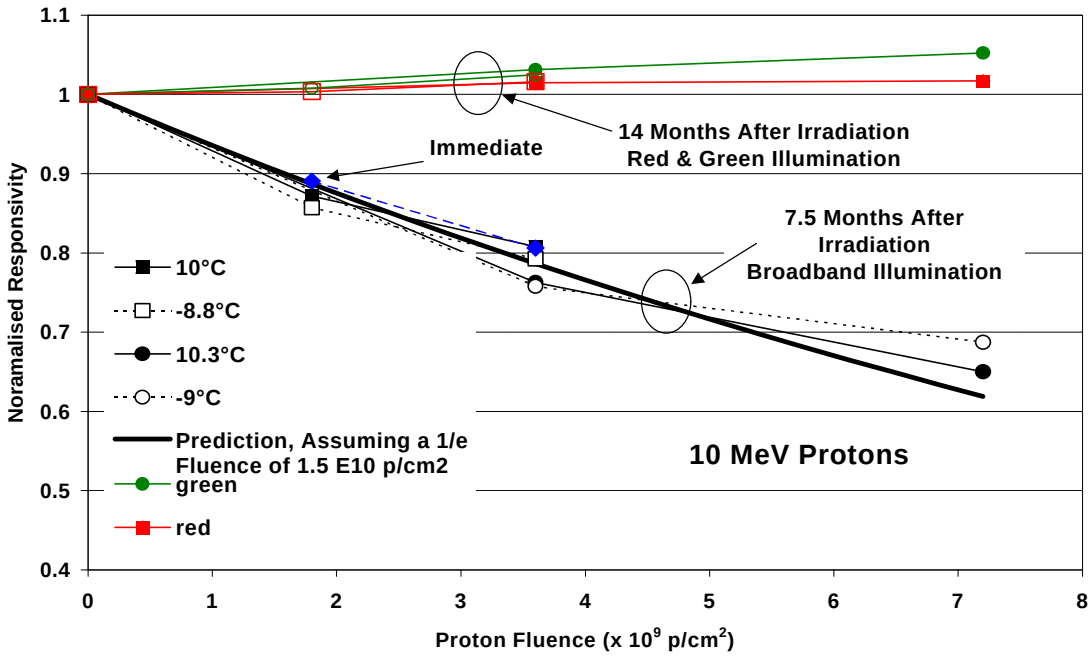

Figure 5.5-2 Average responsivity for proton irradiated devices #s 62 and 63

Results for the cobalt60 irradiated chips did not show any clear trend for a reduction in responsivity. A special test was performed to test this. A flat field illumination was supplied from a Xe arc lamp with a fibre-optic attachment. The end of the fibre was positioned ~50 cm from the imager so as to give a fairly uniform illumination, insensitive to the positioning of the ASCoSS chip. In order to keep the lamp at constant brightness the test was performed within a duration of 1 hour by operating the chips at room temperature with a short integration time (this allowed rapid interchange of devices). Signals were measured with illumination and with the illumination blocked by a screen (to obtain a dark level). The differences between the two levels are given below:

Device	Total Ionizing Dose krad(Si)	Flat field signal (ADU)
#75, un-biased	6	133
#54, biased	6	121
#43, biased	6	120
#84, un-biased	21.2	125
#44, biased	21.2	152

The above results suggest that the proton-induced loss in response is not due to total dose effects, but to displacement damage. This could be causing a reduction in the free carrier lifetime and so a reduction in the diffusion length and hence in the effective volume of the pixel – note that with the present design of ASCoSS chip, most of the pixel volume is field-free and the majority of the charge is collected by diffusion.

The change in diffusion length (L) due to displacement damage is given by the relation:

$$1/L^2 - 1/L_0^2 = K\phi \qquad (5.5\text{-}1)$$

Where L_0 is the pre-irradiation diffusion length and ϕ the proton fluence.

A typical value for the damage constant, K, is 2×10^{-6} cm^{-2} for 10 MeV protons[7] . The measured 1/e fluence of 1.5×10^{10} p/cm^2 then suggests that L_0 is of the order of 100 μm and that the responsivity is significantly changed if the diffusion length is reduced. In addition, it would be expected that the loss in responsivity is wavelength dependent. Unfortunately the early measurements were with broad band radiation. Detailed narrow band measurements were not made until 14 months , by which time the damage had annealed: c.f. the data for red (650 nm) and green (550 nm) light shown in figure 5.5-2. At that time it was possible to record the optical spot profiles shown in figure 5.5-3 but, because the damage had annealed, these show no significant differences between the 0 krad and 4 krad profiles at either wavelength (nor in fact between the red and green profiles). However the pixel dimension is 25 μm (and 17 μm thick) and so significantly less than the 100 μm characteristic length derived from the measurements (note that if L_0 were ~ 50 μm then K would have to be 4 times larger and this does not fit with experimental damage constants).

[7] E. A. Burke, "Energy dependence of proton-induced displacement damage in silicon", IEEE Transactions on Nuclear Science, vol. 33(6), pp 1276-1281 (1986).

The other problem with the displacement damage mechanism is the 'sudden' annealing which took place between 7.5 and 14 months after irradiation. No annealing of displacement damage would be expected on this timescale.

An alternative is to assume that ionization damage is the mechanism, through changes in the field strength distribution (which can be expected to depend on conditions at the surface). On the other hand there were no significant changes due to cobalt60 irradiation (though this may be due to the very different dose rates for the proton and cobalt60 irradiations). However the annealing would be more consistent with an ionizing dose mechanism.

Just prior to the 14 month measurements on the proton irradiated devices (in December 1999/ January 2000), an experiment was performed on one of the spare devices (#35), that had been used for latch-up testing (and so had received very little radiation damage). This device was irradiated in the laboratory with alpha particles for 18 days, between 21 December 1999 and 7 January 2000. The irradiations were performed un-biased, in air (with the source only a few mm above the device). A thin sheet of plastic was used to shield the edges of the device and to leave a small square (~ 320 x 340 pixels) in the centre of the imaging area clear for irradiation. However, unlike the proton irradiation case, the damaged region does not have sharp edges because of the large range of incident angles.

The source was the same as used in the earlier output calibration (section 6.1). The 2.59 kBq Am241 Beta Planchet source (Amersham International, type VZ-1366) was mounted directly on top of the APS device. This produced 5.484 MeV alphas at a rate of 160/cm^2/s at the APS as measured by counting events in the sensor itself. Since the source was thin, there was negligible loss in energy of the particles as they were emitted. Assuming an energy loss rate of 0.585 MeV cm^2/mg gives a ionizing dose rate of 0.13 krad/day. And a total accumulated dose of 2.3 krad (Si).

During the 18 day irradiation the APS experienced a fluence of 2.5 10^8 5.5 MeV alphas/cm^2. Using the results of Dale et al[8], 5.5 MeV alphas have a non-ionizing energy loss which is roughly 60 times higher than that for 10 MeV protons and the fluence of displacement damage equivalent 10 MeV protons was therefore about 1.5 10^{10} p/cm^2 or 8.3 krad of 10 MeV protons.

Figure 5.5-3 shows that the loss in signal immediately after irradiation was at most 10 %, a value which is substantially less than for the proton irradiation, but which is still significant. Since this experiment still does not differentiate between an ionization and a displacement damage mechanism, the results are inconclusive. Also the different magnitude of the response loss may again be due to differences in dose rate and annealing. On the other hand, it shows that the proton measurements are not a one-off case.

[8] C. J. Dale, P. W. Marshall, B. Cummings, L. Shamey and A. Delamere, "Spacecraft displacement Damage Dose calculations for Shielded CCDs", Proc SPIE, vol. 1656, pp 476-487, 1992

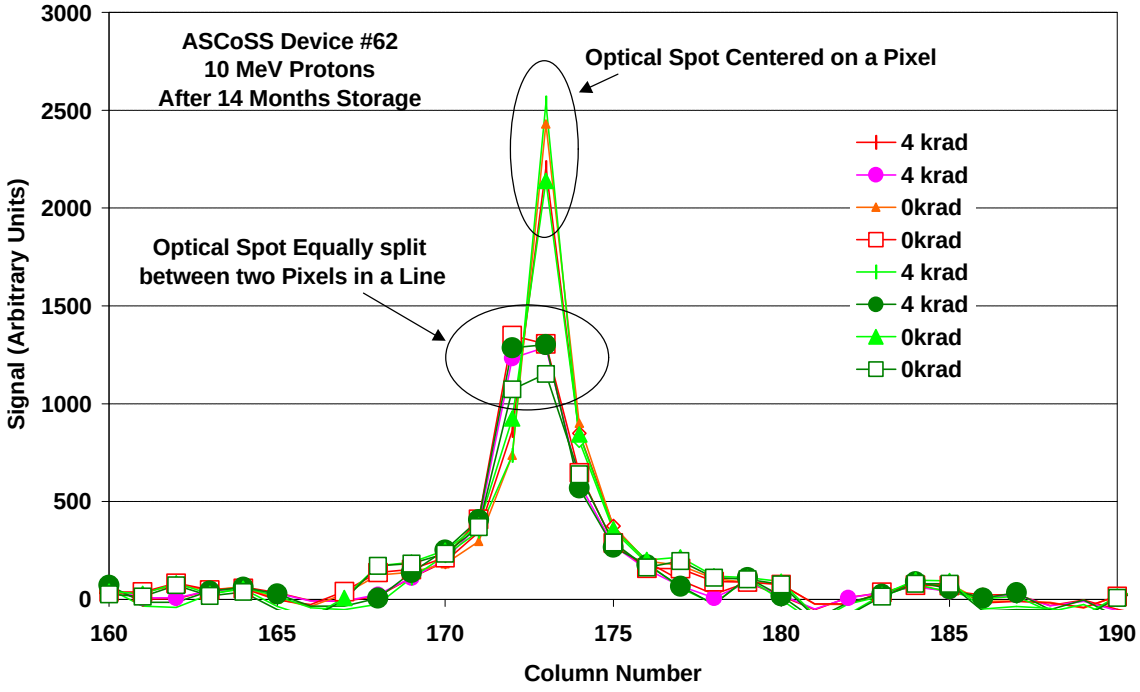

Figure 5.5-3 Optical spot profiles for proton-irradiated device #62 after annealing

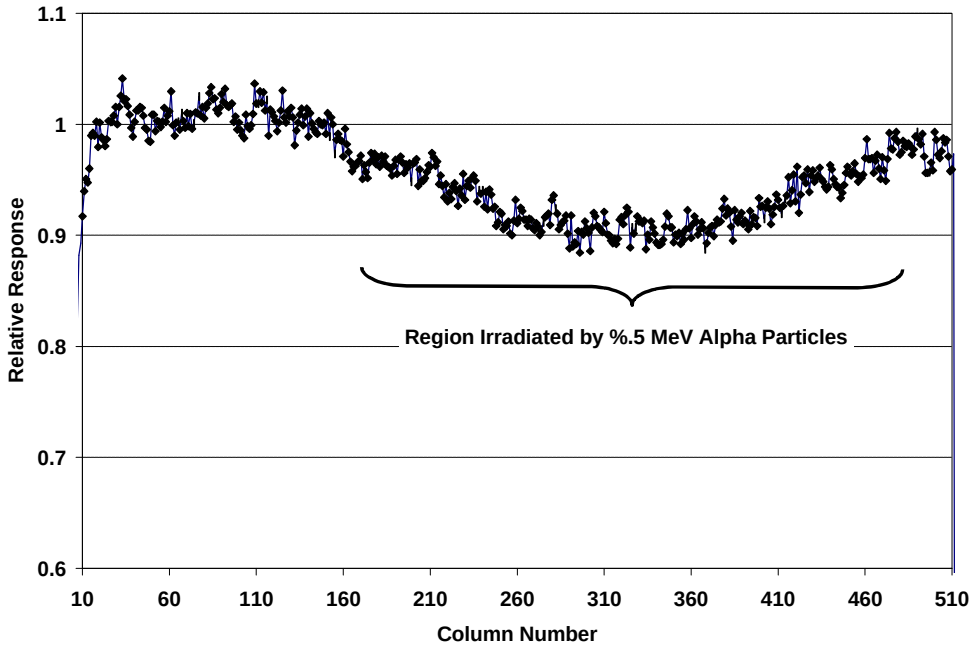

Figure 5.5-4 Relative signal immediately after alpha particle irradiation of device #35 for flat field illumination

In summary, neither a displacement damage nor ionization effects offer a definitive explanation at present, but the ionization mechanism seems the more plausible. Since the device design is being modified the exact explanation is not so important in this particular case. The important conclusion is that responsivity changes *can* be large for APS devices and responsivity (and spot profile) measurements should form a major part of future investigations.

It is also important to examine the photo-response non-uniformity (PRNU). Figures 5.5-5 to 5.3-8 show the PRNU before and after irradiation. The pre-irradiation measurements on devices 25 and 44 were made in both red and green light and the post-irradiation with a broadband tungsten lamp (which gives predominantly red light), however the figure shows that there is no significant wavelength dependence to the PRNU. There is also no significant change with radiation.

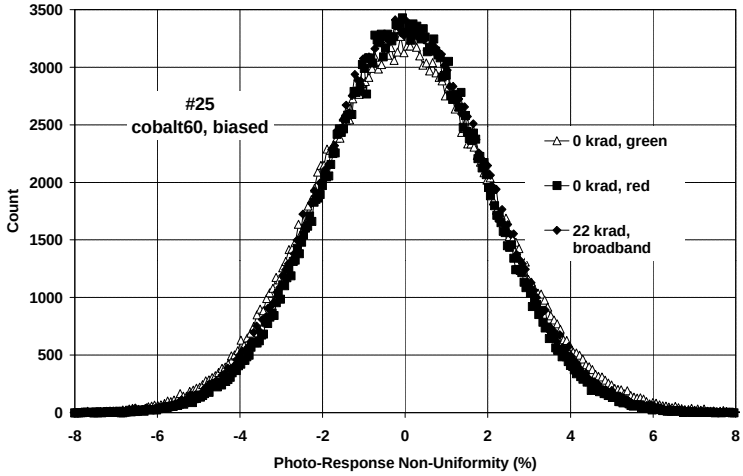

Figure 5.5-5 PRNU results for device #44 after 7.5 months (no annealing)

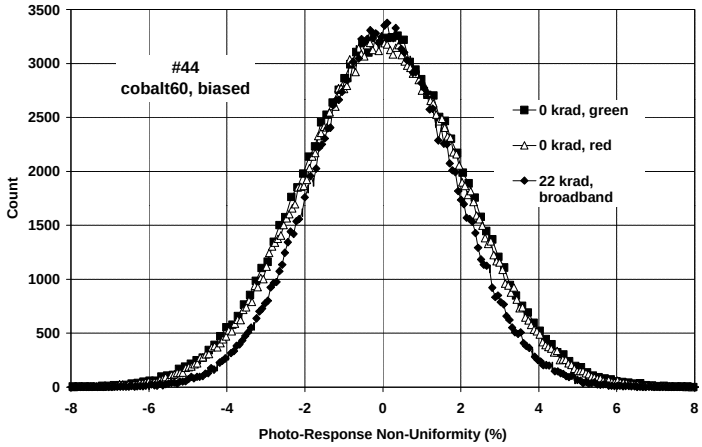

Figure 5.5-6 PRNU results for device #44

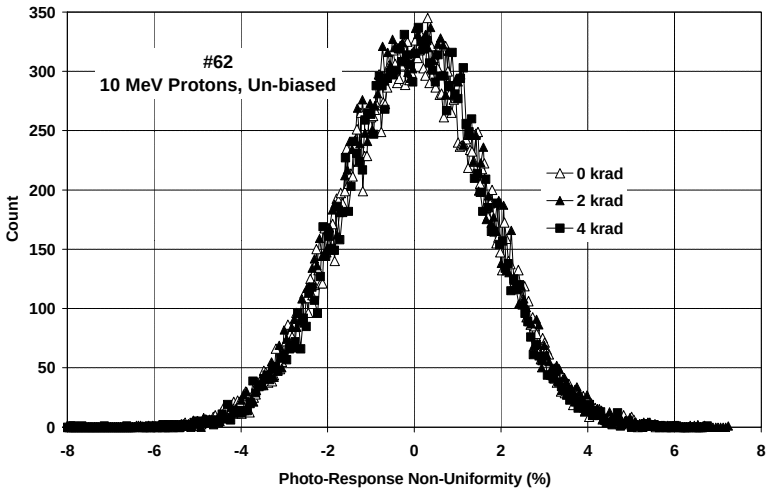

Figure 5.5-7 PRNU results for device #44

5.6 LINEARITY AND FULL WELL CAPACITY

Linearity and full well capacity were measured using a Xe arc source and variation of the exposure time (by changing the timing waveforms supplied to the chip). Figure 5.6-1 to 5.6-3 show typical results. The devices show a slight 'roll-off' in linearity at high signal levels, particularly for spot illumination, but there was no significant change with radiation, the full well capacity remaining at ~ 3200 ADU (14400 electrons). There is a suggestion that the full well capacity has increased in the two devices baked at 100°C9 numbers 25 and 84), but the effect is only weak.

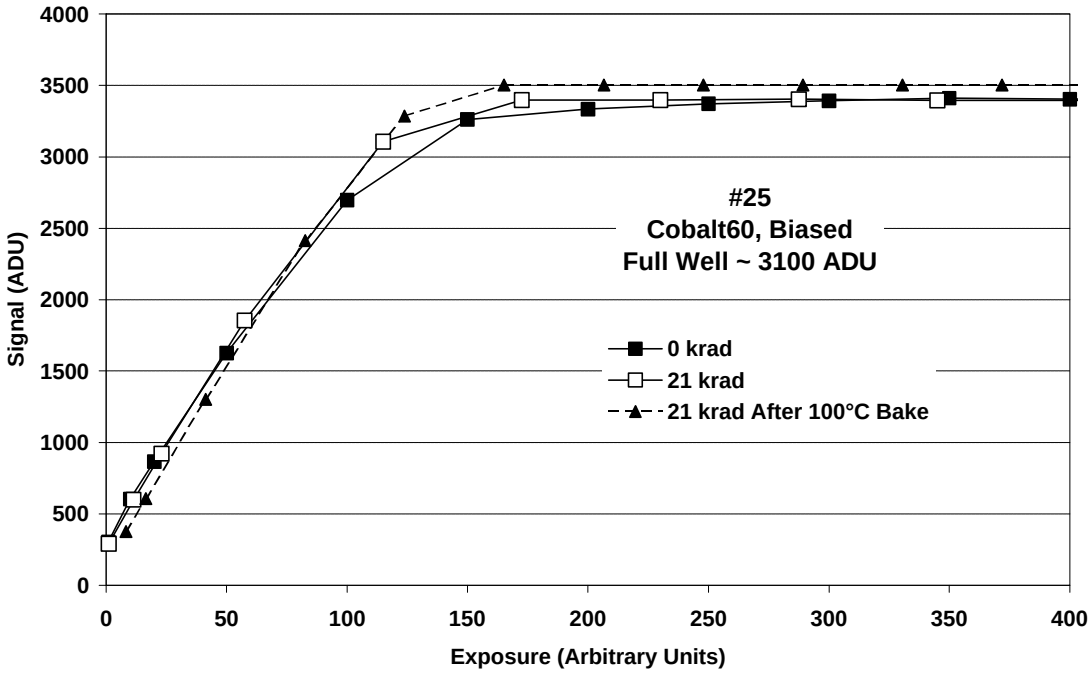

Figure 5.6-1 Linearity plots for device #25

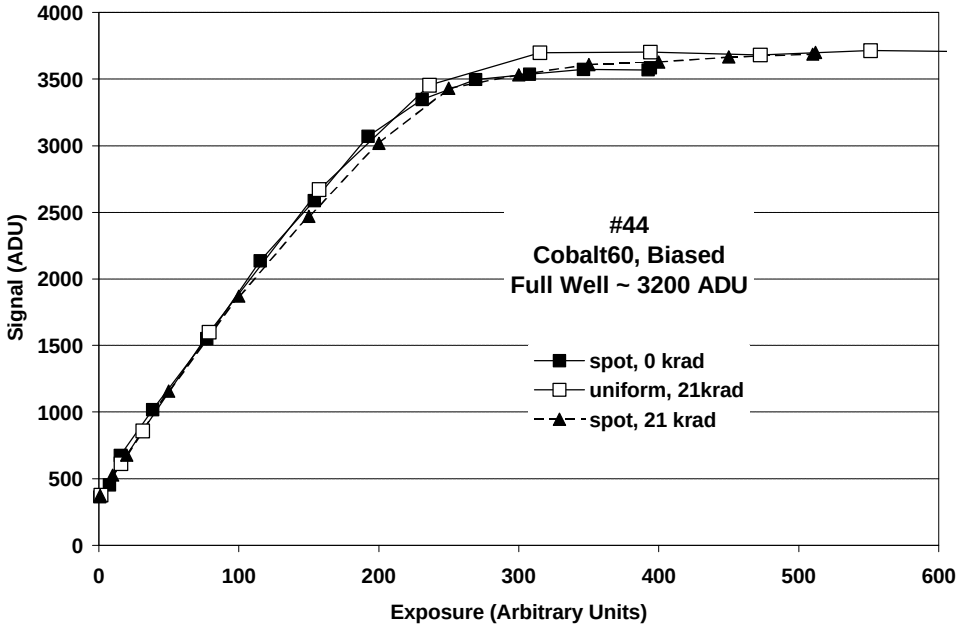

Figure 5.6-2 Linearity plots for device #44

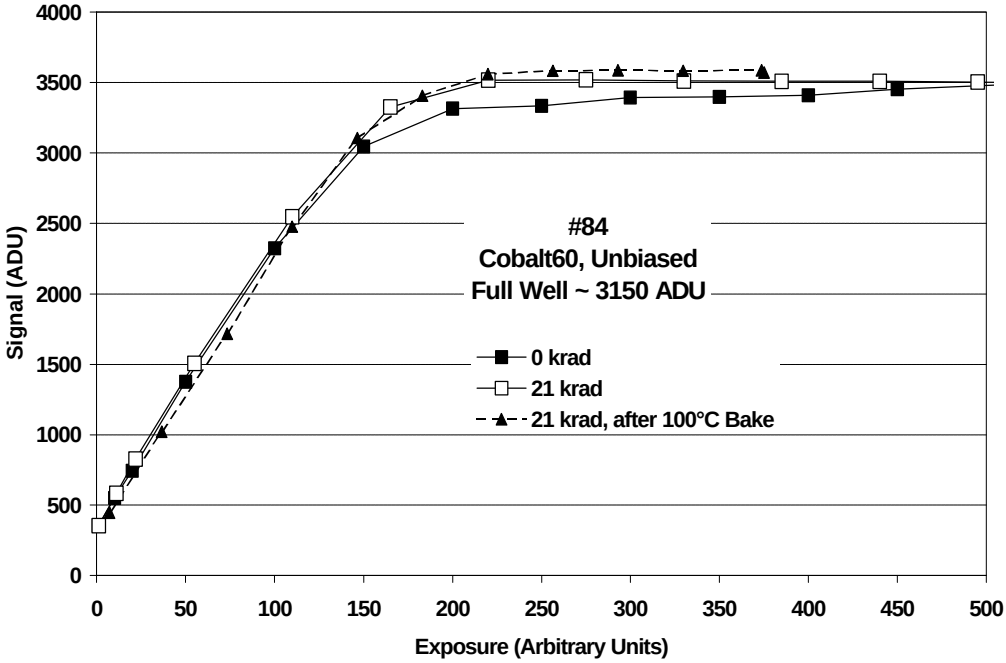

Figure 5.6-3 Linearity plots for device #84

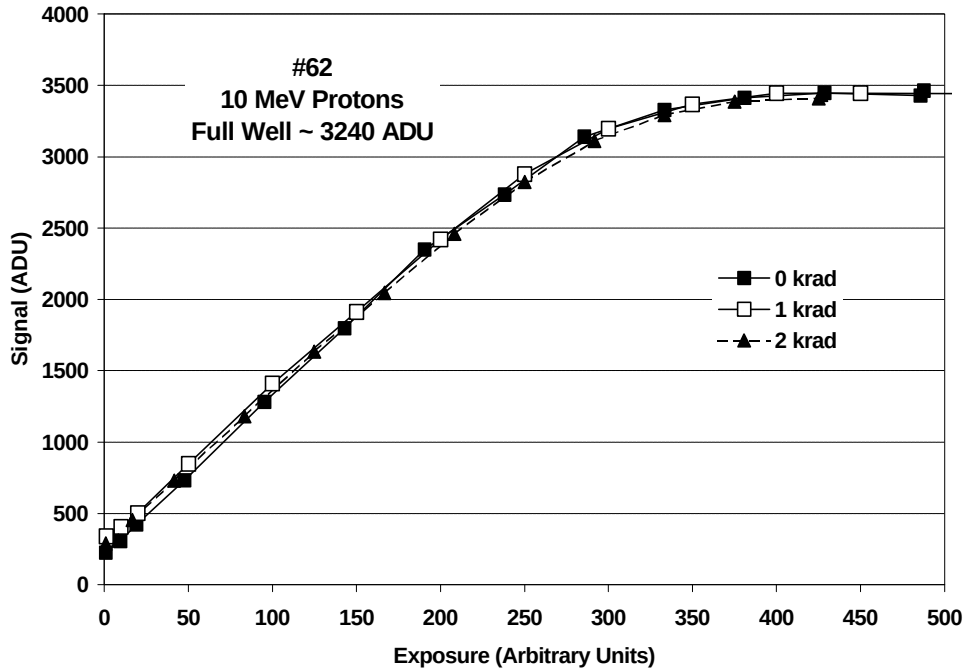

Figure 5.6-4 Linearity plots for device #63

5.7 PERFORMANCE OF THE ON-CHIP 8-BIT ADC

There was very little change in the functionality of the 8-bit ADC. Although the differential non-linearity (DNL) was poor to start with, with many missing codes (the ADC is essentially only 7-bit accuracy), the DNL did not change significantly. The measurements of integral non-linearity (INL) were limited by the linearity of the ramp voltage that was supplied from the test equipment, but again there was little change with radiation – except for a tendency for the offset to change. It would be prudent to allow for several LSB of offset drift in any flight application. Figures 5.7-1 to 5.7-6 show representative results.

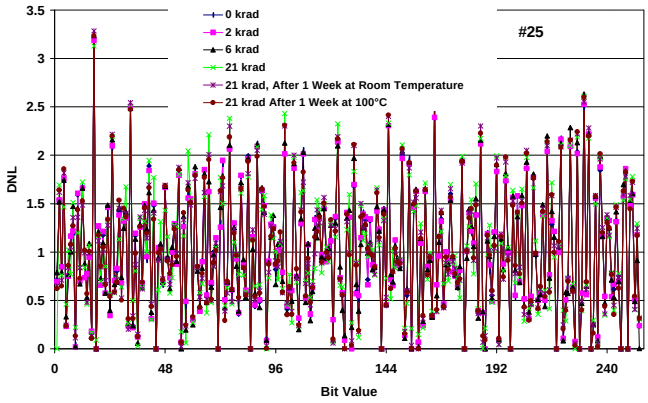

Figure 5.7-1 DNL for #25

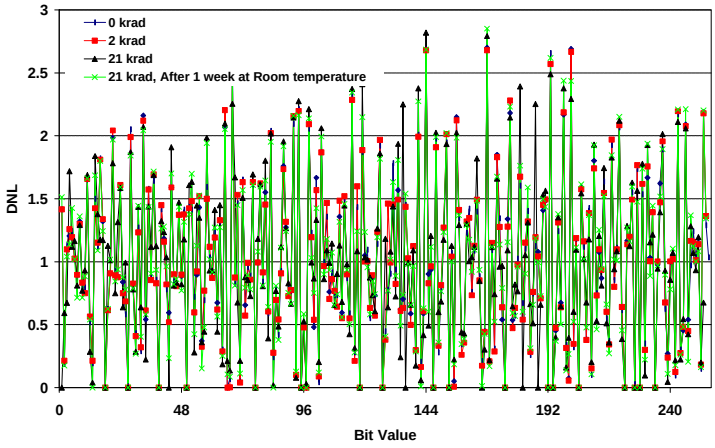

Figure 5.7-1 DNL for #44

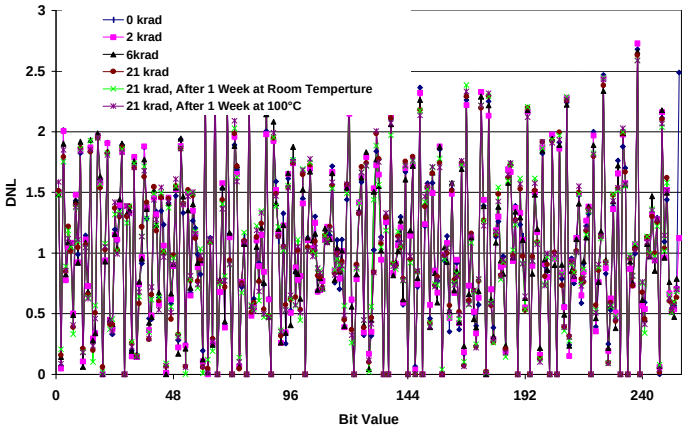

Figure 5.7-1 DNL for #84

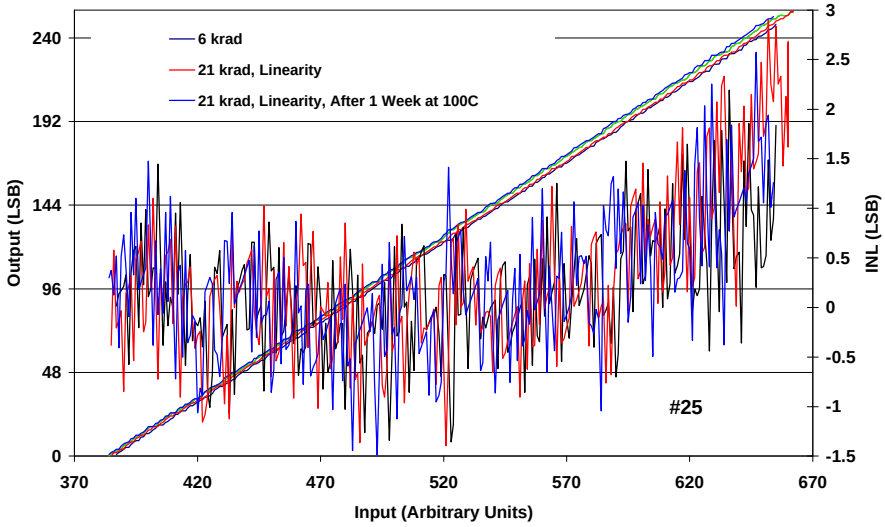

Figure 5.7-1 INL for #25

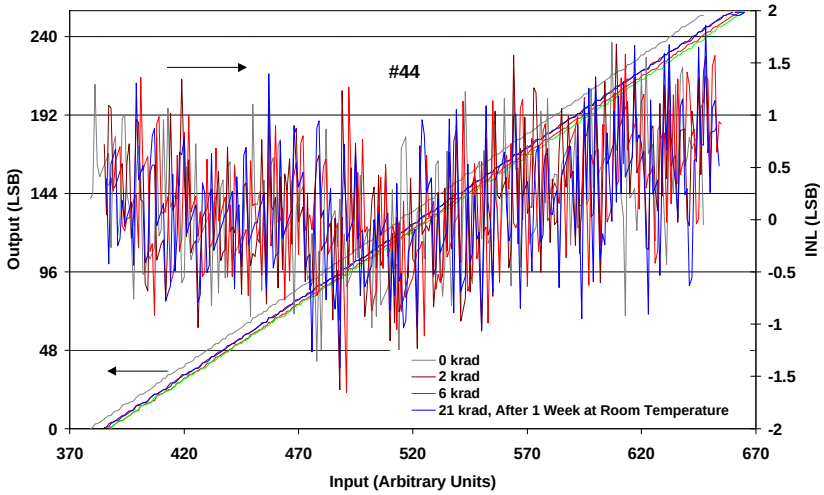

Figure 5.7-1 INL for #44

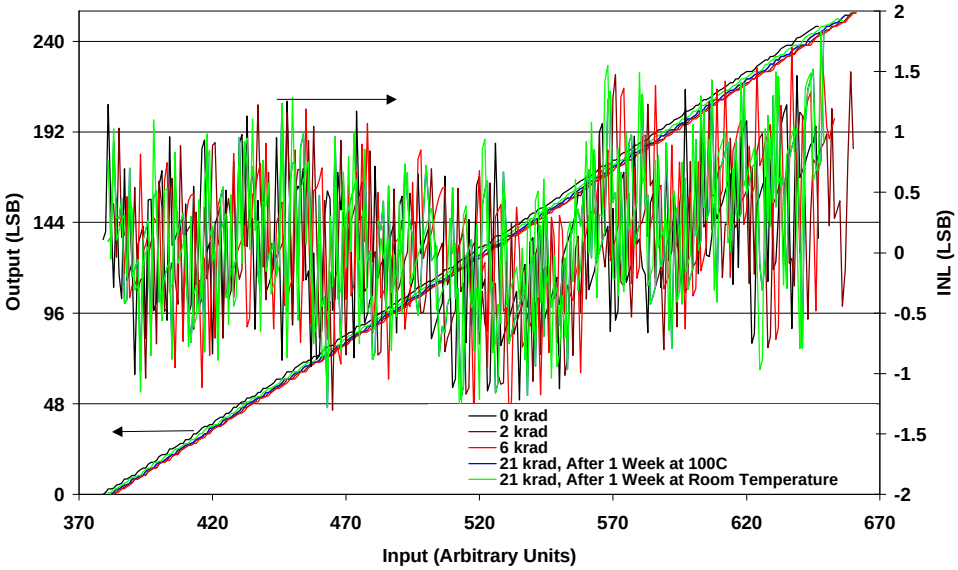

Figure 5.7-1 INL for #84

5.8 LATCH-UP TESTS

During heavy ion testing the sensor (Vdd3 and 4(and ADC (Vdd1 and 2) currents were monitored. When a latch up occurred the current limit on the supply board (60 mA) reduced the supply voltage. The results were as follows:

1) Sensor supplies

$^{40}Ar^{8+}$ ions, (energy 150 MeV), 60° incidence **LET 28.2 MeV/mg/cm^2**

No latch-up was seen at a maximum fluence of 2 10^6 ions/cm^2
No latch-up was seen at lower LETs

2) ADC supplies (VDD_AN_ADC, VDD_DIG_ADC and mpx, mux ADC output)

$^{40}Ar^{8+}$ ions, (energy 150 MeV), normal incidence ***LET 14.1 MeV/mg/cm^2***
No latch-up was seen at a maximum fluence of 5 10^6 ions/cm^2 (data from both devices)

$^{40}Ar^{8+}$ ions, (energy 150 MeV), 45° incidence ***LET 19.9 MeV/mg/cm^2***
device #5
run 3 Latch after 9.0 10^5 ions/cm^2 voltage fell to 2.6 V
run 4 Latch after 1.4 10^6 ions/cm^2 voltage fell to 2.6 V
average fluence for 1 latch = 1.25 10^6 ions/cm^2
device #4
run 3 4 Latch-up events during 2.0 10^6 ions/cm^2 voltage fell to 2.6 V
average fluence for 1 latch = 5.0 10^5 ions/cm^2

average cross section at LET 19.9 MeV/mg/cm^2 ~ 1.4 10^{-6} cm^2

$^{40}Ar^{8+}$ ions, (energy 150 MeV), 60° incidence ***LET 28.2 MeV/mg/cm^2***
device #5
run 1 latch after 5.6 10^5 ions/cm^2 voltage fell to 2.1 V
run 2 latch after 4.9 10^5 ions/cm^2 voltage fell to 2.6 V
average fluence for 1 latch = 5.25 10^5 ions/cm^2
device #4
run 4 5 Latch-up events during 2.0 10^6 ions/cm^2 voltage fell to 2.6 V
average fluence for 1 latch = 4.0 10^5 ions/cm^2

average cross section at LET 28.2 MeV/mg/cm^2 ~ 2.2 10^{-6} cm^2

Hence it is concluded that the 8-bit on-chip ADC has

latch-up threshold *~ 19.9 MeV/mg/cm^2*
saturation cross section *> 2.2 10^{-6} cm^2*

and the latch-up threshold for the rest of the sensor is *> LET 28.2 MeV/mg/cm^2*.

6. ADC RESULTS

6.1 POWER SUPPLY CURRENTS

Figure 6.1-1 shows the supply currents for all the ADCs monitored (i.e. those that were biased) during, and after, irradiation and figures 6.2-2 to 6.1-5 show measurements made with the characterisation board, which can separately measure the analogue and digital supplies for the ADCs. It can be seen that AD9223 devices #4 and #8 show large increases in current above ~10 krad but that this anneals out after a 100°C bake. This increase in current coincided with a significant degradation in the differential non-linearity for these two devices. In effect they both failed after the 19 krad irradiation because of 'stuck bits' – see also the DC level and DNL results. The bits which were stuck were some of the most significant and so output data was significantly corrupted. However, the recovery of the supply current after the bake also coincided with a return to normal DNL performance. Note that the devices #4 and 8 also showed larger than average changes in the VREF voltage.

There was little change in the LTC1415 currents, however it will be seen later that the DNL for the unbiased devices (#1 and #2) was degraded after the 100°C bake, possibly due to 'rebound' effects – but the degradation was not as severe as for the AD9223 devices (only the least significant bits were affected). Note that devices #1 and #2 also showed the largest decrease in digital supply current. Data sheet values are: 20 mA (typ. analogue) 26 mA (max analogue) and 0.02 mA (typ. digital), 0.5 mA (max. digital) for the AD9223 and 11 mA (typ. total), 20 mA (max, total) for the LTC1515. So for the failed AD9223s the currents go out of specification. The low power modes for the LTC1415 ('sleep' and 'nap') remained functional for all the tests.

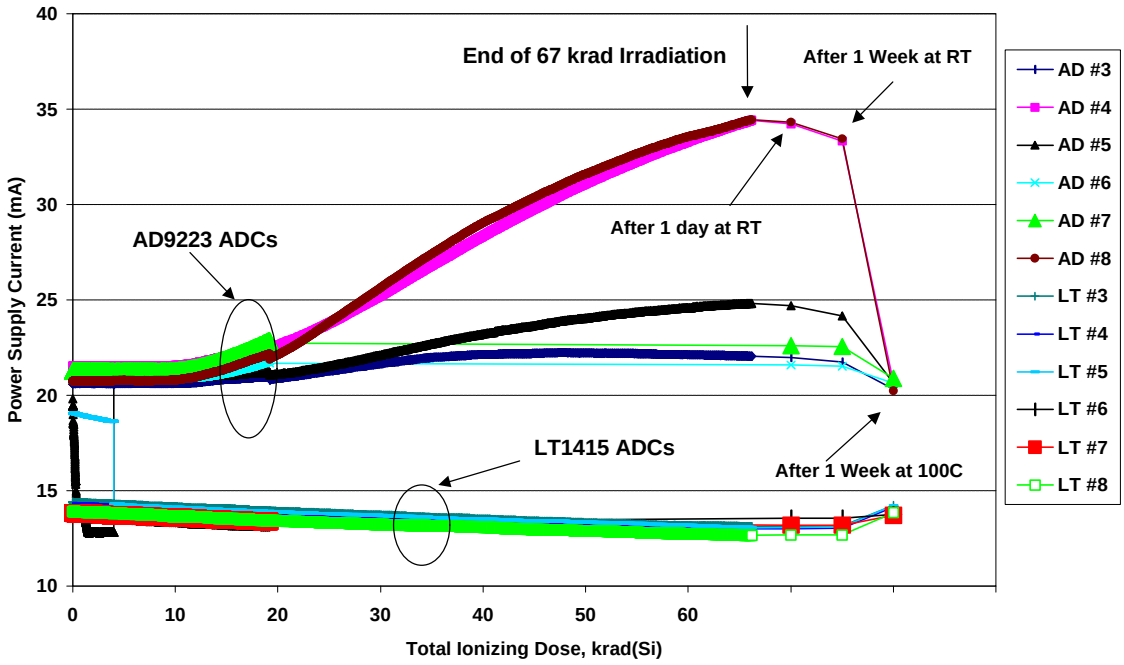

Figure 6.1-1 ADC power supply currents during and after irradiation. Devices #1 and #2 were not monitored during irradiation (they were not biased) and devices #6 and #7 were only given 19 krad total dose. Ad9223 devices #4 and #8 were failed after 19 krad.

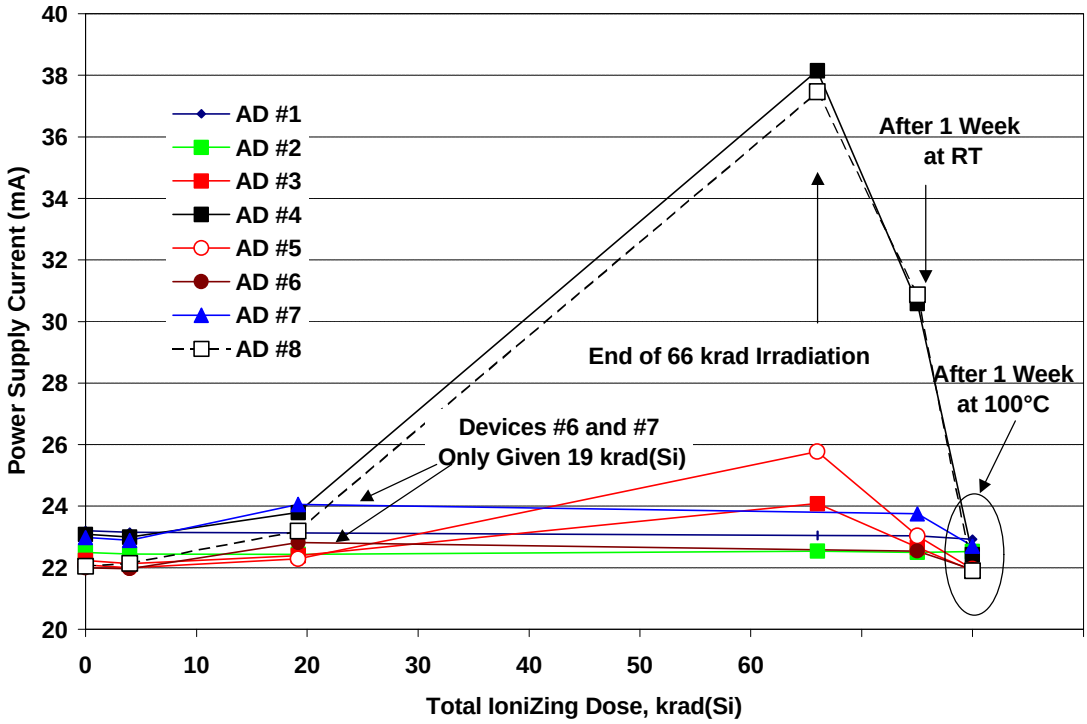

Figure 6.1-2 Analogue power supply current for the AD9223 ADCs monitored with the characterisation board

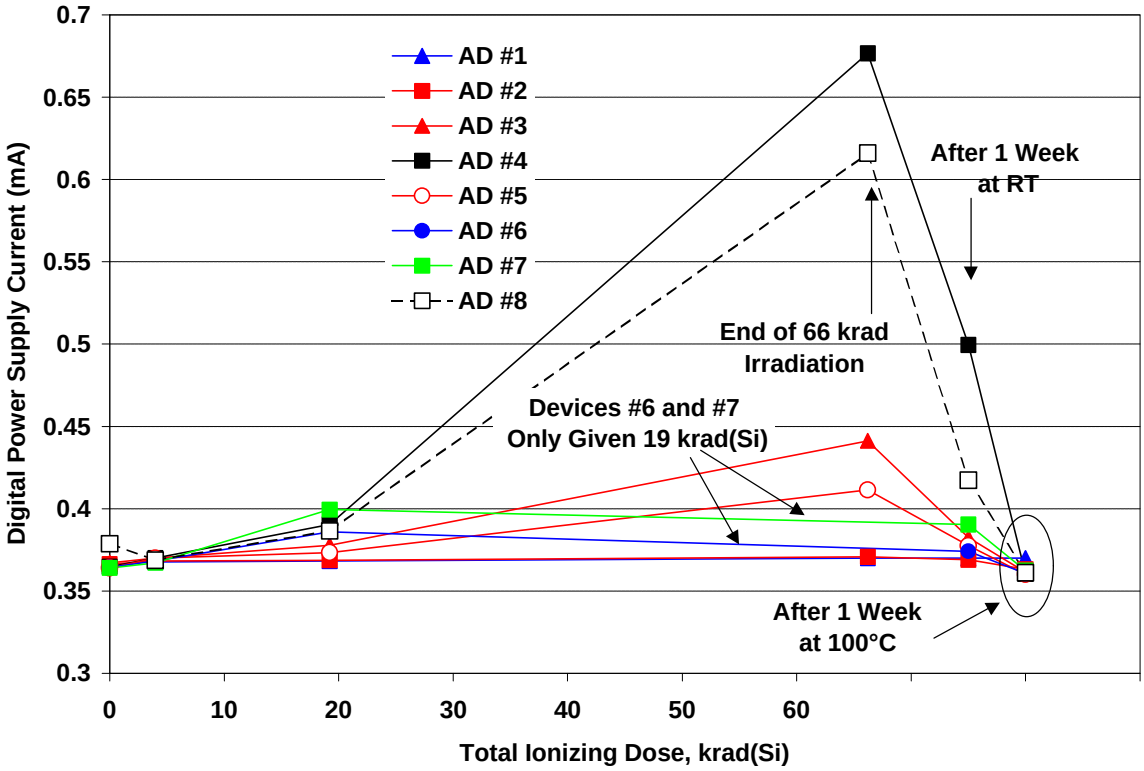

Figure 6.1-3 Digital power supply current for the AD9223 ADCs monitored with the characterisation board

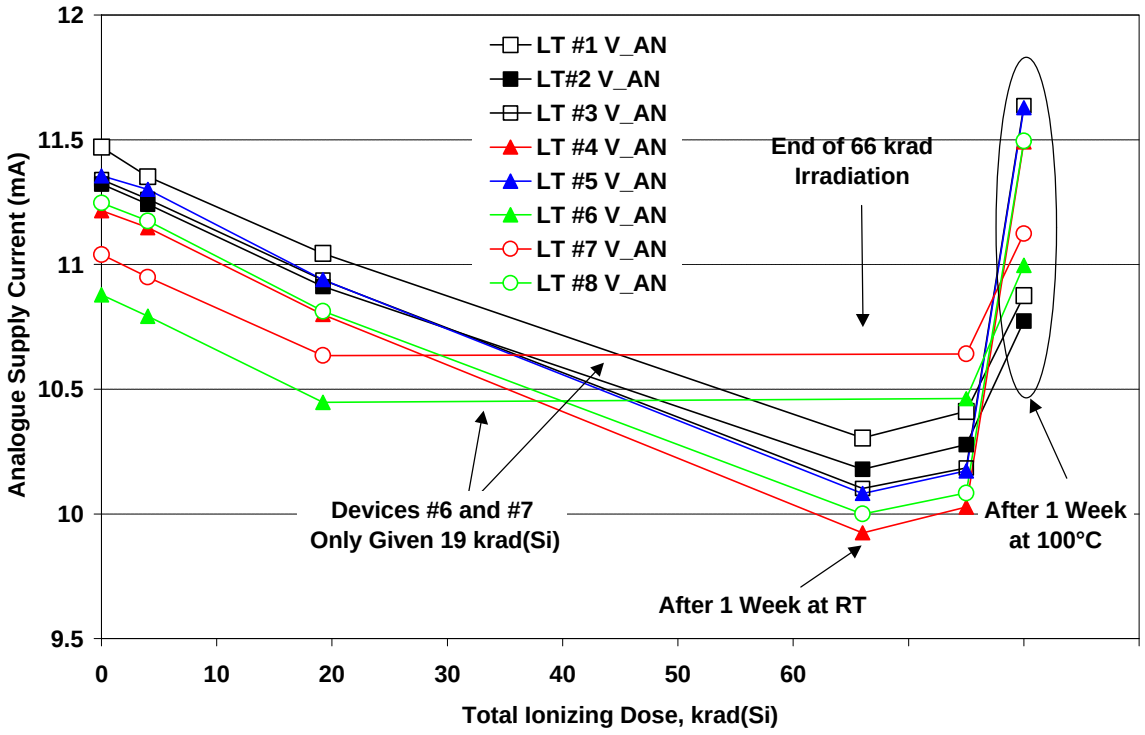

Figure 6.1-4 Analogue power supply current for the LTC1415 ADCs monitored with the characterisation board

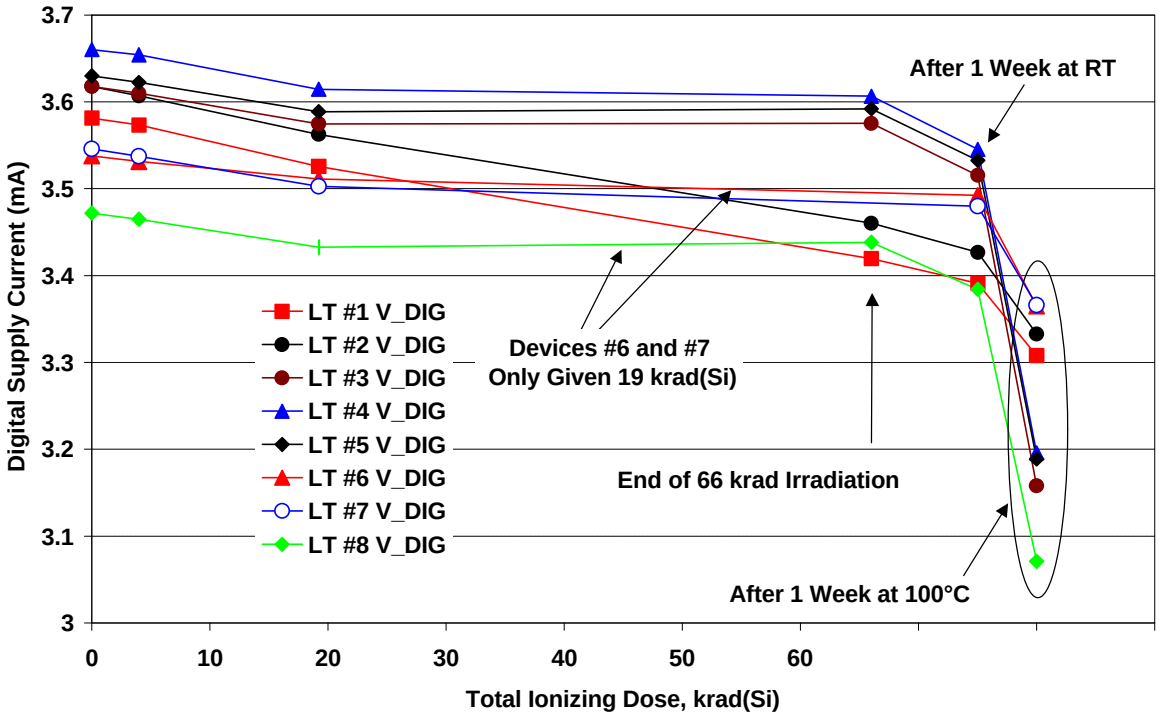

Figure 6.1-5 Digital power supply current for the LTC1415 ADCs monitored with the characterisation board

6.2 REFERENCE VOLTAGE

The value of the on-chip is critical for the offset and gain accuracy of an ADC. Values are shown in figures 6.2-1 and 6.2-2. The changes with radiation are small and within specification (2.5 ± 0.035 V for the AD9223 and 2.5 ± 0.020 V for the LTC1415) and it was not necessary to use an external voltage reference at any stage. As noted above the AD9223 devices which 'failed' immediately after iraddiation (but recovered) showed larger than average changes in VREF.

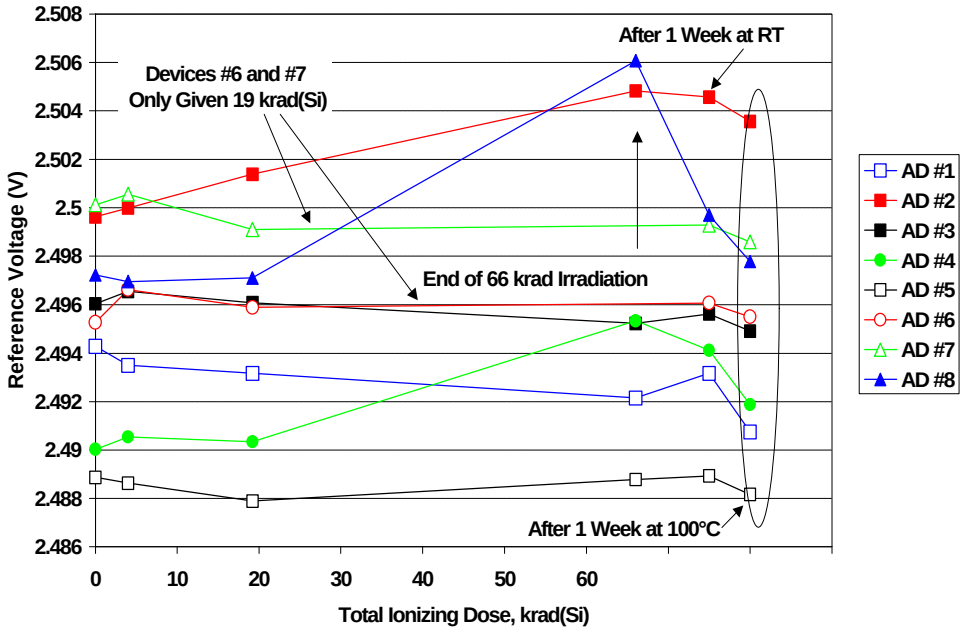

Figure 6.2-1 Evolution of the on-chip voltage reference for the AD9223

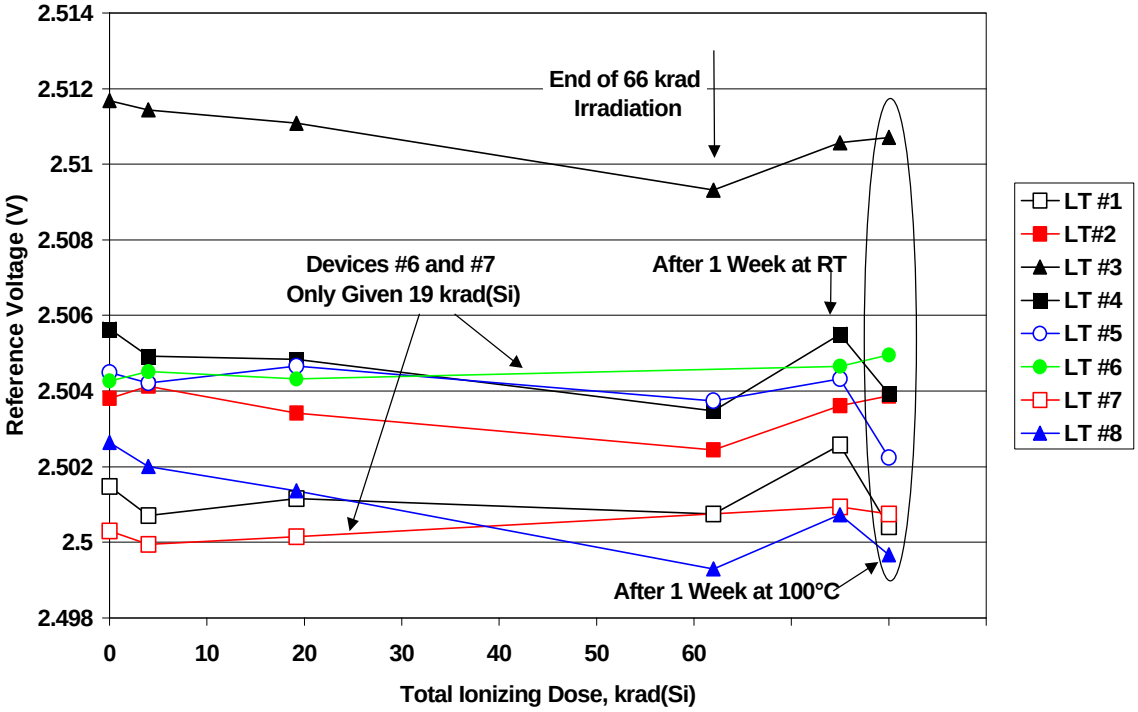

Figure 6.2-2 Evolution of the on-chip voltage reference for the LTC1415

6.3 DIFFERENTIAL NON-LINEARITY (DNL)

Apart from the 'stuck' bits observed with devices #4 and #8 immediately after 66 krad(Si), the Ad9223 devices showed no significant changes in DNL. Figures 6.3-2 and 6.3-3 show typical results, wheras Figure 6.3-1 shows data for the 'temporarly failed' #4.

All the LTC1415 devices behaved normally with no significant changes in DNL until after the 100 °C bake when devices #1 and #2 (both un-biased during irradiation) showed increases in DNL – though the DNL for the LTC1415 was in general higher than for AD9223 and the changes in DNL were not dramatic. Figures 6.3-4 to 6.3-6 show results for devices #1 and #2 and a more typical device (#5). Note that the DNL for the devices varied with operating conditions and was better at some times than at others, nevertheless it is felt that the changes for devices #1 and #2 are probably significant.

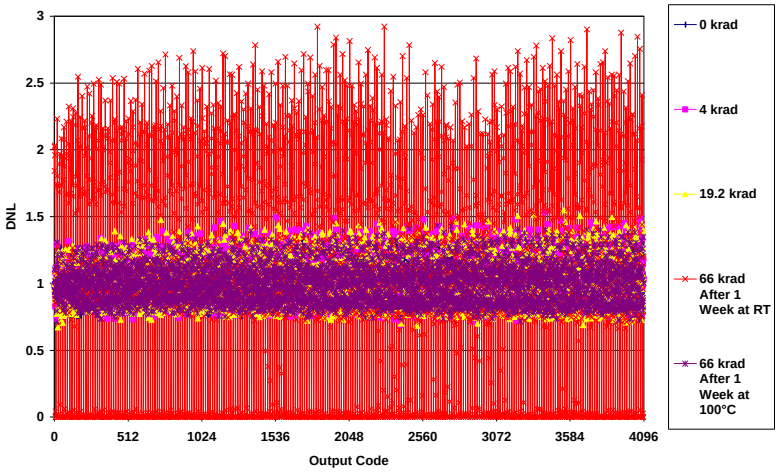

Figure 6.3-1 DNL for AD9223 device #4 showing large DNL after 66 krad

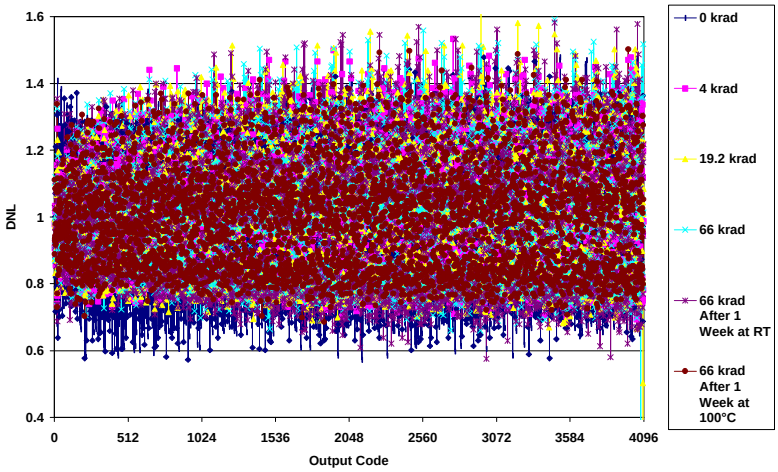

Figure 6.3-2 DNL for AD9223 device #2, un-biased during irradiation

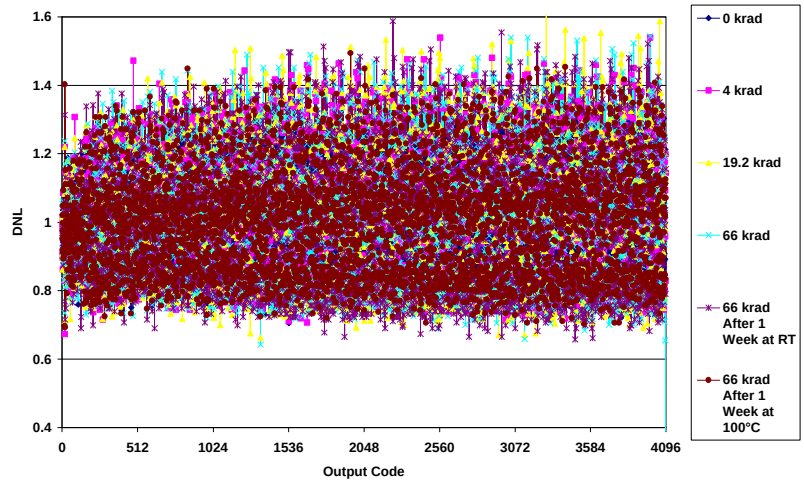

Figure 6.3-3 DNL for AD9223 device #3, un-biased during irradiation

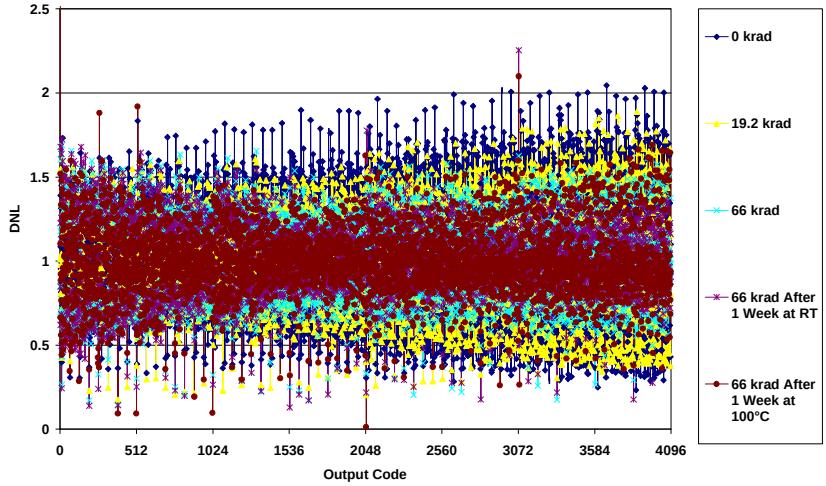

Figure 6.3-4 DNL for LTC1415 device #1, un-biased during irradiation

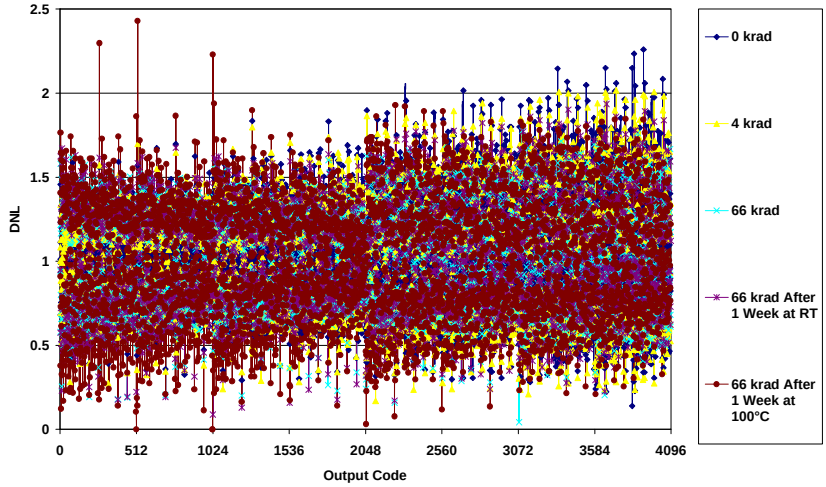

Figure 6.3-5 DNL for LTC1415 device #2, un-biased during irradiation

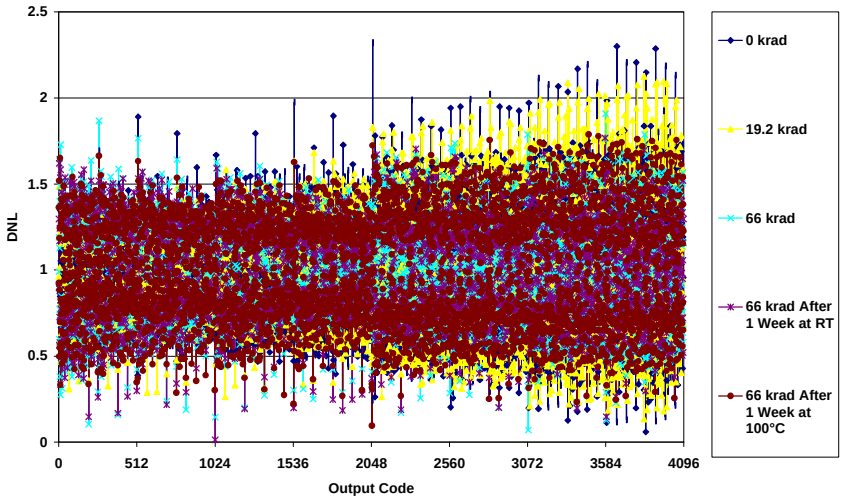

Figure 6.3-6 DNL for LTC1415 device #5, biased during irradiation

6.4 ADC GAIN, OFFSET AND INTEGRAL NON-LINEARITY (INL)

The ADC gain and offset are critical for the accurate measurement of signals. These parameters were checked by applying three stable input voltages, one near the bottom of the ADC range, one near mid-range and one near the top of the range (0.1336 V, 1.139 V and 3.328 V, respectively). Note that the full scale voltage is nominally 5.00 V for the AD9223 and 4.096 V for the LTC1415. The DC input voltages gave average ADC outputs as in the table below and the variation with cobalt60 irradiation is shown in figures 6.4-1 to 6.4-4. With the AD9223 devices there are large changes for devices #4 and #8 due to the 'stuck' bits' problem mentioned above. The output levels returned to normal, however, after annealing. There were small changes (particularly for device #2) but these annealed out. For the LTC1415 devices the changes were small except after annealing, when devices #s 3, 4 and 8 (all biased) showed significant changes in offset. LTC1415 devices #9 and #10 were used as controls and were not irradiated – these showed very small shifts in output level. Note that it was the un-biased devices (#1 and #2) which showed the DNL degradation after the bake.

	Average AD9223 output (pre-irradiation)*	**Average LTC1415 output (pre-irradiation)***
Low DC Input Level	111.7 ADU	134.7 ADU
Medium DC Input Level	935.5 ADU	1140.2 ADU
High DC Input Level	2729.8 ADU	3332.6 ADU

- The starting values were within:

AD9223 ± 2, 3 and 7 LSB of the average value for the low, medium and high levels
LTC1415 ± 1, 3 and 8 LSB of the average value for the low, medium and high levels

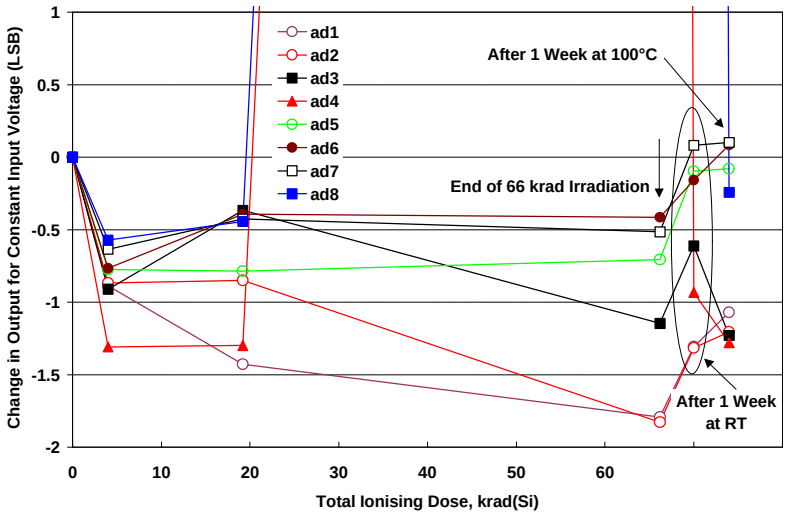

Figure 6.4-1 Variation of the AD9223 output (in ADU) compared with the pre-irradiation value, for the low level DC input

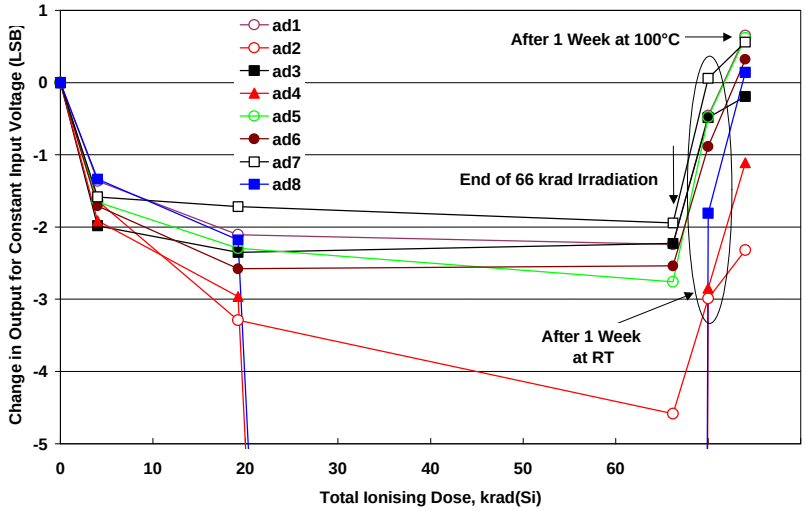

Figure 6.4-1 Variation of the AD9223 output (in ADU) compared with the pre-irradiation value, for the medium level DC input

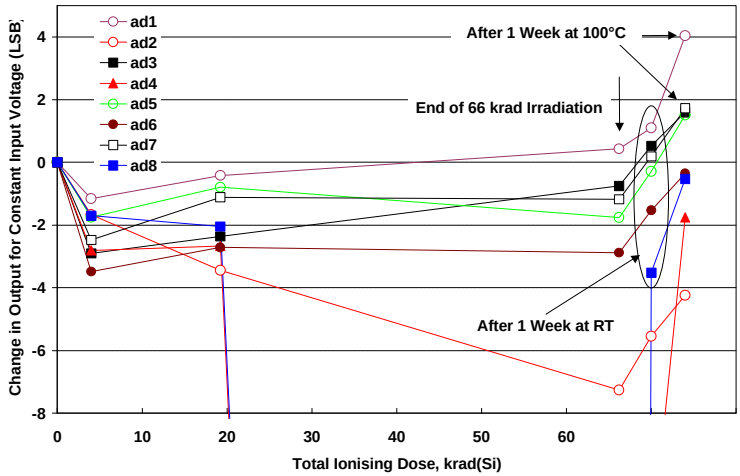

Figure 6.4-1 Variation of the AD9223 output (in ADU) compared with the pre-irradiation value, for the high level DC input

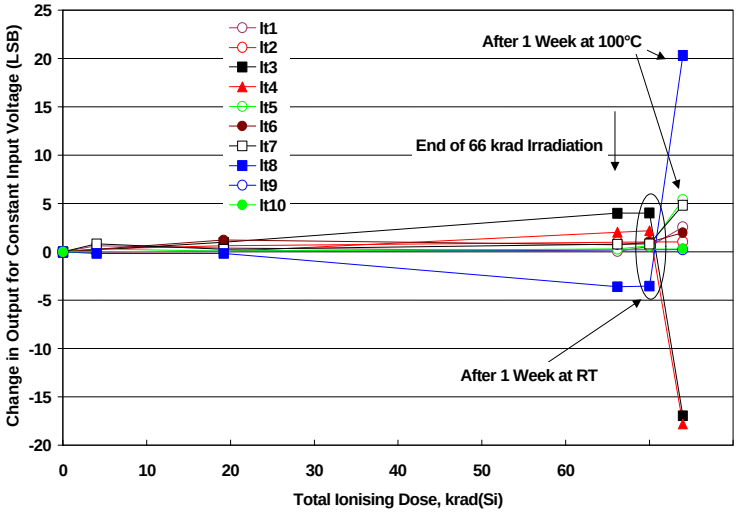

Figure 6.4-1 Variation of the LTC1415 output (in ADU) compared with the pre-irradiation value, for the low level DC input

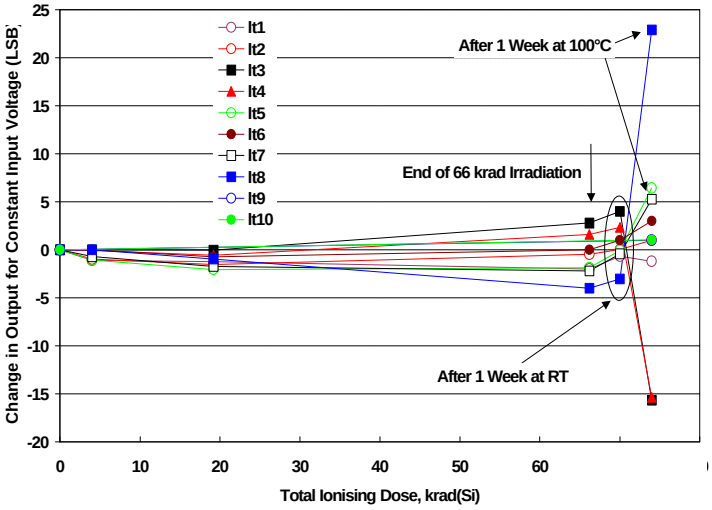

Figure 6.4-1 Variation of the LTC1415 output (in ADU) compared with the pre-irradiation value, for the medium level DC input

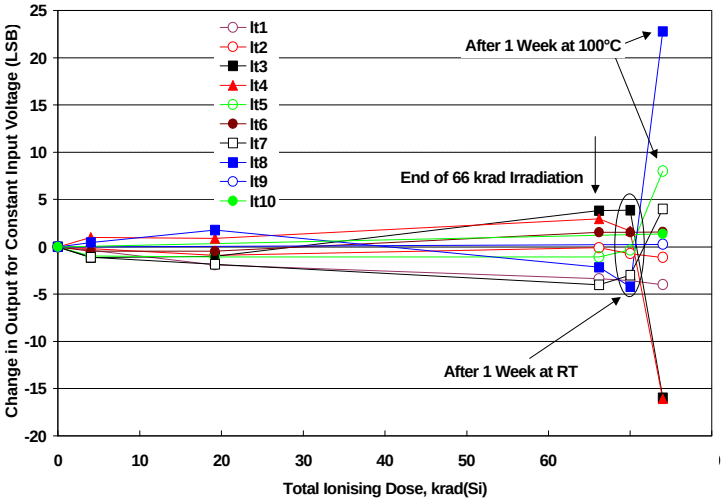

Figure 6.4-1 Variation of the LTC1415 output (in ADU) compared with the pre-irradiation value,for the high level DC input

6.5 ADC TIMING

The delay time between the ADC clock and the rising (or falling) edge of the data is an important parameter and is shown in figures 6.5-1 to 6.5-2. The ADCs remained inside the manufacturers allowed delay time but there is a rising trend and the delay time would probably be exceded at higher doses.

The LTC1415 has a BUSY clock which can be used to latch data into an instrument. In this case the data set up time (the 'data ready before BUSY') is an important parameter. It should be greater than 20 ns for correct operation, and this is easily satisfied by the devices as shown in figure 6.5-3.

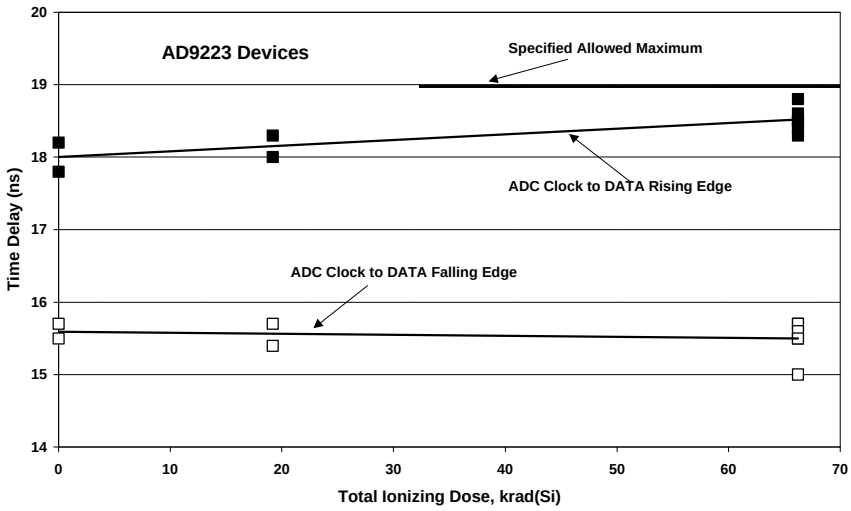

Figure 6.5-1 Delay time between ADC clock and data rising/falling edges for AD9223 devices

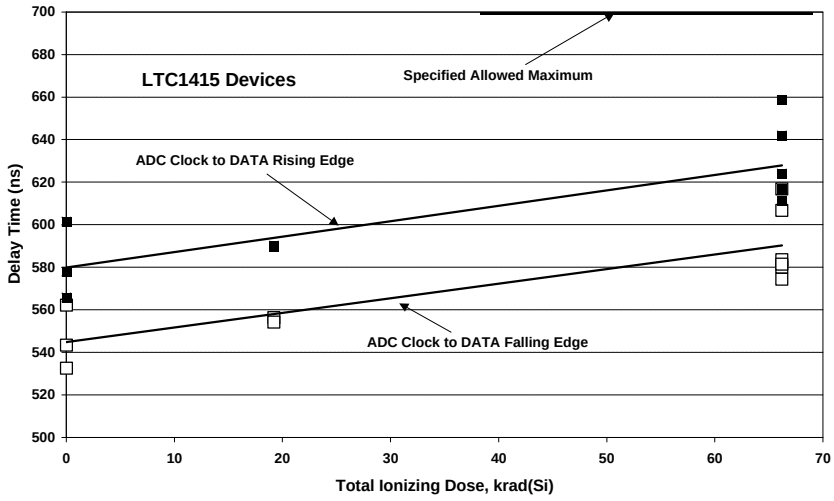

Figure 6.5-2 Delay time between ADC clock and data rising/falling edges for LTC1415 devices

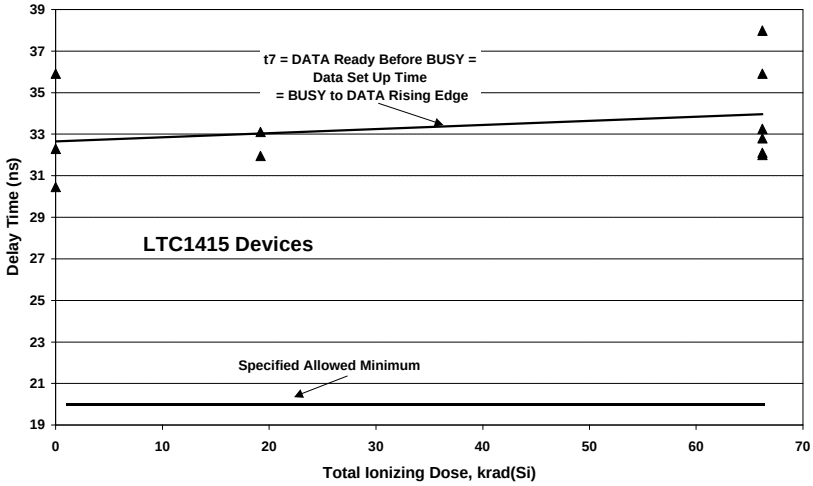

Figure 6.5-3 Data ready before BUSY time for LTC1415 devices

6.6 ADC THRESHOLD VOLTAGES

The threshold voltages for operation of the ADC clock (both device types) and ADC READ (for the LTC1415 only) were measured. Data is presented in figures 6.6-1 to 6.6-5. On each plot a line is drawn by eye as a guide to estimating the shift before annealing. The AD9223 showed shifts of 2-3 mV/krad(Si) with some (~30%), but not complete annealing. The LTC1415 showed a higher shift (~ 5 mV/krad(Si)) but with almost complete annealing for the biased devices (biased during irradiation *and* annealing) and ~ 50% annealing for the un-biased devices (un-biased during irradiation *and* annealing). These shifts are insignificant from an operational point of view and are consistent with a thin gate oxide.

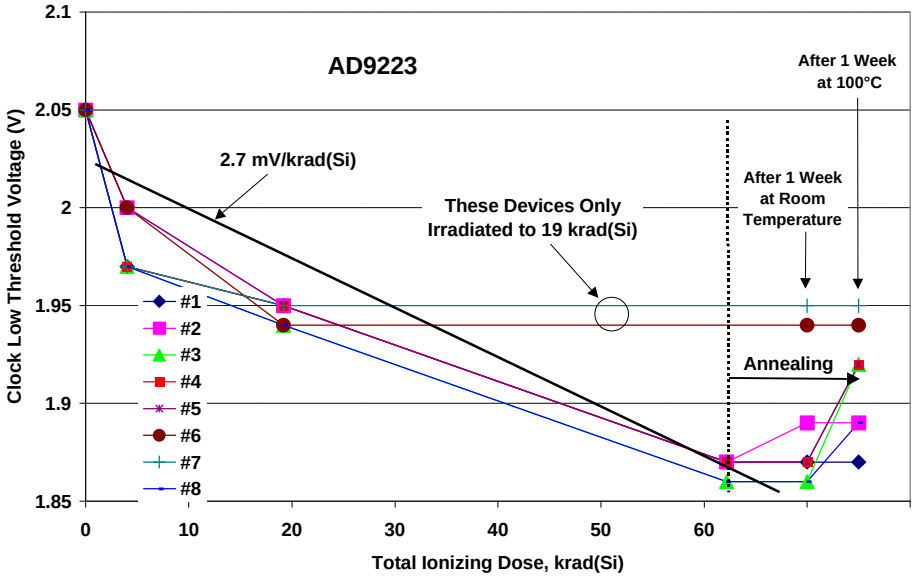

Figure 6.6-1 Threshold shifts for the AD9223 clock voltage

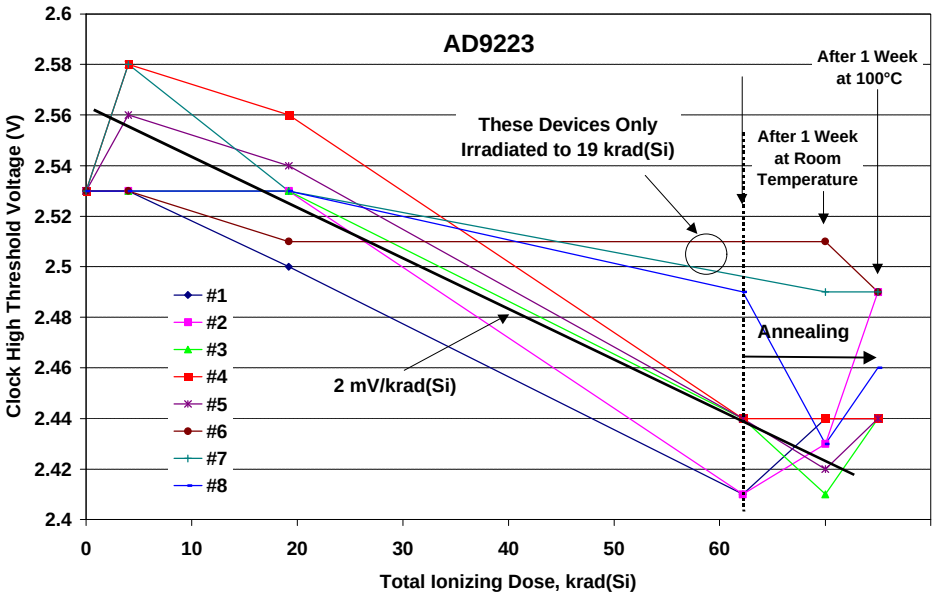

Figure 6.6-2 Threshold shifts for the AD9223 clock voltage

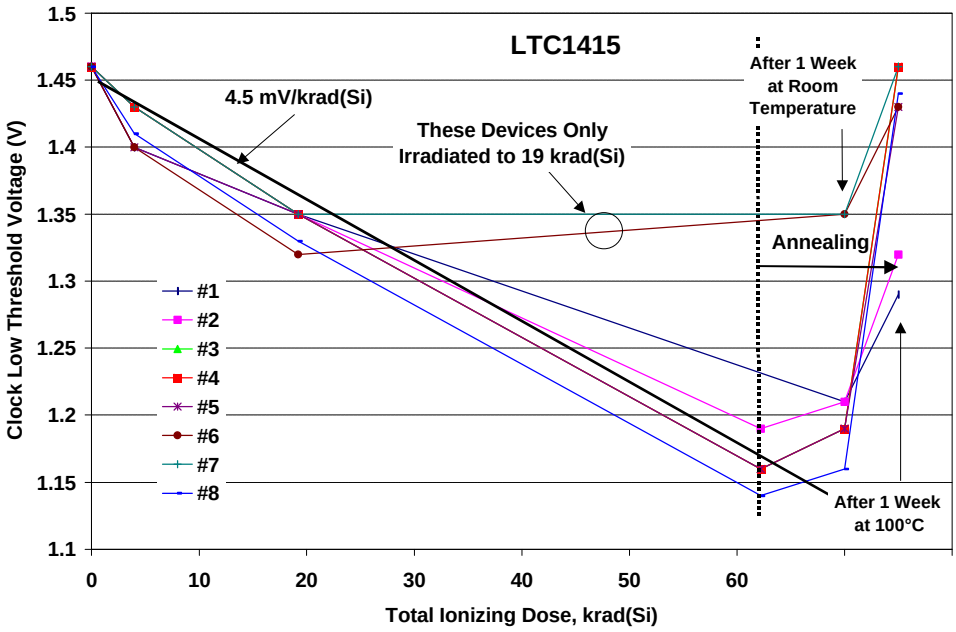

Figure 6.6-3 Threshold shifts for the LTC1415 clock voltage

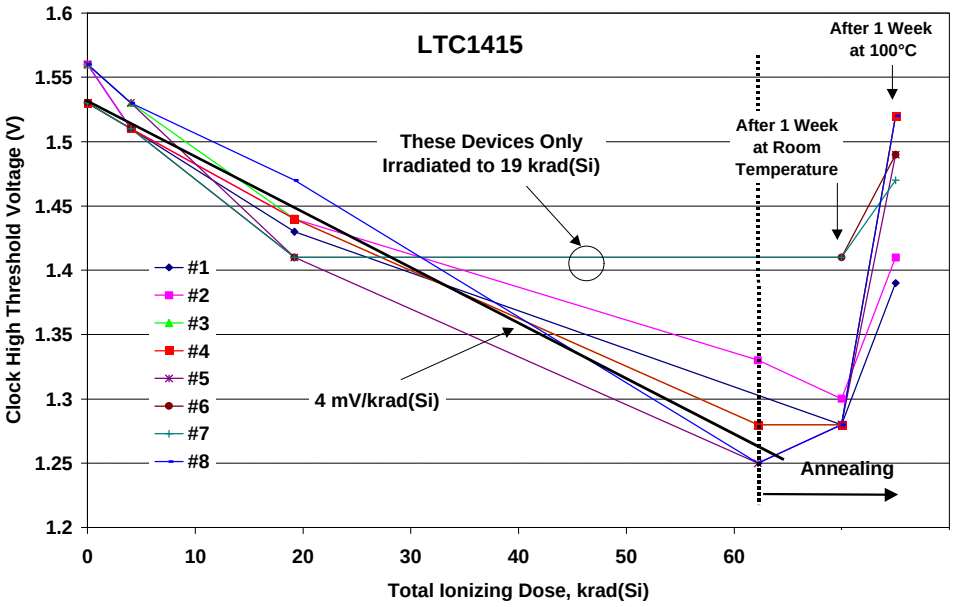

Figure 6.6-4 Threshold shifts for the LTC1415 clock voltage

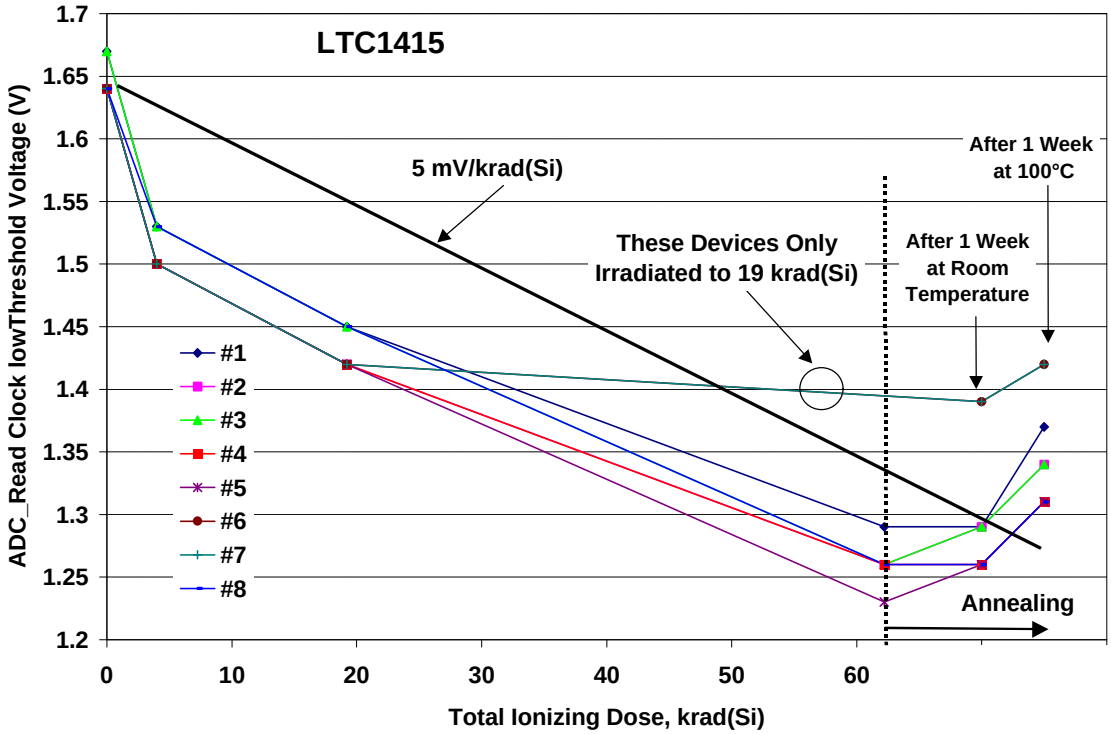

Figure 6.6-5 Threshold shifts for the LTC1415 clock voltage

6.7 LATCH-UP MEASUREMENTS

6.7.1 AD9223

Three de-lidded devices were tested, one from the current CHRIS flight batch A63155.1, date code 9702 (device #2) and two (devices # 1 and 3) from another batch (AG3710.1, date code 9644). The results were as follows:

$^{40}Ar^{8+}$ ions, (energy 150 MeV), normal incidence **LET 14.1 MeV/mg/cm^2**

device #1

run 1	latch after 2.0 10^6 ions/cm^2	voltage fell to 2.84 V
run 2	latch after 2.6 10^6 ions/cm^2	voltage fell to 3.49 V
run 3	latch after 1.6 10^6 ions/cm^2	voltage fell to 2.66 V
run 4	latch after 2.7 10^6 ions/cm^2	voltage fell to 3.44 V

average cross section = 4.5 10^{-7} cm^2

device #2

run 1	latch after 7.0 10^5 ions/cm^2	voltage fell to 2.97 V
run 2	latch after 5.7 10^5 ions/cm^2	voltage fell to 3.68 V
run 3	latch after 1.25 10^5 ions/cm^2	voltage fell to 2.82 V

average cross section = 2.2 10^{-6} cm^2

device #3

run 1	latch after 3.4 10^6 ions/cm^2	voltage fell to 2.67 V
run 2	no latch after 5.0 10^6 ions/cm^2	
run 3	latch after 1.2 10^5 ions/cm^2	voltage fell to 3.91 V

average cross section = 3.5 10^{-7} cm^2

$^{20}Ne^{4+}$ ions, (energy 78 MeV), 60° incidence **LET 5.85 x 2= 11.7 MeV/mg/cm^2**, allowing for cosine angle dependence. No latch-up was seen after 4.1 10^6 ions/cm^2.

It is concluded that the threshold for latch-up is ~ 14.1 MeV/mg/cm^2

The device saturation cross section is unknown but must be > 2 10^{-6} cm^2 for the candidate CHRIS device. Since this is the value close to threshold, the saturation cross section is probably > 2 10^{-4} cm^2

An upper value for the cross section is the device area. Examination of a photomicrograph of the device gave an upper limit of ~ 2 10^{-2} cm^2 (assuming a 25% fill factor for sensitive area).

So we can reasonably predict that the saturation cross section is in the range 2 10^{-2} to 2 10^{-4} cm^2

6.7.2 LTC1415

No latch-up was seen up to the maximum LET of 28 MeV/mg/cm^2 and a fluence of 5.3 x10^6/cm^2.

7. CCD MEASUREMENTS

7.1 INTRODUCTION

Measurements on the CTI of proton damaged CCDs were performed in order to evaluate the effects on the star position accuracy of star trackers operating in moderate to high proton radiation environments. The effect of CTI is to trap signal charge and release it at a later time in the readout. The study concentrated on vertical CTI measurements since these are more straightforward to make and also more important for the application. The horizontal CTI is reduced for star tracker conditions because the pixel time is usually <1 μs and so is less than the capture time. Also, the trapped charge is spread horizontally over many pixels and so does not distort the star centroids (though there will be a contribution to signal loss).

The main interest is for medium accuracy star trackers which require a centroiding accuracy ~ 0.1 pixels and usually operate at temperatures in the range –10°C to –30°C at frame (update) rates of 1 to 10 Hz.

- charge trapped during frame transfer (when lines are moved at a fast rate) tends to be released over a large number of pixels and is effectively lost –making the stars appear fainter and hence more difficult to detect (and make position determinations more noisy). Charge trapping in the horizontal register will also tend to have this effect.

- charge trapped during line readout (when the line moves are relatively slow) tends to release charge over a small number of pixels and so tends to distort the star image and to give an incorrect centroid measurement.

In general the CTI is not a fixed parameter. It depends on:

- signal size
- background (e.g. level of dark signal, stray light or artificially introduced ‘fat zero’)
- clocking (the charge trapped depends on the ‘dwell time’ within a pixel and hence on the rate of moving pixels: CTI tends to be higher for line moves during readout compared with line moves during frame transfer)
- temperature: since this affects the trap emission time and also the thermal dark signal (which affects the background).

All these factors may be inter-dependent.

Although previous work at Sira and elsewhere has established the basic principles of charge trapping, detailed CTI measurement has only really become possible with the use of convenient and fast measurement methods, such as the First Pixel Response, FPR, technique (described below) – and few detailed CTI measurements (revealing the dependencies on signal, background and line move time) have yet been published in the open literature.

A starting point for this study was to characterise the CCD02 and CCD47 devices in detail. This was followed by measurements of star centroid shifts. The experimental techniques used are briefly discussed below. The CCD47-20 has been studied in the frame of the GAIA project (see Sira Report A/1330/01/16, March 1999). However this concentrated primarily on the effects of charge pre-injection on keeping traps filled (so that they cannot contribute to CTI). This study

concentrates on effects at higher temperatures, where pre-injection is not effective (because of the higher temperature and hence shorter emission time).

7.2 MEASUREMENT METHODS

7.2.1 First pixel Response (FPR)

In a frame transfer CCD the basic principal of the FPR method is to use flat field illumination to provide signal charge and to use the split in the electrode structure between the image and storage region clocks to move the storage region charge towards the readout register and hence to create a 'gap' in the flat field image (equivalently the image region clocks can be operated backwards so as to move charge away from the image/storage boundary). The creation of the gap gives a sharp edge to the signal region (Figure 7.2-1), the first line of which looses charge due to trapping. Subsequent lines experience less charge loss because the traps are partially filled (by the signal in preceding lines). Eventually (after several lines into the signal region) an equilibrium is reached where charge loss equals charge deferred. The CTI can then be calculated from the difference (ΔS) between this equilibrium signal value (S) and the first line of signal pixels (the first pixel response):

$$CTI = 1- [1- (\Delta S/S)]^{1/N} \qquad (7.2\text{-}1)$$

where N is the number of line transfers needed for readout.

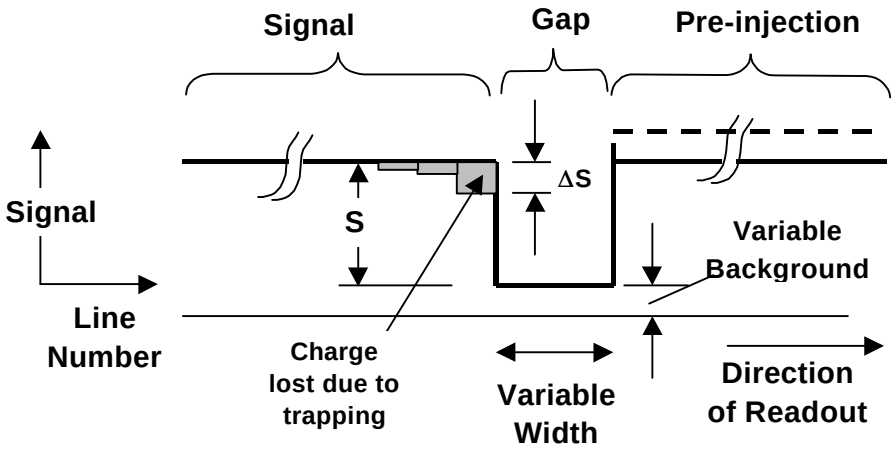

Figure 7.2-1 Vertical slice (column direction) through a CCD image showing signal versus line number when using a clocking sequence for First Pixel Response (FPR) measurements.

With this clocking technique there is inevitably charge (from the illumination) present in the lines before and after the ‘gap’. This is so that the gap can be created electronically (by clocking) rather than optically (e.g. by imaging of a knife edge), which is less sharp. The charge readout in front of the ‘gap’ acts to fill traps ahead of the charge after the gap and so acts as a pre-injection charge pulse. The width of the ‘gap’ can be varied so that the emission times of traps can be measured (if the time to clock charge through the gap region is much longer than the emission time then the traps have time to empty and a ‘worst-case’ CTI is measured). If the ‘gap’ region (together with the ‘signal’ region) is momentarily exposed to illumination (before readout) then a variable background signal can be created; likewise the charge in the ‘signal’ and ‘pre-injection’

regions can be independently varied (by exposure to illumination for controlled periods). To shield pixels from illumination during readout a store shield can be positioned over the storage region, alternatively, a mechanical shutter or LED pulse illumination can be used. For full-frame devices the gap can be formed at the boundary between the area clock electrodes and the readout register – though in this case there is no possibility for pre-injection. For devices with a split readout register (e.g. the CCD47), the technique can be used to determine horizontal CTI.

The emission time of traps was not investigated in detail in this study since it is known that in the present operating regime the E-centre is dominant and its time constants are reasonably well known. However some measurements were made with one CCD02 device

7.2.2 Measurements with Artificial Stars

Star images were projected onto the CCD (inside the cryostat) using a pinhole aperture and a long-working-distance microscope objective. The image was de-focused so that the peak signal (when centred on a pixel) was approximately half the total. This corresponds to a FWHM of ~ 1.1 pixels. A pinhole with multiple apertures was used and aligned so that two star images were centred on the same line when they were both positioned within a '0 krad' region (typically to an accuracy of < 0.05 pixels). Then the projection system was translated until one of the stars was in the irradiated region and one in the 0 krad region. Differences in the vertical centroids of the two stars indicate shifts due to CTI. Measurements were made for several vertical positions of the star within a pixel by making small vertical shifts in the spot position. Note that the vertical shifts do not have to be accurately made since they can be measured using the 0 krad 'reference star'.

Figure 7.2-2 shows a double star image when both are in an un-irradiated part of the CCD. The stars are of different brightnesses due to differences in the diameters of the pinholes (which could not be made accurately the same size. Figure 7.2-3 shows a typical situation where one of the stars in an irradiated region (in this case, 10 krad) and so has a 'tail' due to deferred charge.

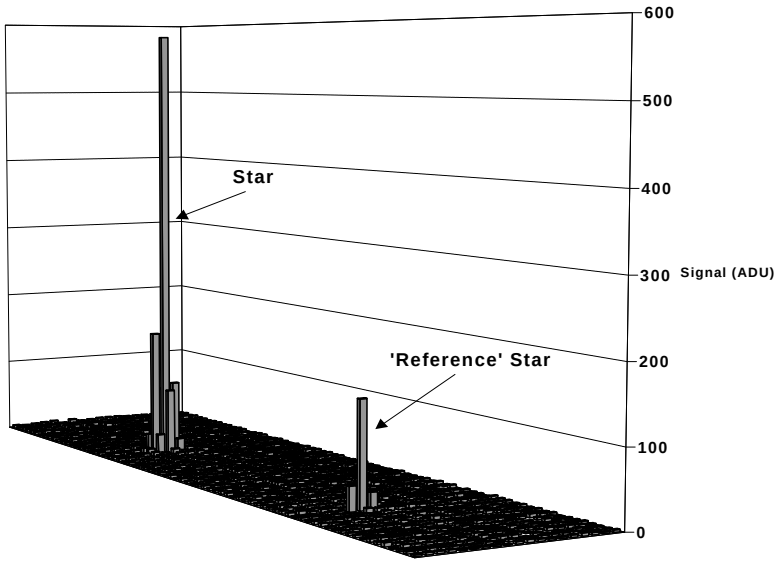

Figure 7.2-2 Double star image when both are in an un-irradiated part of the CCD

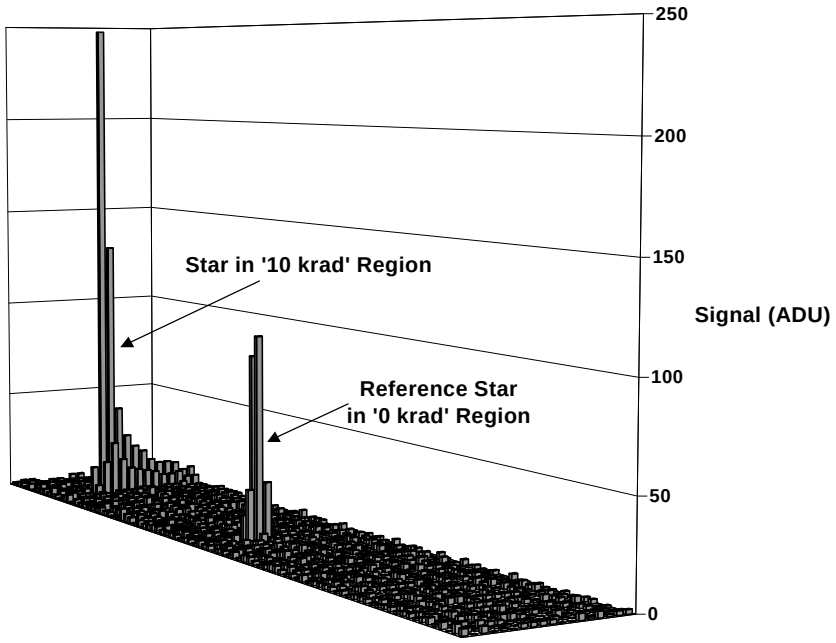

Figure 7.2-3 Double star image when one star is in irradiated (10 krad) part of the CCD. The CCD temperature was –32 °C.

For each star position an average of 16 frames was recorded and a selected region around the two stars was dumped to a Microsoft Excel™ spreadsheet for further analysis.

7.3 FPR RESULTS

7.3.1 CCD02

Results for vertical CTI versus background were obtained for both CCD02 devices and the grade 2 CCD47-20 device for two clocking speed conditions, three positions on the chip (approximately at the top, middle and bottom of the image) and several signal levels, thus forming a fairly comprehensive data set.

Figures 7.3-1 to 7.3-3 show CTI results for CCD02 device #A0723-51 at the top (line 20), middle (line 144) and bottom (line 220) of the image for the 4, 10 and 30 krad regions of the CCD. The plots are identified as follows:

- Filled triangles 4 krad data
- Open circles 10 krad data
- Filled squares 30 krad data
- Light green signal = 50 ADU = 800 electrons
- Blue signal = 130 ADU = 2,100 electrons
- Dark green signal = 360 ADU = 5,800 electrons
- Black signal = 1000 ADU = 16,000 electrons
- Red signal = 3000 ADU = 48,000 electrons

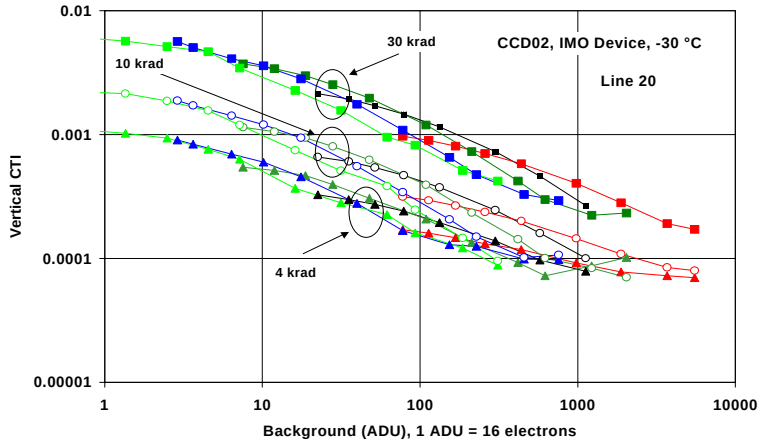

Figure 7.3-1 Vertical CTI obtained using the FPR method for CCD02 device #A0723-51. Top of CCD, 2.25 µs line move during frame transfer, 0.37 ms during readout

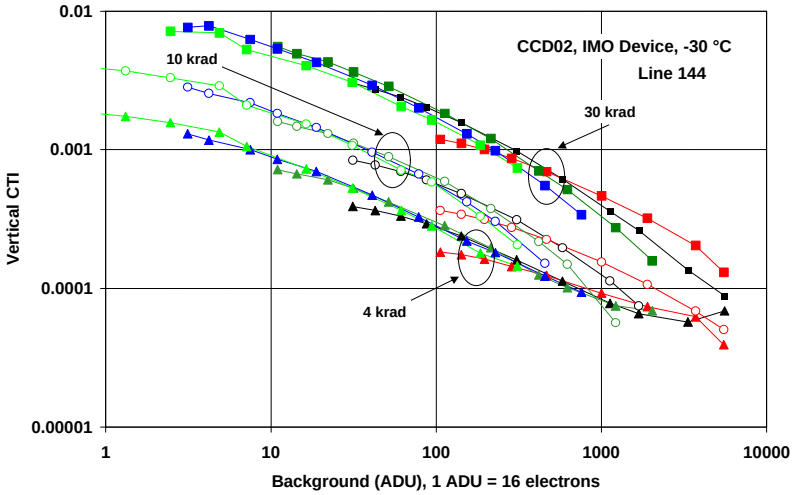

Figure 7.3-2 Vertical CTI obtained using the FPR method for CCD02 device #A0723-51. Middle of CCD, 2.25 µs line move during frame transfer, 0.37 ms during readout

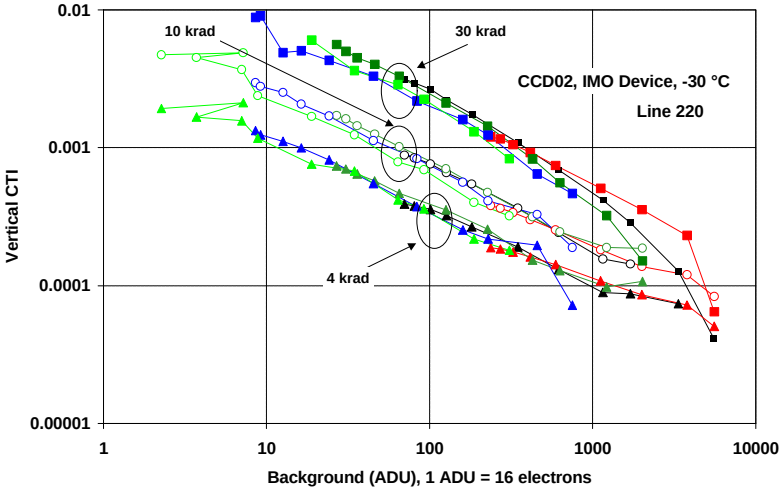

Figure 7.3-3 Vertical CTI obtained using the FPR method for CCD02 device #A0723-51. Bottom of CCD, 2.25 µs line move during frame transfer, 0.37 ms during readout

Figures 7.3-4 and 7.3-5 show additional centre- and bottom-of-image data obtained with the same device. As expected, all the plots show that the vertical CTI increases with proton fluence. It was found that all the plots for the different fluence regions on the IMO device could be superimposed if scaling factors to allow for the damage ratios were applied. An example is shown in figure 7.3-6. The same scaling factors were found in all cases and these corresponded well with the actual proton fluences (see figure 7.3-7). The figure also shows data from the advanced IMO (AIMO) device, which is discussed below. The CTI for the 4 krad region on the IMO device was always slightly high compared with extrapolations from the 10 and 30 krad regions but this is probably not significant given the 5% tolerance on dosimetry.

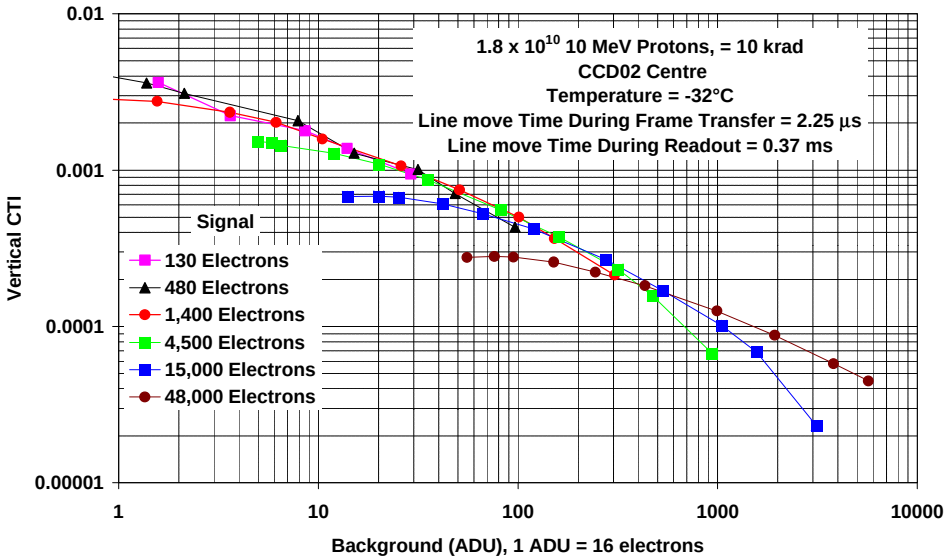

Figure 7.3-4 Additional data for vertical CTI for CCD02 device #A0723-51. Centre of CCD, 2.25 µs line move during frame transfer, 0.37 ms during readout

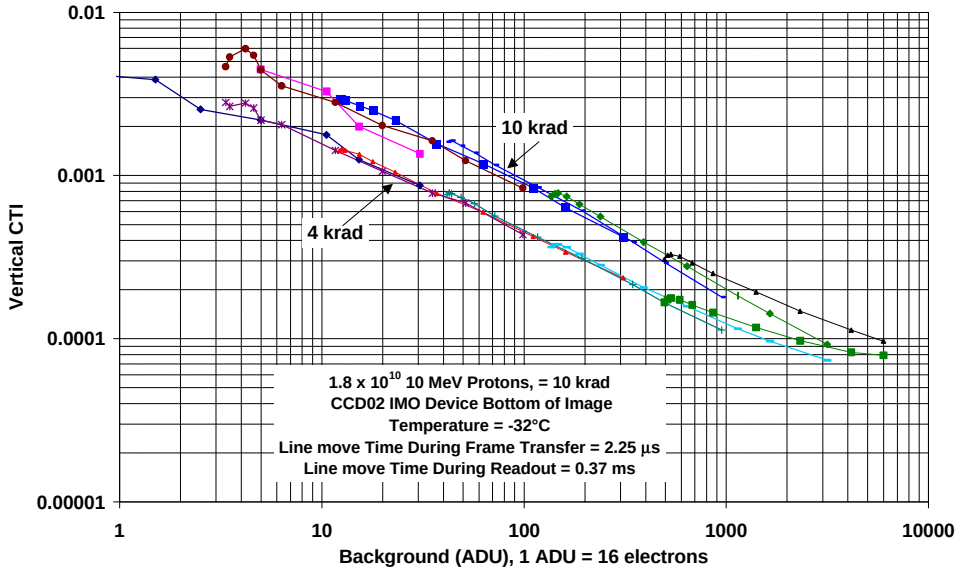

Figure 7.3-5 Additional data for vertical CTI for CCD02 device #A0723-51. Bottom of CCD, 2.25 µs line move during frame transfer, 0.37 ms during readout

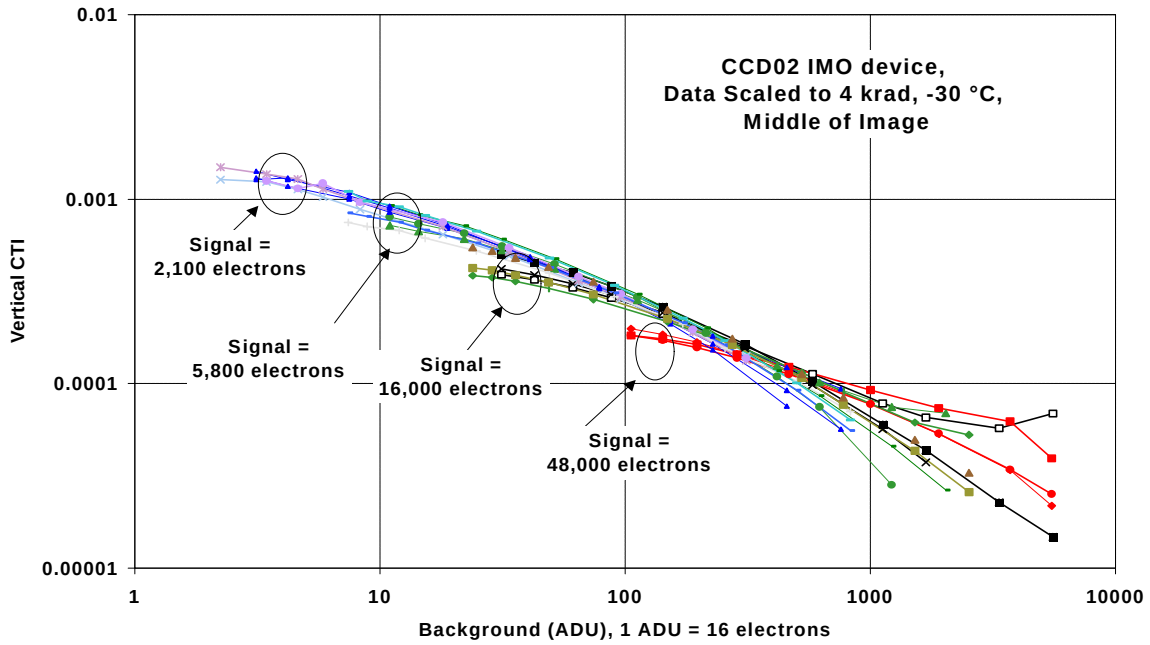

Figure 7.3-6 FPR data from figures 7.3-1 to 7.3-3 scaled so that the plots for the three fluence regions are superimposed on the 4 krad plot

The scaling seemed to break down at high signal and background levels and predominantly fast line moves (top of the image) – a case where the CTI is lowest, but is measured to be somewhat higher than expected, based on scaling of data for higher fluence or predominantly more slow line moves. Note, however that in the low CTI regime the measurement errors will be more significant and it is possible that this non-scaling is simply a measurement artefact.

It can also be seen from figures 7.3-1 to 7.3-5 that the form of the curves changes with position in the image, that is with the number of slow (readouts) compared with fast (frame transfer) line moves. At the top of the image (predominantly fast line moves) there is a dependence of the CTI on signal. High signal gives improved CTI at low backgrounds but slightly worse CTI at high backgrounds. At the bottom of an image (roughly 50% fast line moves) there is very little dependence on signal level. Data for the centre of an image is between the two extremes and the dependence on signal is not strong. This lack of signal dependence will be useful when considering simulation of CTI effects on an image. To a first approximation it appears not to be necessary to model the changes in CTI as charge is moved through the device and the signal changes (due to the trapping processes that occur on the way). Instead, it should be possible to model the effects by assuming a constant CTI (but still dependent on background level).

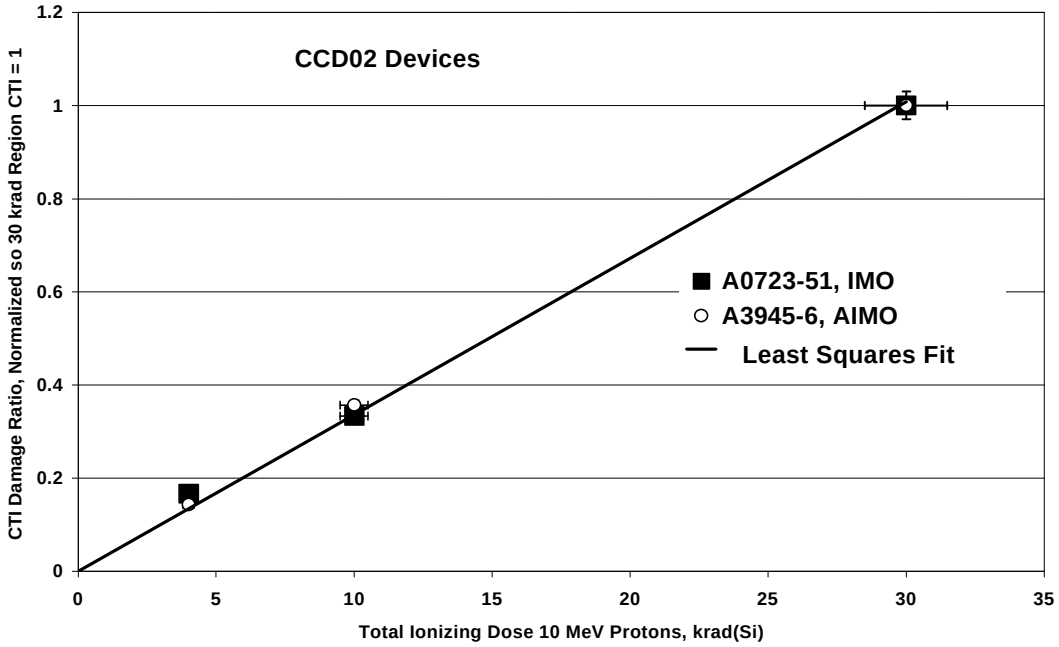

Figure 7.3-7 CTI Damage factor (averaged from all data and normalised so the 30 krad value = 1)

From the data for the three chip positions it is possible to derive the ratio between the CTI values for fast and slow line moves. This was done by scaling the plots for the bottom and centre of an image so that they were superimposed on those for the top (as far as possible given the changes in shape of the curves). Figure 7.3-8 gives all the data from figures 7.3-1 to 7.3-3 scaled for proton fluence and position in the image. The superimposition is quite good, indicating that the CTI versus line move time relation is not strongly dependent on background. It was however found to depend on signal and different scaling factors were used for the different signal levels. Figure 7.3-8 also contains IMO device data obtained at the slower line move rate (6.75 μs during frame transfer, 0.875 ms during readout). As might be expected the CTI ratio remained the same (the ratio of the line move times is approximately the same) but all the CTI data was increased by approximately 10% (because of the longer dwell time). The shape of the CTI plots was not significantly affected by the 3 times increase in line move time.

Figure 7.3-9 shows data for the AIMO in comparison with the IMO device . For the AIMO chip the scaling is not so good, indicating that the shape of the curves is changing with line move time. However the concept of scaling is still reasonably valid to a first approximation. It is not known if these changes in curve shape are due to device-device differences or are related to the difference in electrode structure (IMO versus AIMO). The derived CTI ratios are shown in figure 7.3-10. It can be seen that the CTI for fast (2.25 μs) line moves is approximately 2.5 times less than for 0.37 ms line moves. This dependence is consistent with other measurements at Sira. In fact the first report of a dependence of CTI on the dwell time in a pixel was Hopkins et al 1994* and the factor ~ 2.5 is exactly as reported in that paper. The data for the AIMO is likely to be more approximate than that for the IMO CCD due to the problems with scaling mentioned above.

* I. H. Hopkins, G. R. Hopkinson and B. Johlander, 'Proton-induced charge transfer degradation in CCDs for near-room temperature applications', IEEE Trans. on Nuclear Science, NS-41 (6), pp 1984-1991 (1994)

Note that, although some data was obtained at the 2.25 µs/0.37 ms line move rates, the data presented here for the AIMO device was for the slower 6.75 µs/0.875 ms rate and has been scaled by a factor 1.1 for comparison with the IMO data. A scaling factor of 1.3 was also applied for the top-of-image data for the IMO device to allow for emission time effects (as discussed below). Note also that in the plots for the AIMO device the lower conversion gain of this device (12 electrons/ADU rather than 16 electrons/ADU for the IMO device) has been allowed for and the background values have been scaled to a gain of 16 electrons/ADU as noted in the labels for the x axes of the plots.

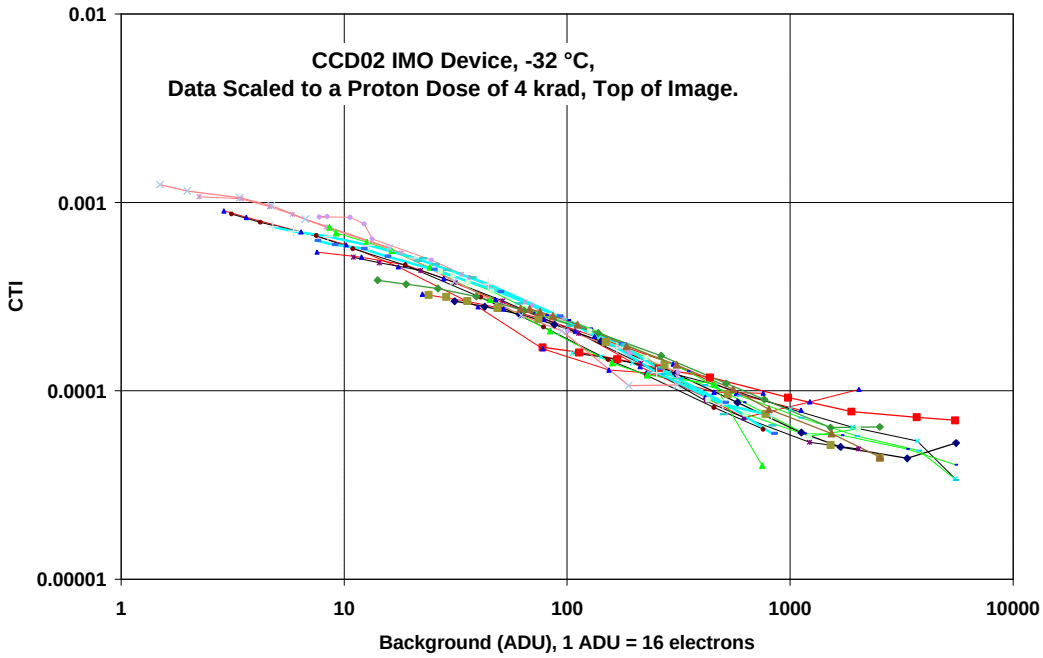

Figure 7.3-8 CTI data for the IMO CCD scaled so that the plots for the three image positions are superimposed on the 4 krad plot

Because the AIMO device cannot be clocked backwards in the vertical direction, the FPR clocking sequence was different to that used for the IMO chip. The different clocking sequence allowed an estimation of the emission time constant by measurement of the CTI as a function of the time delay between the sharp edge (used for the first pixel charge loss measurement) and preceding charge which acts to fill traps in advance of the sharp edge (labelled 'pre-injection' in figure 7.2-1). This data is shown in figure 7.3-11 together with a theoretical exponential curve with a time constant of 1.4 ms which is the calculated value of the emission time at –32 °C for the E-centre. It is seen that there is a good agreement with the theory, indicating that the E-centre is the dominant trap in these conditions. The delay time used for the measurements discussed above was ms and so a correction factor of 1.3 was applied to the top-of-image data to allow for pre-injection during frame transfer (pre-injection during readout is not important since traps can fully emit during the slow line moves involved).

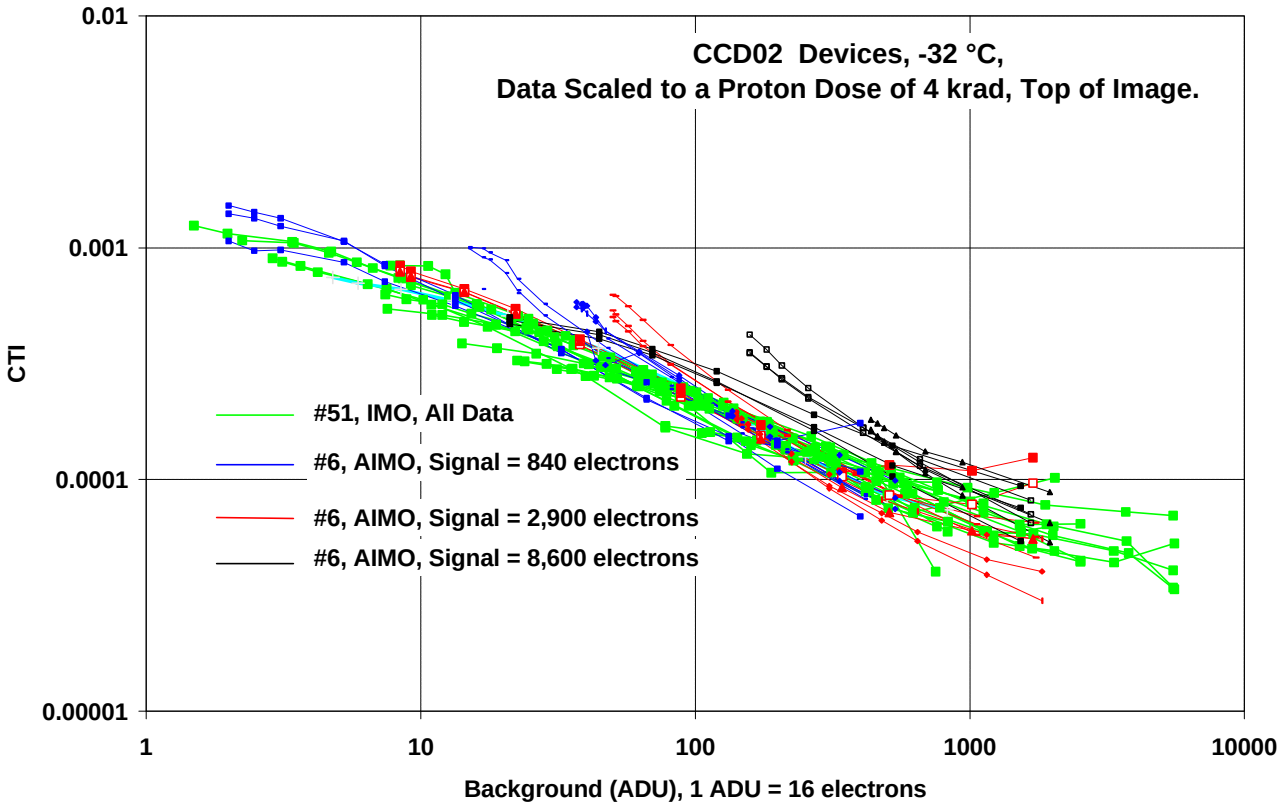

Figure 7.3-9 CTI data for the AIMO CCD scaled so that the plots for the three image positions are superimposed on the 4 krad plot. Also shown (in green) is the data for the IMO CCD (from figure 7.3-8).

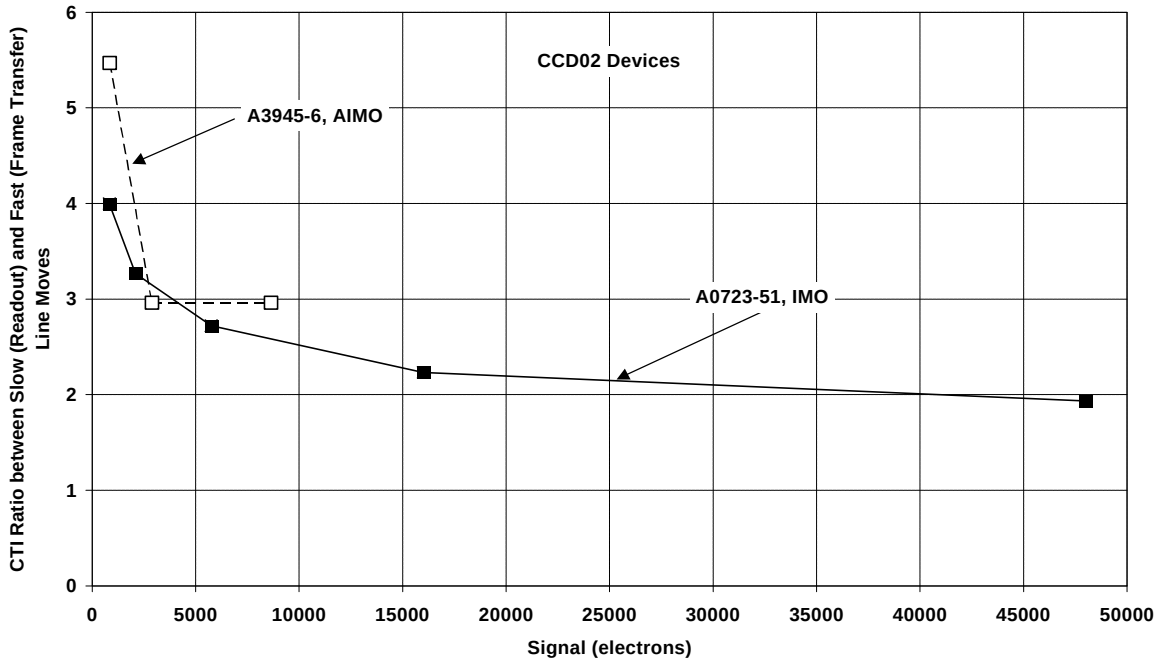

Figure 7.3-10 Derived values of the CTI ratios for 2.25 μs and 0.37 ms line moves. Data for the advanced inverted mode device #A3945-6 is also shown.

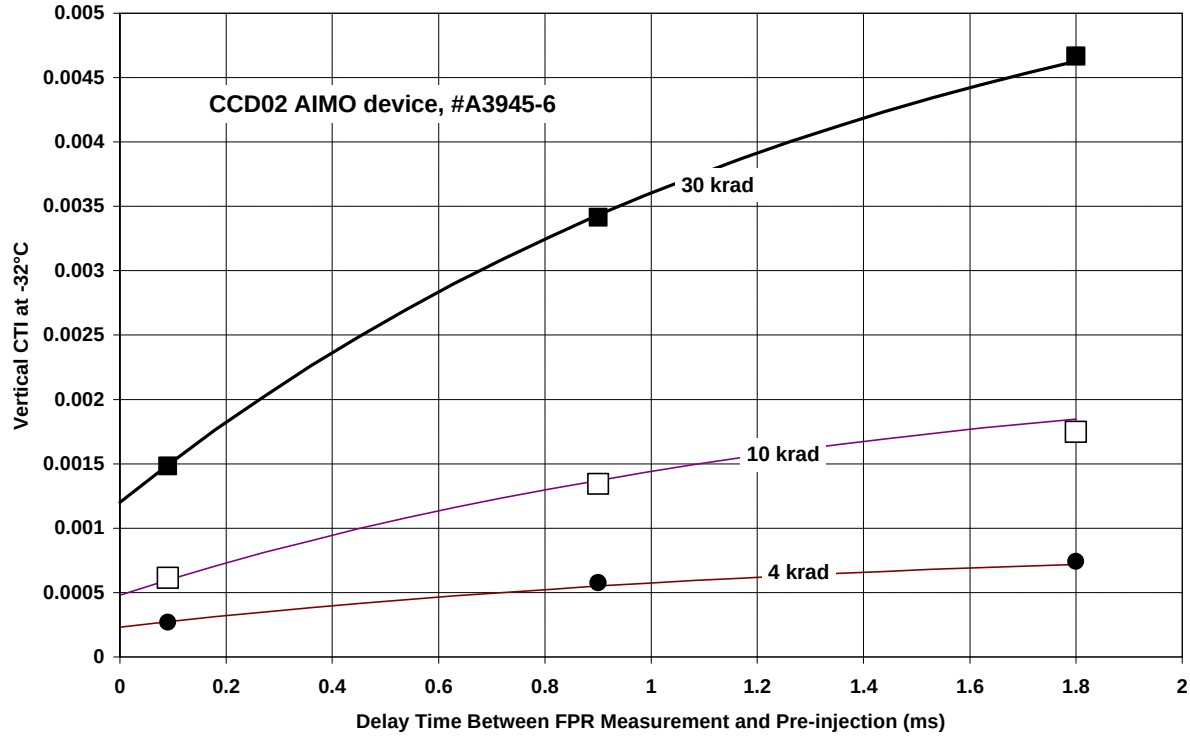

Figure 7.3-11 Measurements of the trap emission time for the AIMO device, the data can be fitted assuming an emission time of 1.4 ms.

7.3.2 CCD47

This section discusses FPR measurements on CCD47-20 device # 7271-2-3. The other CCD47-20 was of identical design and was kept as a spare. Figure 7.3-12 shows data scaled for both proton dose and position in the image (as discussed for the CCD02). The plots are colour coded for the image size (as explained in the figure caption). There is some spread in the data but it is apparent that the plots for a given signal size cluster together. This is clearer if data for a single dose region are plotted. Figure 7.3-13 gives data for the 10 krad region, again scaled for position in the image. It is seen that the shape of the plots, for a given signal size, are almost identical. This is in contrast to the CCD02 where there was a variation in the shape with position (i.e. with dwell time).

Figure 7.3-14 shows the CTI ratio for fast (4 μs) and slow (0.48 ms) readouts derived from the position-in-image scaling as well as the values derived for the two CCD02 devices. The results are very similar.

Figure 7.3-15 compares all the data for the CCD02 (in black) and CCD47 (in red) devices with the background values scaled to a conversion gain of 16 electrons/ADU. It is difficult to compare individual curves because of the different variations with dwell time and signal scaling for the different device types, but approximate trend lines have been drawn by eye and it can be seen that the CCD47-20 has roughly a factor 3 lower CTI at low backgrounds and roughly a factor 2.5 lower at high signals. This is as would be predicted from the ratio of the pixel areas (22 μm x 22 μm for the CCD02, 13 μm x 13 μm for the CCD47, giving an area ratio of 2.9).

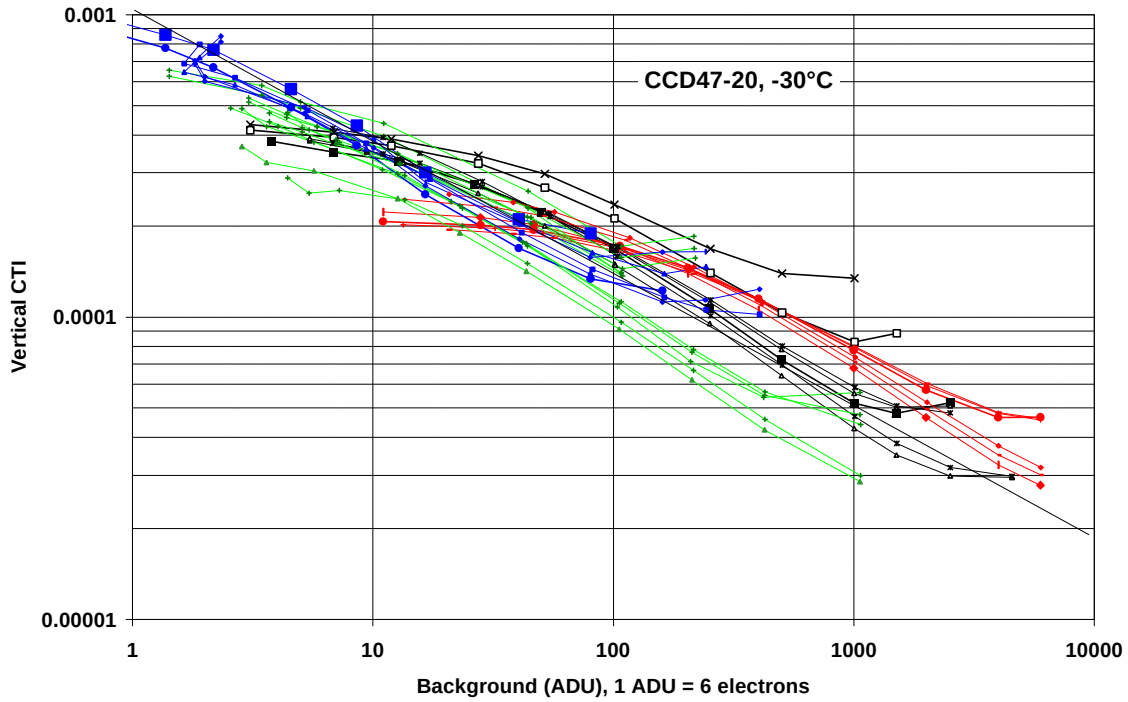

Figure 7.3-12 FPR measurements for the CCD47-20 device, scaled to a 10 MeV proton total ionizing dose of 4 krad(Si) and for position at the top of the image (signal-size-dependent scaling factors have been applied to the centre- and bottom-of-image data). The plots are colour coded to identify the signal size:
blue: 85 ADU (510 electrons), green: 200 ADU (1,200 electrons),
black 520 ADU (3,100 electrons), red:2000 ADU (12,000 electrons),

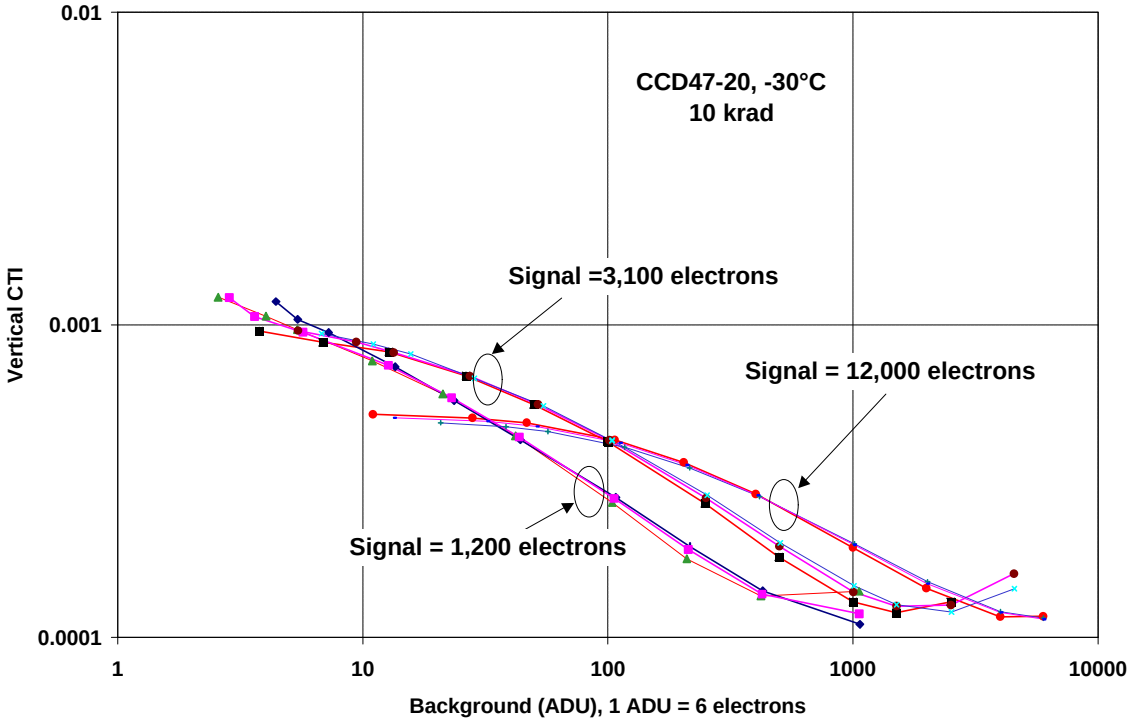

Figure 7.3-13 FPR data for the 10 krad region, scaled for position in the image

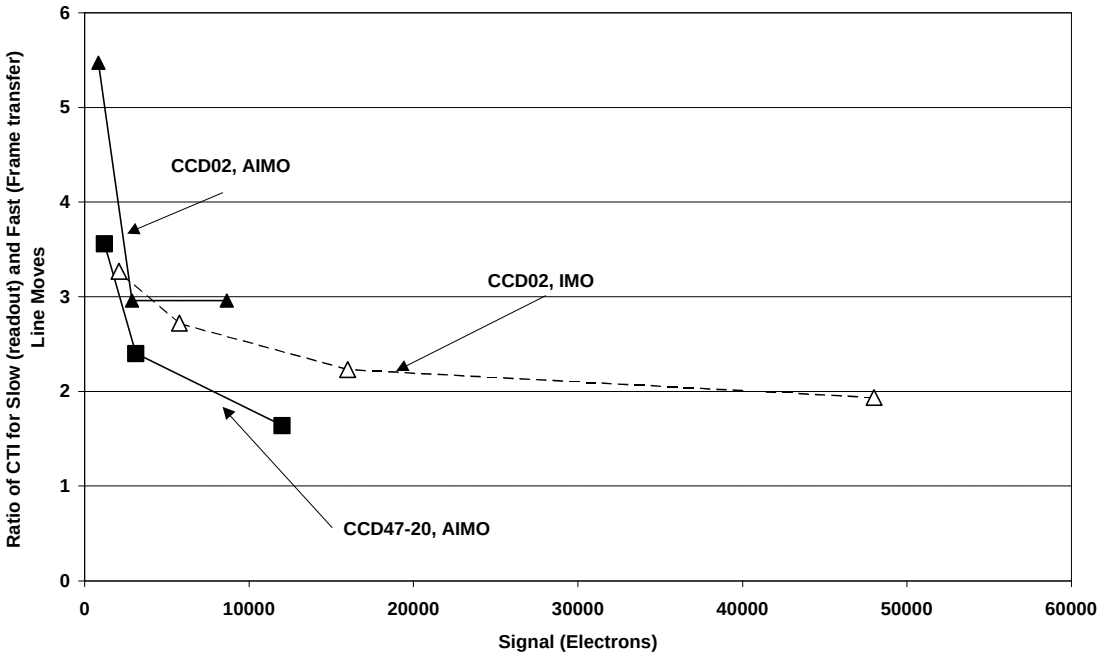

Figure 7.3-14 CTI ratio for fast (4 μs) and slow (0.48 ms) readouts derived from the position-in-image scaling as well as the values derived for the two CCD02 devices.

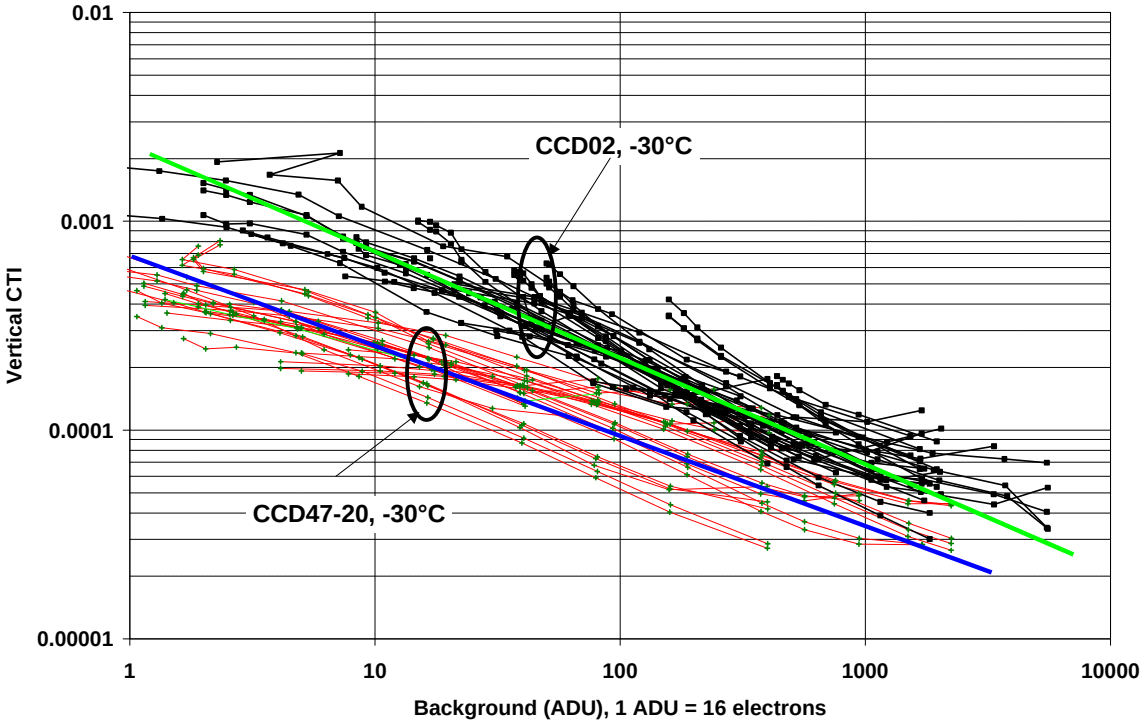

Figure 7.3-15 All the FPR data for the CCD02 (black) and CCD47 (red) devices with background values scaled to a conversion gain of 16 electrons/ADU. The blue and green trend lines have been drawn by eye.

7.4 STAR CENTROID DATA

7.4.1 Introduction and Discussion of Simulation Models

The CTI results discussed above suggest that the smearing effect on star images will be strongly dependent on the background but will only be slightly dependent on the signal level. To test these predictions and to estimate the overall effect on star position accuracy data was collected using the double aperture spot projection system described above (section 7.2.2). Data was collected from averages of 16 frames for blocks of 5 x 5 pixels centred on the star positions in the 0 krad and irradiated regions (either 4 or 10 krad). Star centroid positions were calculated using a centre of gravity algorithm on a 3 x 3 matrix of data:

$$\text{Centroid position (pixels)} = \frac{-0.5*A + 0.5*B + 1.5*C}{A + B + C} \qquad (7.4\text{-}1)$$

Where A, B and C are the summed signals (with background subtracted) for the three rows of three pixels.

Data was obtained for several positions of the star within a pixel and for several signal sizes and backgrounds. Two CCD temperatures (-32 and –25 C) were used as well as several positions of the star within the image. For the CCD47-20, which has a dump gate, the effect of fast 'windowed' readout was also investigated.
The centroid error for 0 krad, which should ideally be zero, was measured by positioning both spot images within the 0 krad region. A constant 'error' of 0.1 pixels was measured. This was due to a small misalignment in the spot illuminator. Since this bias error was found to be constant it can be allowed for in the interpretation of the results.

The centroid measurements were compared with the results of simulations made using the CTI data discussed above. Sira has an in-house C-code simulation model based on previous CTI data for CCD02 devices. This simulates the transport and trapping of charge packets through the CCD but it does not take into account the new CTI data presented above, also it is known that this simulator does not precisely model the effect of trap filling by preceding charge packets (the leading edge of the star image). The weak dependence of the CTI on signal size suggests that a simpler model which uses a constant CTI value (though still dependent on background) can be used. This was implemented using a Microsoft Excel™ spreadsheet. After each pixel transfer during readout the charge loss for the pixels in the 5 x 5 block was calculated using the assumed CTI value and the charge emitted from previous transfers estimated from previous charge losses and assumed values for the line move time and the trap emission time.

The model also assumes that there is negligible image distortion from line moves during frame transfer (because in this case trapped charge is expected to be spread over a large number of trailing pixels and, though giving a loss in signal size, should not give a large distortion to the star images). It will be seen that this assumption is not correct. This inaccuracy is likely to be due to a combination of the presence of fast traps and the effect of the signal dependence of the CTI and the effect of 'pre-injection' due to the presence of previous charge packets. Hence the model gives incorrect results when the CTI effects are dominated by fast line moves (that is for stars at the top of the image or when windowing is used). However the spreadsheet model gives good results for the case where the smearing is mainly due to slow line moves.

Although the previous C-code Sira model does not give an accurate simulation of the centroid error as a function of position in a pixel it will be seen that the windowed readout case is fairly well represented without needing to assume fast trapping states.

To summarise, there are two simulation models available at present. The C-code simulator does not precisely model the centroid effects either for fast or slow line moves but is within a factor two. The Excel™ model gives a good prediction for situations were the CTI due to slow line moves is dominant but neglects CTI due to fast line moves. In cases where the CTI due to fast line moves is important (top-of-image data or windowed mode) then the C-code model has to be used.

7.4.2 CCD02

Figure 7.4-1 shows measured and 'true' (i.e. reference star) centroid positions for a variety of signal and background conditions for the IMO CCD02 (10 krad region, bottom of image). Also shown (as thick black lines) are predictions from the spreadsheet model, which are labelled with the CTI value assumed. These assumed values are as close to the measured CTI values (c.f. figure 7.3.3) for the bottom of the image if a correction factor is applied to take into account the fact that the CTI data is calculated from the ***total*** number of line moves (including frame transfer) whereas the spreadsheet model considers only line moves during readout. This correction entails a multiplication of the plotted CTI values by 1.5.

Several conclusions can be made

- Centroid errors are large for low backgrounds, even for low irradiation levels.
- Provision of background (or 'fat zero') has a large effect on the centroid errors. The most effective way of improving accuracy (better than increasing star brightnesses or changing the temperature) is to increase the background level (to > 1000 electrons/pixel for environments giving 4 krad(Si) or more).
- The centroid shifts do not change much with location within a pixel but the worst case for errors is when the star is on the boundary between pixels (rather than being centred on a pixel)
- For the same signal and background, the error tends to be worse as the temperature is increased (from –32°C to –22°C). This is because the differed charge is spread over fewer pixels at the higher temperature and tends to distort the star profile more. This is illustrated in figure 7.4-2.
- Increasing the line move times did not have a large effect on the centroid errors
- The centroid error for stars at the top of an image is significant and is ~ 0.1 pixels at low backgrounds. As discussed above this is likely to be due to the signal dependence of CTI for fast line moves but there will also be a contribution from emission from any fast trapping states.

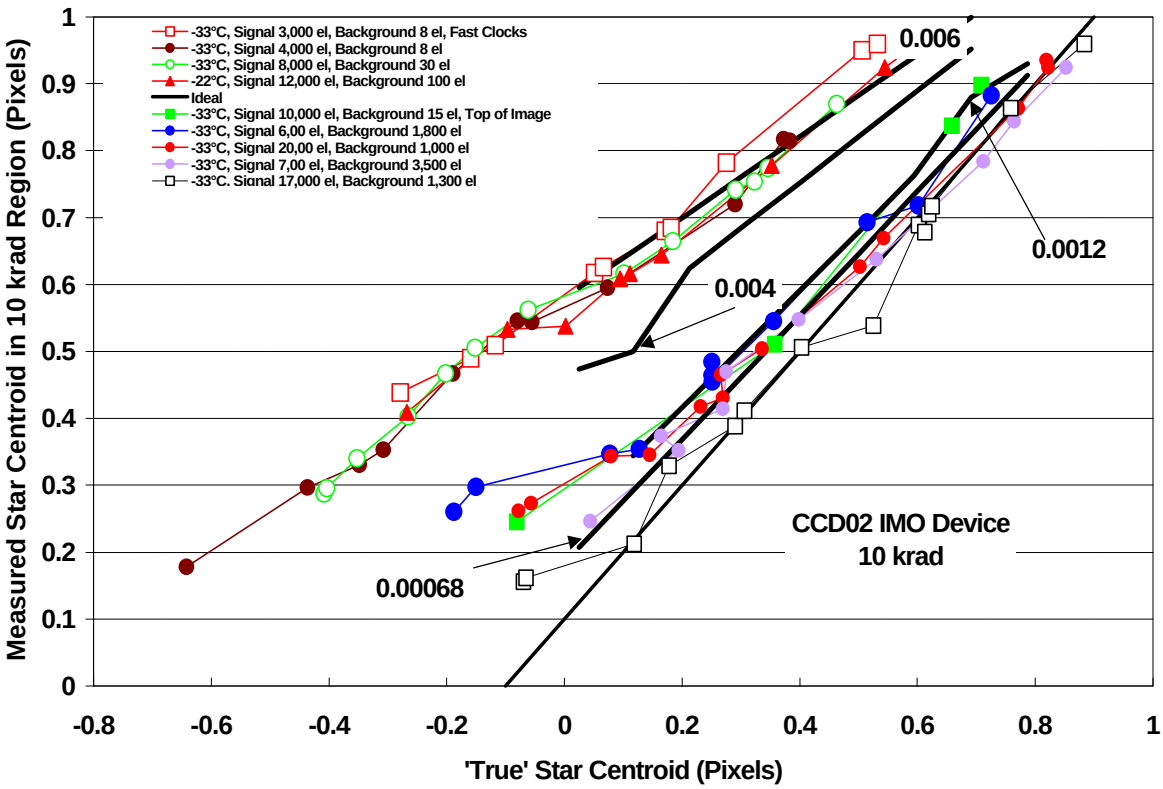

Figure 7.4-1 Centroid errors for the IMO CCD02 device, with the spot positioned near the bottom of the image (line 256). The lower thick solid line represents the 0 krad case. There is an approximately 0.1 pixel error due to in the alignment of the two stars. The other thick black lines are the results of spreadsheet simulation and are labelled with the assumed CTI value.

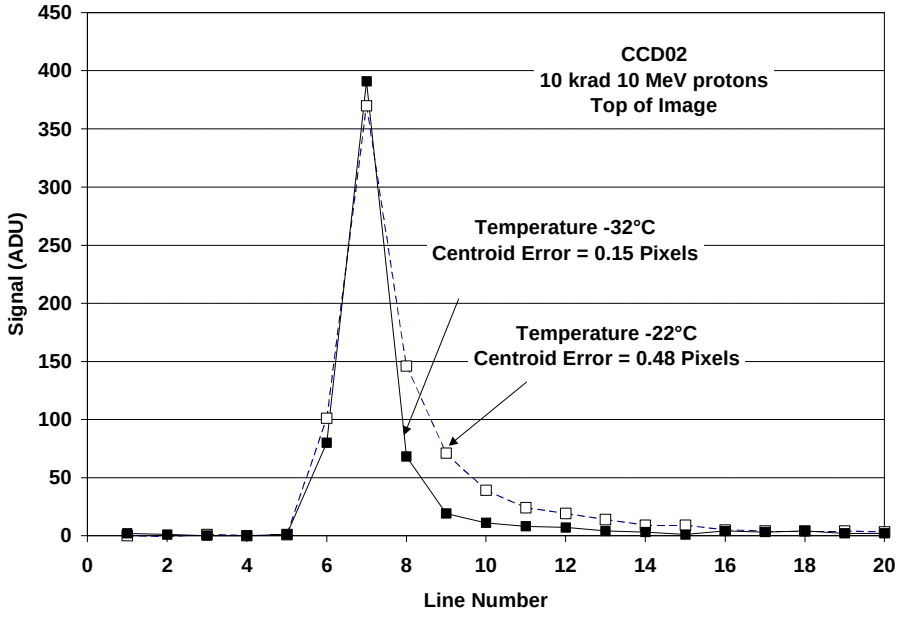

Figure 7.4-2 The effect of *increasing* the CCD temperature from –32°C to –22°C is to *reduce* the trap emission time from ~1.3 ms (1.5 line move times) to ~0.7 ms (0.8 line move times) and *increase* the centroid error even though the star profile appears more symmetrical.

7.4.3 CCD47-20 results

Figure 7.4-3 shows results for the CCD47-20 after 10 krad with the spot positioned in the centre of the image (line 512). These are very similar to the CCD02 results shown in figure 7.4-1. Plots for the three different signal levels are shown in blue, red and green. The centroid error decreases as the background increases and there is also a dependence on the signal size. The simulations were based on the CTI values found using the FPR method. Figure 7.4-4 marks the values used and these have been multiplied by 1.5 to allow for the increase in CTI with line move time (the simulation assumes only 512 slow line moves).

Figures 7.4-5 to 7.4-9 show the effect of increasing the CCD temperature from –33º C to –17º C, of windowing, of readout from the top of the image and at 4 krad.

The trends are essentially as discussed above for the CCD02. Figure 7.4-9 shows that even at 4 krad 10 MeV protons (which is a typical environment for LEO) centroid errors are significant unless either a high background, or windowed operation are used.

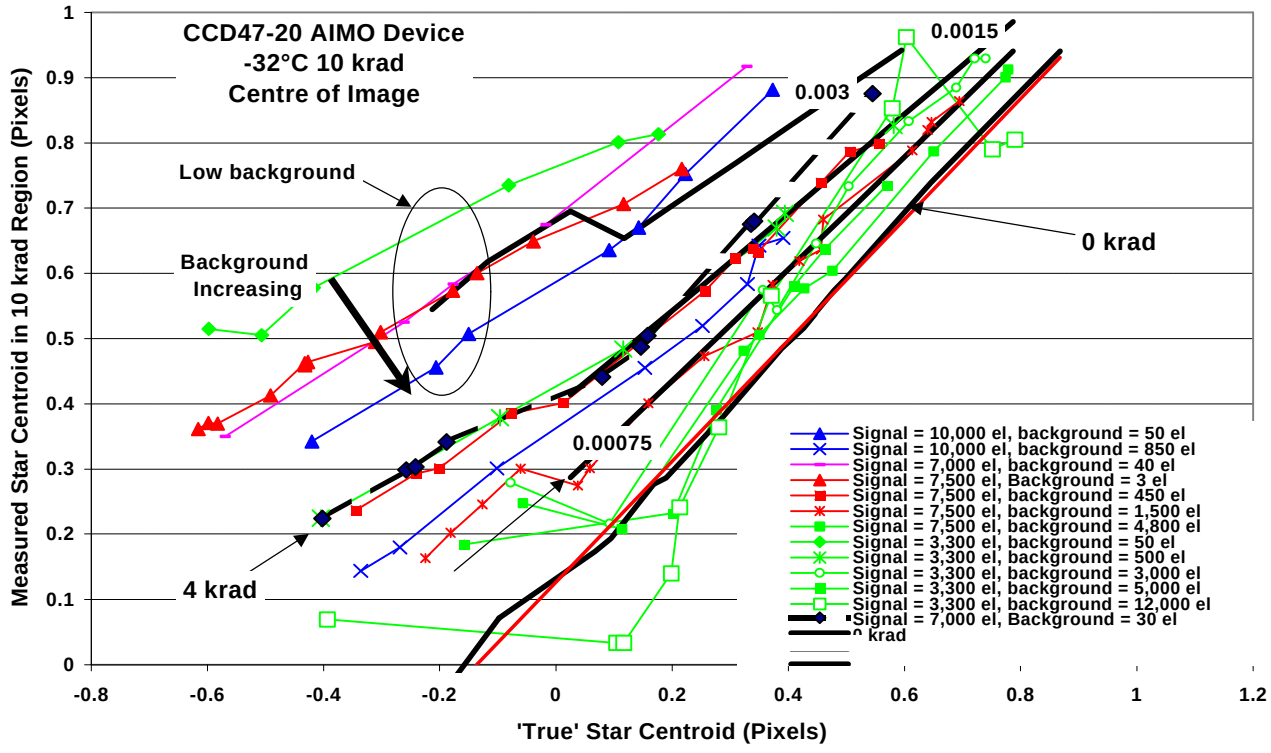

Figure 7.4-3 Centroid errors for the CCD47-20 device. The lower thick solid line represents the 0 krad case. There is an approximately 0.1 pixel error due to in the alignment of the two stars. The other thick black lines are the results of spreadsheet simulation and are labelled with the assumed CTI value.

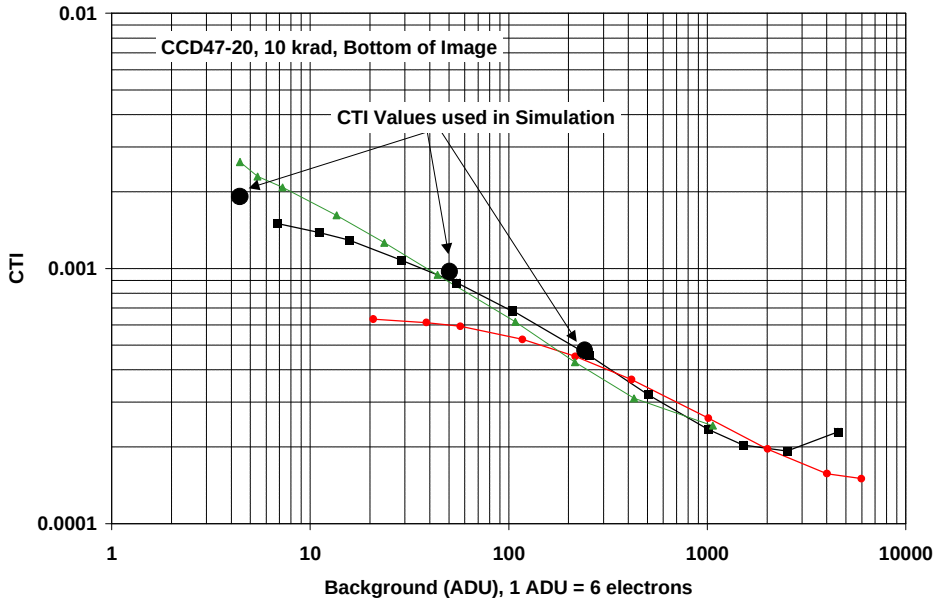

Figure 7.4-4 The CTI values used for the spreadsheet simulations shown in figure 7.4-3. These have to be multiplied by 1.5 to allow for the line move time.

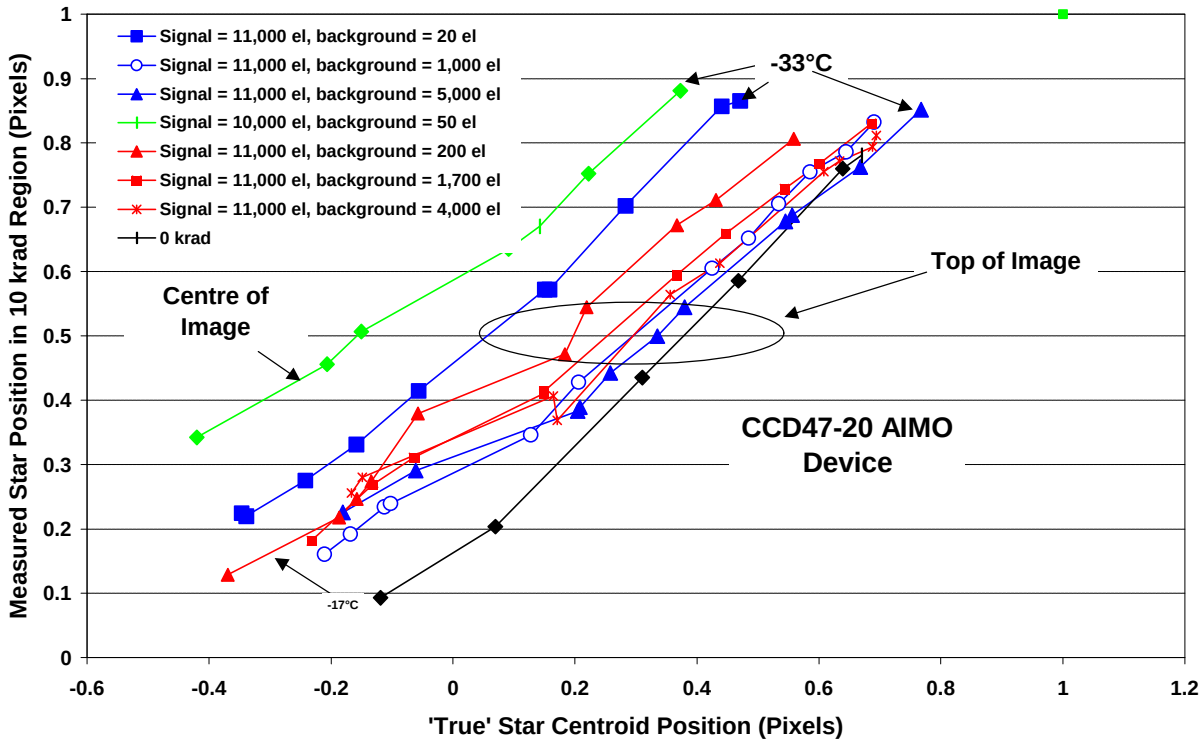

Figure 7.4-5 Centroid errors for the top of the image at –33°C (blue) and –17°C (red) compared with –33°C values at the centre of the image (green symbols)

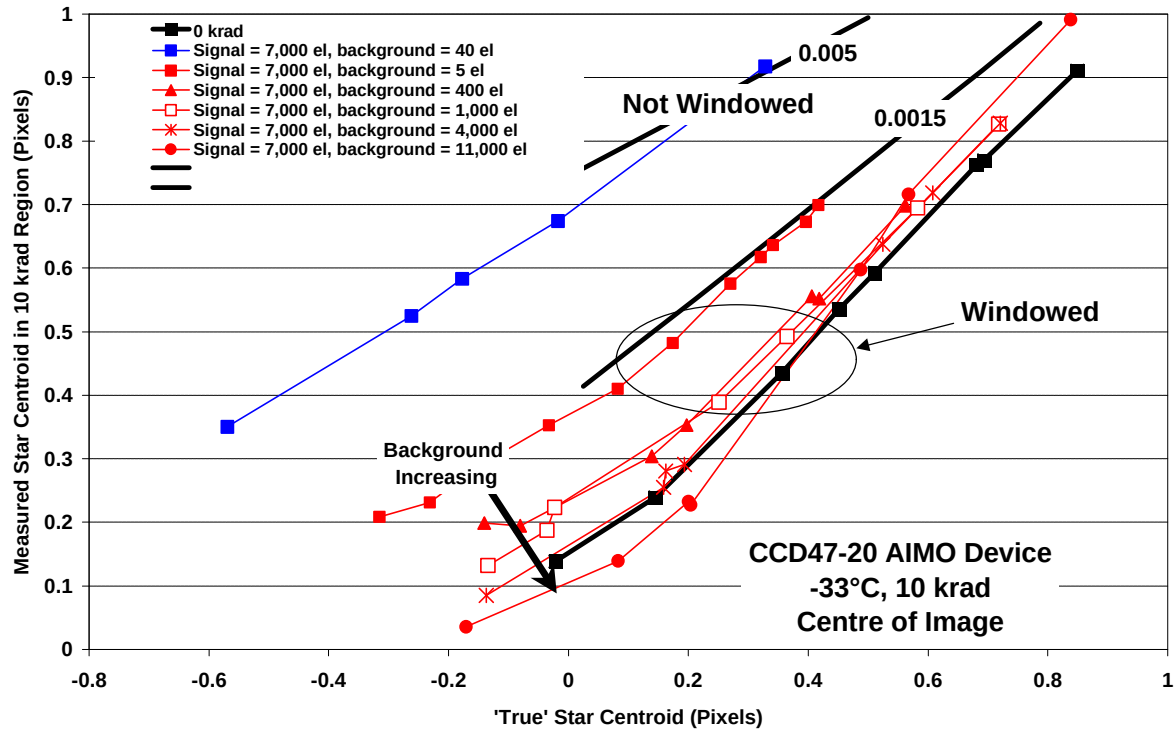

Figure 7.4-6 The effect of windowing on centroid errors for the 10 krad region at –33°C

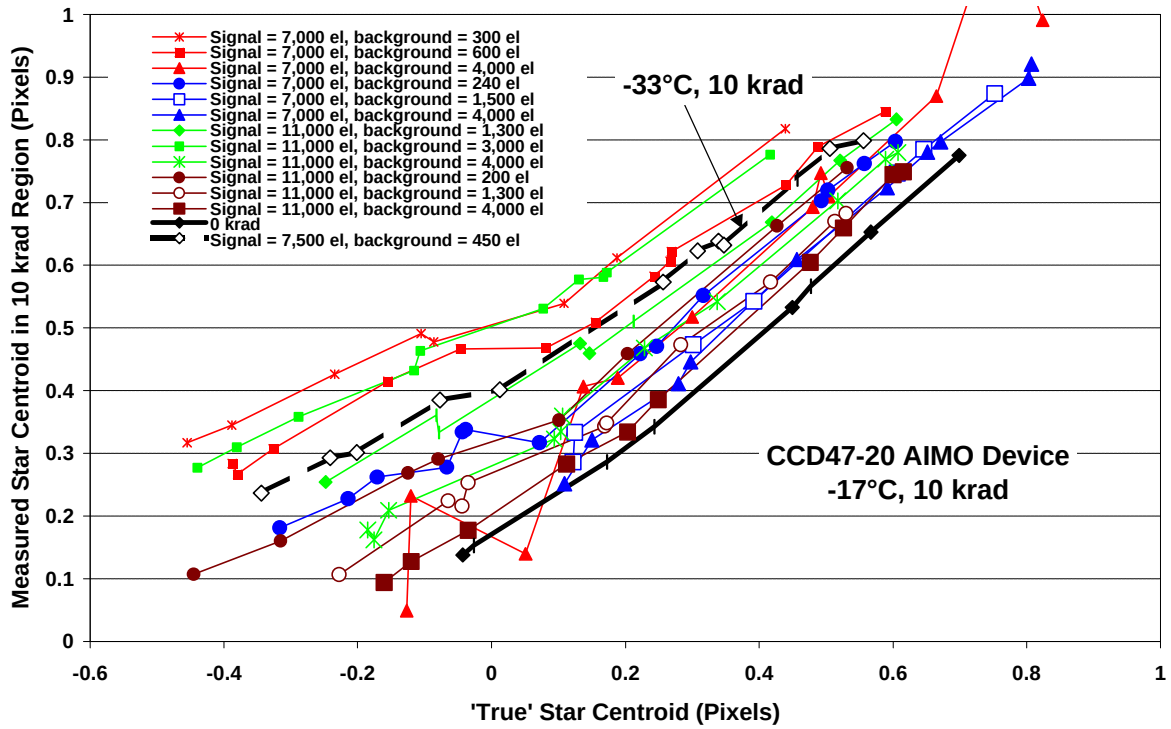

Figure 7.4-7 The effect of windowing on centroid errors for the 10 krad region at both –32°C and –17°C

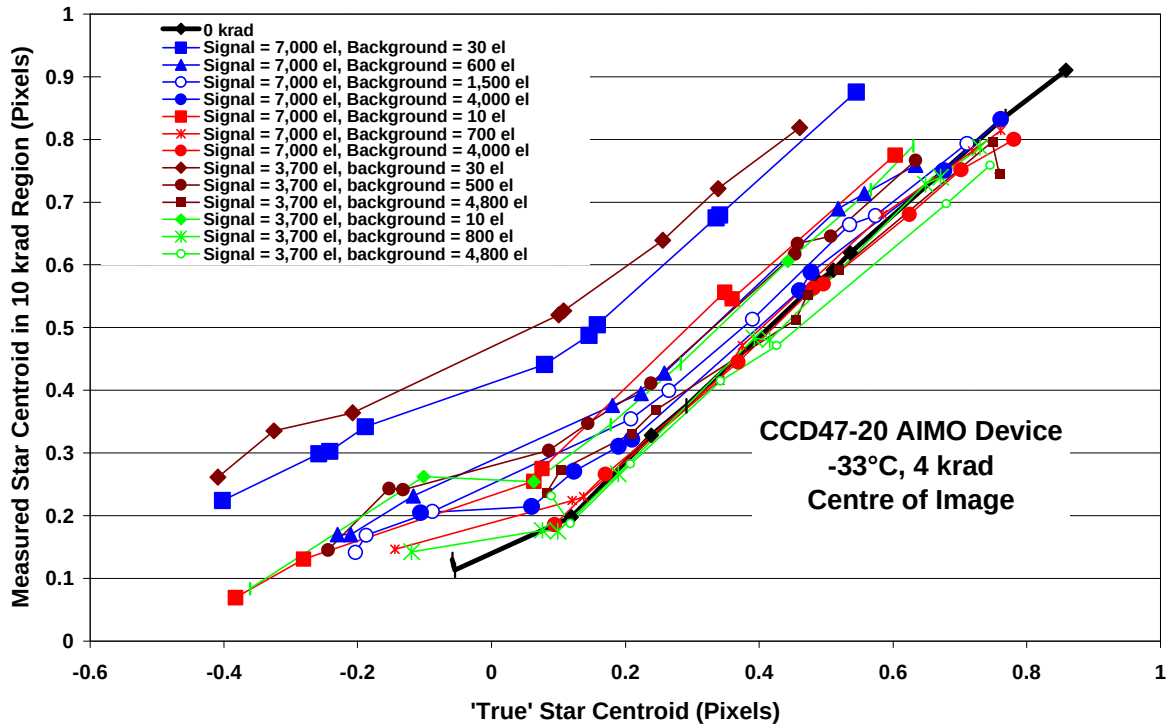

Figure 7.4-8 The effect of windowing on centroid errors for the 4 krad region at –33ºC. Windowed data is shown in red and green (non-widowed in blue and brown).

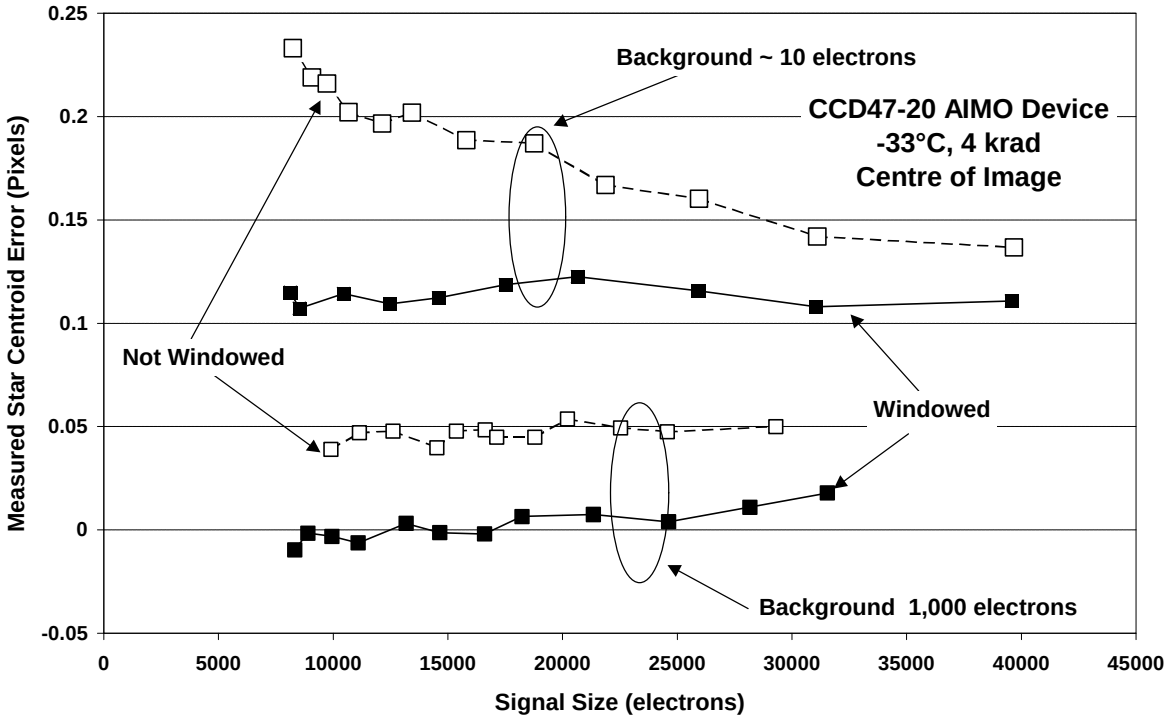

Figure 7.4-9 Centroid errors as a function of signal size for constant background, windowed and non-windowed (centre of image)

7.4.4 Further Results

Further insight into the effect of CTI on centroid positions can be gained by considering the relation between centroid error and charge loss. Both these quantities will increase with CTI. Figure 7.4-10 shows results for both device types, in non-windowed mode with the star at the bottom (CCD02) and centre (CCD47-20) of the image. The data was obtained for a variety of signals, backgrounds and positions within a pixel but there is a tendency for the results to lie on a 'universal' curve.

It is seen that the centroid error increases approximately linearly with the fractional charge loss until the error reaches ~ 0.4 pixels. At this point the brightest pixel is no longer the true brightest pixel but shifts to the pixel behind it and the centroid error increases dramatically. Also shown are the results from the Excel™ simulation. These agree reasonably well but, as noted above, the model does not correctly model the effects of signal dependent CTI and trap filling by preceding charge packets, hence the centroid error tends to be under-estimated.

Also shown in the figure are results for the CCD47-20 in windowed mode. This is the same data as given in figure 7.4.9 for the low background case but re-plotted in terms of charge loss. There is a spread in the charge loss values because of the spread in signal size but the centroid error stays fairly constant. There is a different behaviour in windowed mode because the charge loss for a given CTI will be similar to that in non-windowed mode but the centroid error is less because the charge which is lost (trapped) is spread over more pixels and so does not distort the star profile as much.

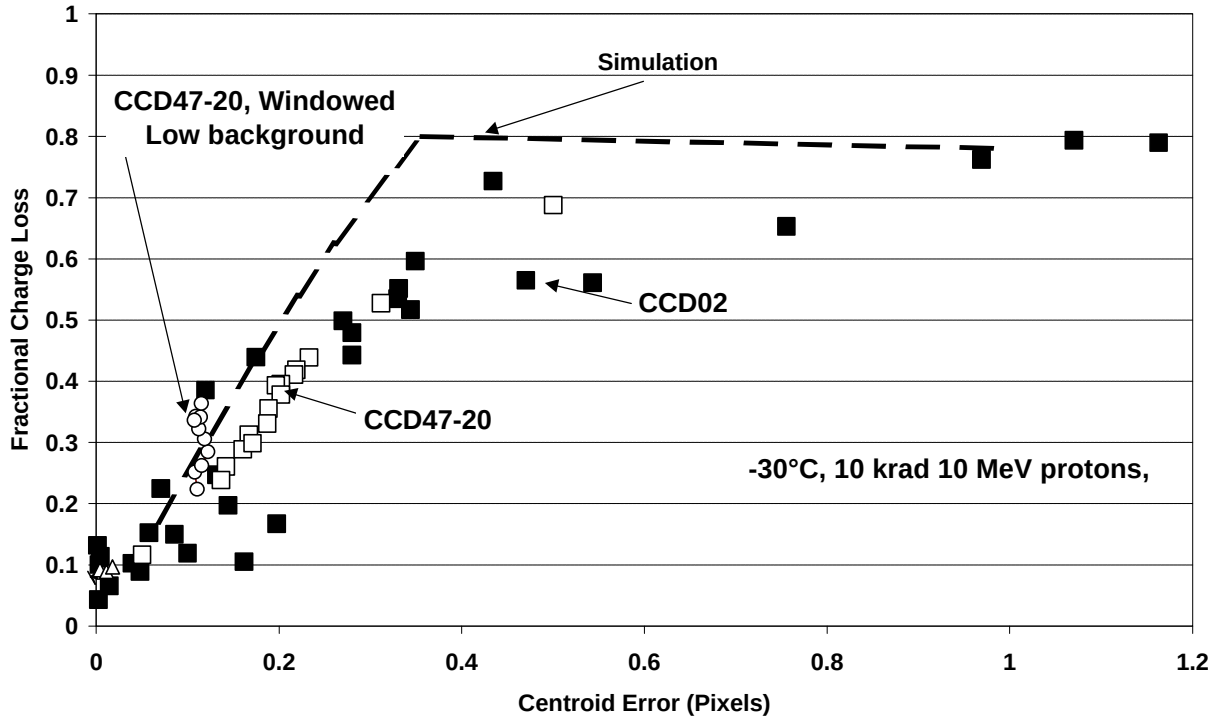

Figure 7.4-10 Fractional charge loss versus centroid error for the CCD02 and the CCD47-20 compared with spreadsheet simulations.

It is tempting to think that there may be an alternative to the centre-of-gravity centroiding algorithm (equation 7.4-1) which will give lower centroid errors. Some examples of algorithms which fit to symmetrical functions have been given by Endo et al[9] :

Gaussian:

$$\text{Centroid position (pixels)} = \frac{\ln(A) - \ln(C)}{2[\ln(A) - 2\ln(B) + \ln(C)]} \qquad (7.4\text{-}2)$$

Lorentzian

$$\text{Centroid position (pixels)} = \frac{(1/A) - (1/C)}{2[(1/A) - (2/B) + (1/C)]} \qquad (7.4\text{-}3)$$

Parabolic

$$\text{Centroid position (pixels)} = \frac{A - C}{2(A - 2B + C)]} \qquad (7.4\text{-}4)$$

Where, as before, A, B and C are the summed signals (with background subtracted) for the three rows of three pixels.

A brief investigation did not show any advantage to using any of these algorithms.

Another alternative is to use an asymmetrical function, such as the lognormal distribution[10] or to truncate any of the above functions so as to make them unsymmetrical. Unfortunately however, the spot profiles are such that it is difficult to differentiate between a spot which has been shifted due to CTI and one which is shifted due to a simple change in position (field angle). This is illustrated in figure 7.4-11. Even with CTI degradation the spot images still look spot like within the 3 x 3 matrix of pixels used for centroid measurements. The CTI does produce a trail of charge but this is difficult to distinguish. There is the possibility to take a larger matrix (4 x 4 or 5 x 5 pixels) but this will introduce errors due to noise and inter-pixel nonuniformities. Once it was realised that CTI degraded images do not give significantly different spot profiles, attempts to improve on the centroid algorithm were stopped.

[9] I. Endo, T, Kawamoto, T. Ohsugi, T. Taniguchi and T. Takeshita, 'Systematic shifts of evaluated charge centroid for the cathode read-out multiwire proportional counter', vol. 188 pp 51-58, 1981

[10] N. L. Johnson, S. Kotz and N. Balakrishnan, 'Continuous Univariate Distributions', Wiley-Interscience, 1994

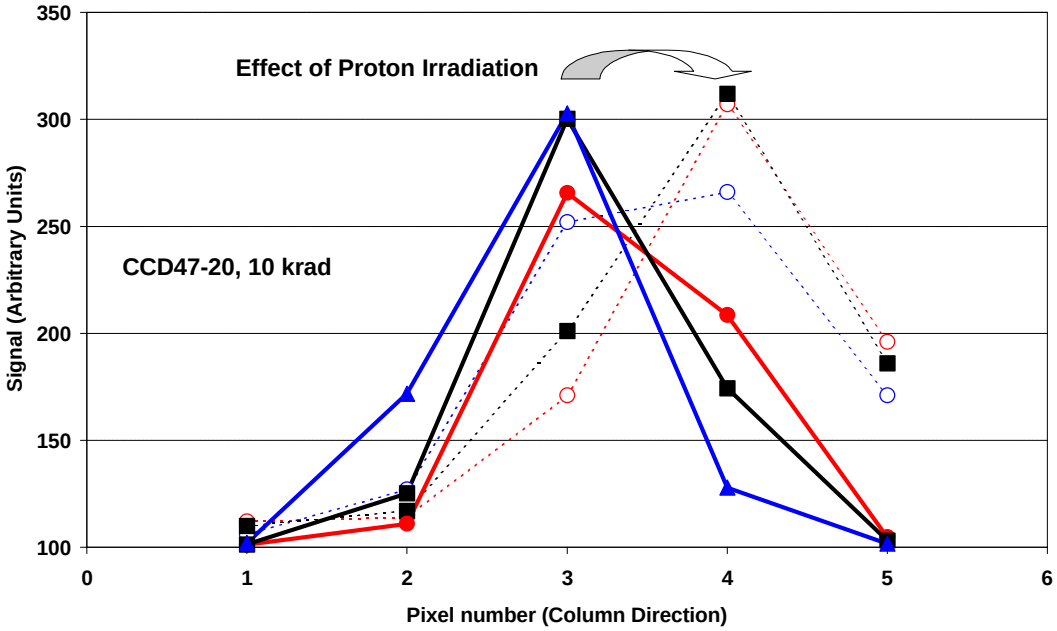

Figure 7.4-11 Spot profiles (in the column direction and normalised to the same peak amplitude) before and after proton irradiation

8. SUGGESTIONS FOR FUTURE WORK

In this section, suggestions are given for future work in each of the three areas: ADCs, active pixel sensors and CCDs.

8.1 ADCS

There is a continuing demand for precision (>12 bit) high speed, low power ADCs and evaluation of new devices is likely to be required as they become available. In particular, high speed 16-bit ADCs (such as the SPT8100 5 MHz ADC, or the 1 Hz MAXIM, MAXI200) are likely to need both total dose and single event characterisation.

8.2 ACTIVE PIXEL SENSORS

The next version of the ASCoSS device is being developed and will require a radiation evaluation when it is available (expected mid 2000). A full evaluation will, as in this study, entail latch-up, total dose and proton tests. Device responsivity will require careful measurement in order to ascertain if the changes seen in this study occur in the new version.

8.3 CCDS

Although CCDs have been extensively studied over the past few years there are still many open questions:

a) Dependence of trap concentrations on proton energy
b) Modelling of CTI at low signal levels. Recent results from other projects suggest that the CTI can be improved at low signal levels. This seems to be very dependent on the effectiveness of the 'fat zero' (which is temperature dependent). Preliminary modelling by Marconi Applied Technologies (EEV) suggests that the effect can be explained but detailed work has not yet been performed.
c) Total dose effects on new (e.g. two stage) output amplifiers
d) Dark current histograms for small pixel devices and versus proton energy
e) RTS effects (particularly at low temperatures and for small pixel devices)

APPENDIX 1 ASCOSS SENSOR PIN CONFIGURATION

PIN	Name	Comment
1	NC	Do not connect
2	NC	Do not connect
3	NC	Do not connect
4	NC	Do not connect
5	NC	Do not connect
6	NC	Do not connect
7	NC	Do not connect
8	NC	Do not connect
9	nbias	output column source follower bias. connect with 10-100 kOhm to vdd
10	clk_xrd	clock x read
11	v_ref	reference voltage for column amplifiers, ~1.2 Volt
12	vdd	supply voltage sensor
13	gnd	ground sensor
14	clk_yrd	clock y read
15	pbias1	column amplifier bias. connect with 1 MOhm to gnd
16	pbias2	column source follower bias. connect with 1 MOhm to gnd
17	knbias	column source follower bias. connect with 1 MOhm to vdd
18	\sync_xrd\	Sync x read shift register (active low)
19	\s2\	control signal column amplifier (low during row calibration)
20	\sync_yrd\	sync y reset shift register (active low)
21	NC	Do not connect
22	NC	Do not connect
23	NC	Do not connect
24	NC	Do not connect
25	NC	Do not connect
26	NC	Do not connect
27	NC	Do not connect
28	NC	Do not connect
29	NC	Do not connect
30	NC	Do not connect
31	NC	Do not connect
32	vdd	supply voltage sensor
33	gnd	ground sensor
34	reset_r	reset right hand side of imager. to be connected to reset_l
35	reset_select	selection reset
36	NC	Do not connect
37	vdd_array	analog supply of pixel array. connect to vdd
38	ab_gnd	anti blooming ground. connect to 0 .. 1 Volt
39	d0	output bit ADC (MSB)
40	d1	
41	d2	
42	d3	
43	d4	
44	d5	
45	d6	
46	d7	output bit ADC (LSB)
47	\e_adc\	enable ADC (active low)
48	mpx	multiplex ADC output. connect to vdd
49	\clk_adc\	clock ADC. latch on negative edge
50	reset_l	reset left hand side of imager. to be connected to reset_r
51	gnd	ground sensor

52	vdd	supply voltage sensor
53	vdd_dig_adc	digital supply of ADC
54	Vdd_ana_adc	analog supply of ADC
55	gnd_dig_adc	digital ground of ADC
56	vh_adc	high reference voltage of ADC. connect through a resistor of 2 kOhm to vdd. Decouple to gnd
57	gnd_ana_adc	analog ground of ADC
58	vm_adc	mid reference voltage of ADC. Decouple to vdd (C > 1uF)
59	rd_adc	bias digital part of ADC. connect through a resistor of 10-50 kOhm to gnd_dig_adc
60	ra_adc	bias analog part of ADC. connect through a resistor of 100 kOhm to vdd_ana_adc
61	vl_adc	low reference voltage of ADC. connect through a resistor of 4 kOhm to gnd. Decouple to vdd
62	adc_in	input ADC (2Volt < adc_in < 4Volt)
63	NC	Do not connect
64	obias	bias output amplifier. connect with 10-50 kOhm to gnd
65	a_gain0	output amplifier gain selection bit
66	a_gain1	output amplifier gain selection bit
67	a_pout	analog output of sensor
68	vdd	supply voltage sensor
69	gnd	ground sensor
70	amux0	input selection of output amplifier. 0 = sensor, 1 = a_in2
71	\shx\	sample and hold output signal of sensor. (connect amux0 to gnd, then 0 = track, 1 = hold)
72	dcv	reference voltage of output amplifier. ~ 1Volt (adjustable for each sensor!)
73	a_in2	second analog input of output amplifier
74	NC	Do not connect
75	gnd	ground sensor
76	vdd	supply voltage sensor
77	clk_yrst	clock y reset
78	\sync_yrst\	sync y reset (active low)
79	\shcol\	column sample and hold. (during row calibration, 1=hold, 0=track)
80	\s3\	control signal column amplifier (low during row readout)
81	s1	control signal column amplifier (minimal 1 us high during row calibration)
82	NC	Do not connect
83	NC	Do not connect
84	NC	Do not connect

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