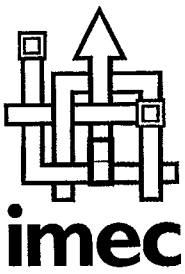

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Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials

Literature Study on Radiation Effects in Cryogenic Electronics

Deliverable D1

C. Claeys and E. Simoen

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Abstract

This report constitutes the Deliverable D1 of Work Order 1938/96/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials". It gives a critical overview of an extensive literature search in the field. First, attention is given to fundamental aspects related to the cryogenic operation of silicon-based electronics. Subsequently, the radiation aspects of cryogenic electronics are studied. Attention is given to both ionization and displacement damage, with special emphasis on the requirements for cryogenic irradiation testing. The outcome of the literature study is used to draw some general conclusions, which are essential for the definition of a radiation test plan. The proposed irradiation plan for the first phase of this Work Order is given in the last section.

Chapter 1

INTRODUCTION

This introduction first points out the importance of cryogenic electronics for space applications in order to justify the need for radiation studies at cryogenic temperatures. Some typical examples are discussed, taking into account the future missions scheduled by ESA. Next the overall outline of the report is given.

1.1. Application of Cryogenic Electronics in Space

The application of cryogenic electronic integrated circuitry in space is mainly related to the cryogenic preamplifiers for different types of radiation and particle detectors and in particular for large arrays of such type of detectors. In order to realise large arrays of detectors the preamplifiers and associated multiplexing electronics can not be outside the dewar with the detector elements, rather they will have to be brought as close as possible to the detector array for limitations of noise, crosstalk and number of feedtroughs. In particular applications cryogenic electronics is also used with single element detectors. In that case the low-noise performance is the driving force. This implies that this electronic circuitry should be operational at temparatures equal or close to the operational temperature of the detectors.

Detectors operated at cryogenic temperatures can be found in a lot op space applications, but mainly in scientific missions. These detectors cover a large part of the electromagnetic spectrum and include also certain types of particle detectors. Below some examples are briefly mentioned.

Superconducting Tunneling Junction (SJT) detectors

ESA has the goal to develop a camera to replace the Faint Object Camera (FOC) on-board the Hubble Space Telescope (HST) by the year 2002-2003. The detector considered at the moment will consist of an array of typically 100 x100 STJs. The detector will be sensitive in the wavelength range from 115 nm to 1000 nm. These detectors have to be operated in the sub-1K region and as a consequence this applies also to the read-out electronics if one chooses for a close integration of the detectors with this electronics.

Bolometer type detectors

Bolometers are thermal radiation sensors. The radiation absorbed by the detector results in an increase of the temperature which is detected by a thermal sensors. In most cases the thermal sensor is a temperature dependent resistor, also called thermistor. The three types op bolometers are metal, semiconductor and superconductor, respectively. It is clear that superconductor bolometers must be cooled to be operational. In general the bolometer performance is improved for all types by cryogenic cooling.
Bolometer properties improve with a high value for the temperature coefficient of resistance, a resistance compatible with low-noise preamplifiers, high radiation absorbance and a low value of the thermal capacitance. By cooling the bolometer to a very low temperature the ultimate detector sensitivity can be orders of magnitude larger than at room temperature. Cooling in general reduces the thermal noise, increases the temperature coefficient of resistance and lowers the thermal capacity.

Bolometer detectors have been used for the detection of Far Infra Red (FIR) and milimeter-wave radiation, x-rays and charged and neutral particles. the ultimate performance required in scientific experiments is reached only at cryogenic temperatures.

Bolometer type mm-wave detector arrays will be used on the Far Infrared Space Telescope (FIRST) planned by ESA for launch around 2005. Cryogenic bolometer detectors are also used in high energy physics for neutrino experiments and high resolution energy measurements of x-rays and charged particles.

Photoconductive Far Infra Red (FIR) detectors

In a photoconductive semiconductor detector the absorption of radiation causes a corresponding conductance or resistance change by a change of free carrier concentration by photo exitation. In order to achieve the best possible performance the thermal generation is to be kept below a certain temperature related to the forbidden energy gap and as a consequence the corresponding detector cut-off wavelength. The longer the cut-off wavelength the lower the corresponding operating temperature. Stressed Ge:Ga detectors with cut-off wavelengths around 200 μm have operating temperatures around 1.6 K. This requires electronics operational at the same temperature. This type of detectors has been used on the ISOPHOT experiment on ISO and is planned to be used also on the FIRST mission.

1.2. Outline of the Report

The second chapter deals with a critical literature study of cryogenic electronics. The fact that silicon has a 1.1 to 1.2 eV band-gap E_G has some important implications for its low temperature behaviour. While in metals, the resistance goes down with cooling - mainly due to a reduction of the phonon population, which causes a reduction of the lattice scattering and an increase of the mobility - the silicon resistivity typically shows a minimum at some intermediate temperatures and increases again when the carrier freeze-out regime is entered. At the same time, the different carrier scattering mechanisms show distinct temperature dependencies, giving rise to a pronounced variation of the bulk and the inversion layer mobility with temperature. The temperature has not only an impact on the average (static) transport properties but also on the low-frequency fluctuations (the noise). Given the fact that most of the cryogenic electronics' applications have a strong analogue nature, this is an important parameter. Finally, the silicon devices not only show low-frequency (LF) fluctuations, but also changes on a longer time-scale, which range from transient and kink phenomena up to long-term operation instabilities, which can be related to hot-carrier degradation or irradiation. Another issue at cryogenic temperatures is that the device operating temperature can differ significantly from the ambient temperature, due to the occurrence of self-heating. Beside a theoretical discussion of some fundamental aspects, this chapter gives attention to the differences in device performance. The latter is treated in view of the selected device technology.

The third chapter discusses radiation effects on the cryogenic operation of silicon devices. With respect to performance degradation, the space radiation environment can distinguish roughly between ionization damage, displacement damage and single particle (or event) effects, which may have a transient (temporary) or a more permanent (hard) nature. This results in a number of degradation effects, like charge trapping, the creation of interface traps at the Si-SiO_2 interface, a reduction of the mobility, single event upset (SEU) and latch-up (SEL) in CMOS. The main displacement damage degradation effects are an increased resistivity and even type inversion for high-resistivity Si nuclear-radiation detector material, increased dark (leakage) current in junction devices and CCDs, reduced minority carrier lifetime in bipolar devices (solar cells), etc. These different aspects are addressed, especially from a cryogenic operation viewpoint. The main goal of this chapter is to investigate the need for performing radiation experiments at cryogenic temperatures.

The fourth chapter summarises the most important conclusions resulting from the two previous chapters dealing with a critical literature study. Important guidelines are given, which should be taken into account during the definition of the irradiation test plan for cryogenic space applications.

A preliminary irradiation testing plan for the first phase of this Work Order, including the type of devices that will be studied and the envisaged irradiation rounds, is given in the last chapter. This test plan has to be considered as preliminary and will be updated whenever appropriate. The latter surely will occur in case that it would become possible to perform irradiations at cryogenic temperatures. Cryogenic irradiation tests are more important for total dose compared to bulk damage effects.

In order to optimise the future use of the critical literature review, an extensive reference list has been included.

Chapter 2

LITERATURE STUDY CRYOGENIC ELECTRONICS

2.1 Introduction

This chapter is based on a critical literature search concerning the operation behavior of cryogenic silicon-based electronics. The overall goal is to obtain a better insight into the underlying physics of silicon devices operating at cryogenic temperatures in order to investigate the impact of the operation of such cryogenic circuits in a radiation environment as encountered during space missions.

The theoretical treatment starts with a review of some basic device properties such as carrier freeze-out, Fermi level effects and mobility behaviour. A distinction will be made between the different types of devices. For many space applications, the low frequency noise has to be optimised. Therefore the low temperature noise behaviour is reviewed for a variety of silicon devices. The same is done for device reliability and stability aspects. A last paragraph briefly discusses self-heating effects, which have an influence on the real temperature the devices are operating.

2.2. Basic Device Properties

This section discusses first of all carrier freeze-out and Fermi levels effects, both for non-degenerately and degenerately doped silicon. The different types of devices such as e.g. resistors, diodes, Bipolar Junction Transistors (BJTs), Junction Field Effect Transistors (JFETs) and Charge Coupled Devices (CCDs) are systematically discussed. Subsequently, the mobility behaviour at cryogenic temperatures is reviewed, including a discussion of the bulk mobility, velocity saturation and inversion layer effects impacting the surface mobility

2.2.1. Carrier Freeze-out and Fermi Level Effects.

2.2.1.1 Non-degenerately-doped silicon.

Carrier freeze-out in a non-degenerately doped semiconductor ($n<<10^{18}$ cm^{-3}) is caused by the shift of the equilibrium Fermi level with lower temperature towards one of the band-edges. For an n-type material, doped with a shallow donor with ground-state energy E_D below the conduction band E_C, a homogeneous concentration $N_D >>$ the intrinsic carrier concentration n_i and a degeneracy factor g=2, the charge balance or neutrality equation gives a free electron density:

$$n = \frac{N_D}{1 + 2\exp\left(\frac{E_D - E_F}{kT}\right)} \qquad (1)$$

with k Boltzmann's constant. Equation (1) shows that for high temperature, where $E_D >> E_F$, $n \approx N_D$ and all donors are ionised (positively charged). For low temperature, E_F approaches E_D (or becomes even higher) so that $n \approx 0$ and all donors are occupied by their electrons. The corresponding material conductivity, given by:

$$\sigma = q\, n\, \mu \qquad (2)$$

becomes very small, even if the mobility μ increases upon cooling.

Similar considerations hold for the thermal carrier generation across the bandgap, or from a near mid-gap deep level. In that case, quite often the Boltzmann approximation can be used, resulting in the following type of equation:

$$n_i = \sqrt{N_C N_V}\ \exp(-\frac{E_G}{2kT}) \qquad (3)$$

For carrier generation from a deep level with energy E_T, a similar temperature-dependence exists, whereby $E_G/2$ is replaced by E_T and the product of the effective density of states for the conduction and valence band is substituted by N_T^2, the square of the deep-level concentration.

An important remark is that for a non-equilibrium region, characterised by a change in the (quasi)-Fermi level potential (i.e. a p-n junction) the freeze-out concept is not valid. In other words: in the depletion region of a reverse biased junction, the donors (acceptors) will be fully ionised even at deep cryogenic temperature (liquid-helium temperatures -LHT).

The occurrence of freeze-out and of the change of the Fermi energy with temperature in the neutral semiconductor region has some important consequences for the device operation. The following effects play:

MOSFETs

The most direct effect of freeze-out on a MOSFET is an increase of the threshold voltage V_T, defined by:

$$V_T = \frac{E_G}{2} - \frac{qN_{ox}t_{ox}}{\varepsilon_{ox}} + \frac{\phi_B}{2} + \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si} N_A (\phi_B + V_{BS})} \qquad (4)$$

for an enhancement mode n-MOSFET. Hereby is q the elementary charge, N_{ox} the fixed oxide charge density, t_{ox} the gate oxide thickness and ε_{ox} the permittivity of the oxide. In eq. (4) N_A is the substrate (p-well) doping density and V_{BS} the substrate-to-source potential. It should be remarked here that since the last term in eq. (4) corresponds to the depletion region term in the substrate, the full (electrical) concentration applies in this case and no freeze-out needs to be considered here. Even if thermal ionization at LHT may be very slow, other electric field assisted mechanisms like the Poole-Frenkel effect can cause ionization, albeit with large time constants and thus generating a slow transient response to a bias change (see section 2.4).

The strongest temperature dependence stems from the inversion potential ϕ_B, i.e. the surface Fermi level at the point of channel inversion approximately given by:

$$\phi_B = 2\phi_F + \eta_i\, kT \qquad (5)$$

with η_i an empirical factor and ϕ_F the Fermi potential in the neutral substrate referred to the intrinsic Fermi level ϕ_i. $q\phi_F$ is defined by eq. (1). The latter can be solved from eq. (1), resulting for a p-type substrate in:

$$\phi_F = \frac{kT}{q}\ \ln\{\frac{2N_A}{n_i}\frac{1}{1 + \sqrt{1 + 4\, g_A \frac{N_A}{n_i}\exp(\frac{E_A - E_F}{kT})}}\} \qquad (6)$$

with g_A the degeneracy factor of the acceptor level (=4). A more detailed description of the underlying theory can be found in the literature [1-2]. An example of the temperature variation of V_T for Silicon-on-Insulator (SOI) partially depleted (PD) and fully depleted (FD) n-MOSFETs is shown in Fig. 1 [3]. Both for n- and p-MOSFETs carrier freeze-out in the substrate results in a gradual increase of V_T. In principle, the higher the substrate (well) concentration the larger the fraction which becomes deactivated at a certain temperature. This implies that the freeze-out effect would become more pronounced for down-scaled technologies. Looking at eq. (4), one can see a compensating effect by the gate oxide thickness reduction, for the depletion term. However, another related effect which should be taken into account for submicron MOSFETs is the short-channel effect (SCE). The latter describes the impact of the lateral field on the threshold voltage for short-channel transistors. Low temperature operation slightly increases the SCE, as evidenced by Fig. 2 [4], although it can be described by the standard room temperature models.

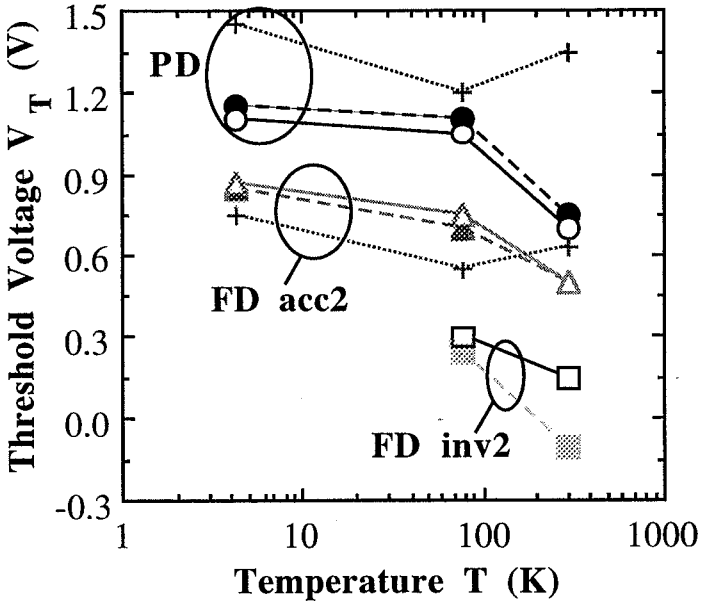

Fig. 1: Threshold voltage as a function of T for a PD and a FD 0.5 μmx20 μm SOI n-MOSFET. Full lines represent theoretical estimates; dashed lines TC extracted data and dotted lines extrapolated V_Ts. FD acc2 corresponds to the case with the back-gate in accumulation; FD inv2 to the case with the back-gate inverted.

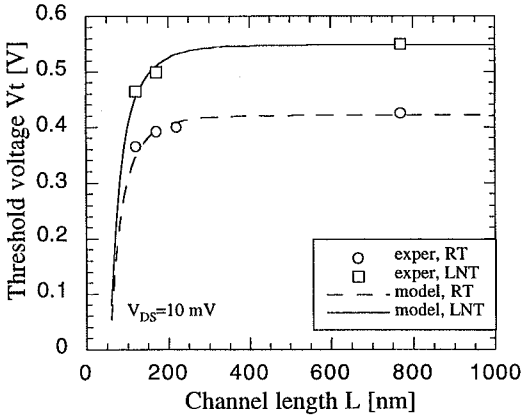

Fig. 2: Comparison between the SCE model and the experimental V_T data at two different temperatures, i.e. 300 K (room temperature - RT) and 77 K (LNT).

A final short-channel threshold voltage effect to be considered is the so-called Drain-Induced-Barrier-Lowering (DIBL), occurring for larger drain biases V_{DS}. Low temperature studies have revealed that the DIBL effect improves at 77 K (liquid nitrogen temperature - LNT) [5], mainly due to the increase of the subthreshold slope upon cooling [6].

Radiation has a pronounced effect on the threshold voltage, mainly through the creation of ionization damage in the gate oxide, which increases the fixed oxide charge (qN_{ox})contribution to V_T and the interface state related contribution. The primary effect is to reduce V_T for n-MOSFETs, as predominantly positive charge (trapped holes) is induced in the gate oxide by irradiation, while the threshold voltage becomes more negative (increases in absolute value) for exposed p-MOSFETs. The physics and impact of low-temperature operation is discussed in more detail in chapter 3.

In modern submicron MOSFETs, the series resistance R_{SD} associated with the Lowly Doped Drain (LDD) region in Fig. 3 and with the n^+ source/drain regions and contact resistances is no longer negligible with respect to the channel resistance R_{chan}. In addition, cooling generally increases R_{SD}, as shown in Fig. 4 for 0.7 μm CMOS n-MOSFETs [3].

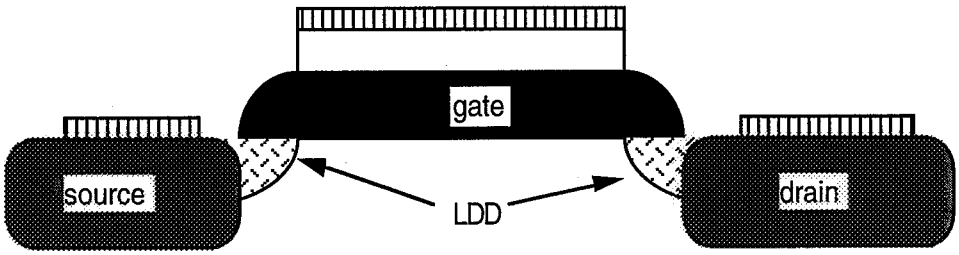

Fig. 3: Schematically representation of a submicron MOSFET.

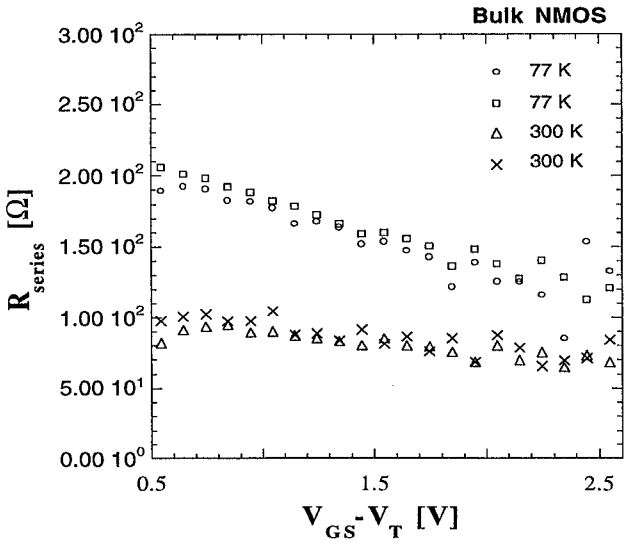

Fig. 4: Extracted R_{SD} as a function of the gate overdrive voltage at 300 K and 77 K, for an array of n-MOSFETs fabricated in a 0.7 μm CMOS technology.

It is believed that this increase in R_{SD} is associated with carrier freeze-out in the LDD regions, which are non-degenerately doped. Another effect is that according to Hafez et al. [7], the LDD resistance at cryogenic temperature becomes lateral-field dependent, as shown in Fig. 5. This gives rise to an output conductance $g_d=\partial I_D/\partial V_{DS}$ at cryogenic temperature which increases significantly for LDD MOSFET upon going from the linear region to the saturation region (Fig. 6). As a result, the extraction of the series resistance from the low-temperature linear characteristics, using classical array methods [8], or single-transistor methods [9], becomes quite complex, as discussed in more detail in Refs. 3,4 and 10.

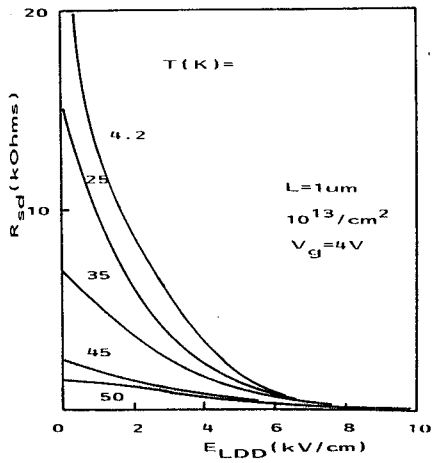

Fig. 5: Variations of the LDD resistance R_{SD} with the electric field E_{LDD} as obtained in LDD MOSFETs operated at various temperatures (after Hafez et al [7]).

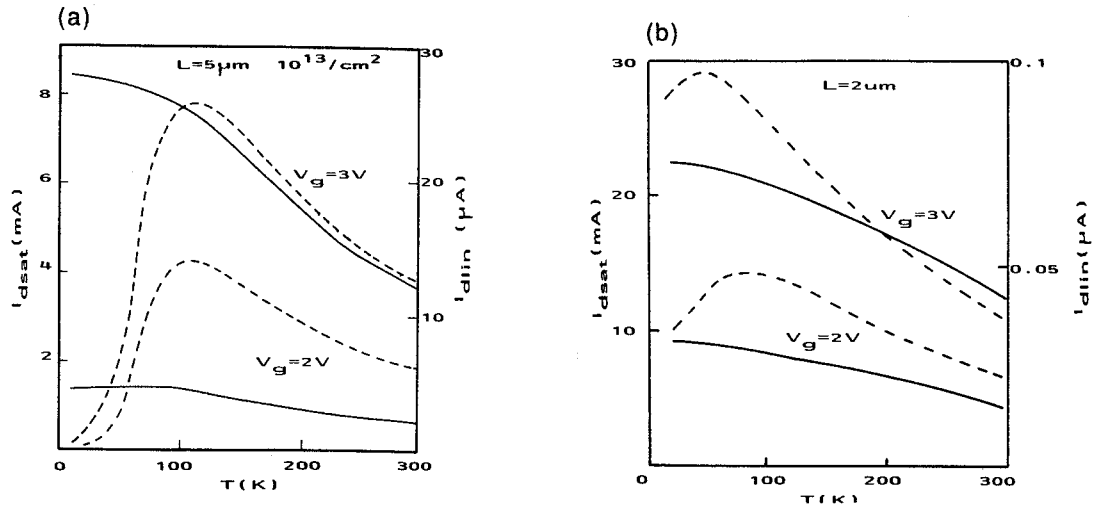

Fig. 6: Variation of the drain current with temperature for the linear (I_{dlin} - dashed line) and the saturation (I_{dsat} - solid line) regime as obtained on MOS devices with (a) and without (b) LDDs (after Hafez et al [7]).

As will be discussed in more detail below, radiation creates positive charge in the spacer oxides covering the LDD regions in Fig. 3, and reduces the series resistance for n-MOSFETs (enhancement of the electron density by the attractive trapped-holes) and degrades R_{SD} for p-MOSFETs. In turn, this seriously degrades the transconductance of low-temperature irradiated (or operated) p-channel devices.

Carrier freeze-out has its strongest impact on the resistance of the Si substrate. Normally doped silicon becomes an insulator in the LHT range, below, say, 40 to 50 K. This is particularly important for sufficiently large V_{DS} to create impact-ionisation near the drain (saturation regime). The created holes (n-MOSFETs) are swept by the field near the drain to the substrate (p-well) contact and give rise to the substrate current I_B. The latter is also considered to be a good measure for the hot-carrier degradation (for the lateral electric drain field). However, due to the large series resistance of the substrate, a considerable potential drop builds up when a substrate current flows. This potential drop is represented in Fig. 7 for a bulk n-MOSFET operated at 20 K and at 300 K [11]. The situation is similar to the case of partially depleted SOI n-MOSFETs, which operate with a floating film. Due to the increase (forward biasing) of the substrate potential V_{BS}, the threshold voltage will be lowered and the injected drain current will increase, giving rise to a so-called kink (Fig. 7). For sufficiently large potential drop, the source-substrate (film) junction will start to conduct (parasitic bipolar action) and extra electrons are injected into the channel. This implies also that only part of the multiplication generated current will be collected by the substrate contact, while a considerable fraction serves as the base current for the source-substrate-drain parasitic npn [12].

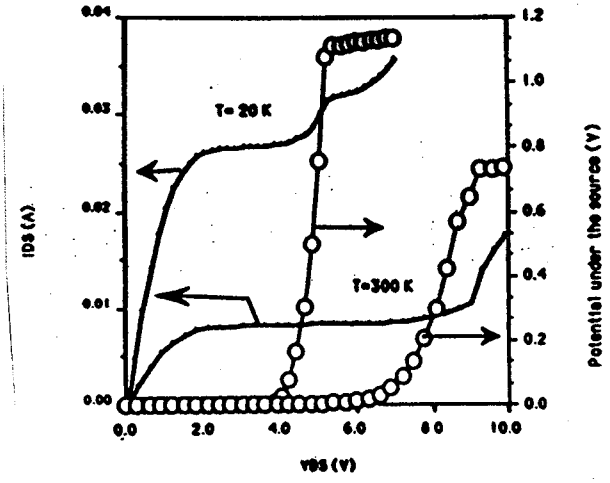

Fig. 7: Measured I_D and potential under the source for T=20 K and T=300 K (after Deferm, Simoen and Claeys [11]).

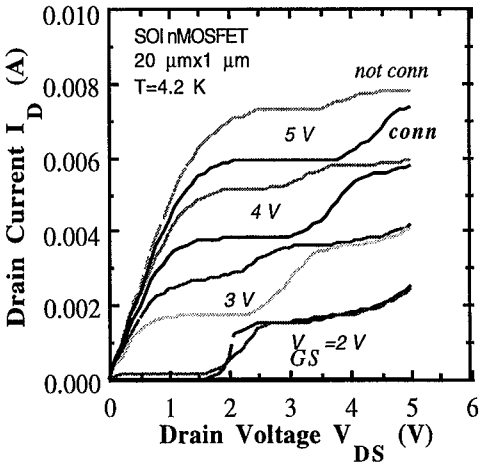

Fig. 8: Output curves of a 20 µmx1 µ partially depleted SOI MOSFET for different V_{GS} and corresponding with floating operation (thin lines) and a grounded film (bold lines) (after Simoen and Claeys [14]).

As can be seen in Fig. 7, the onset of the kink is strongly affected by the temperature and shifts towards larger V_{DS}s, for higher temperatures [13]. The same type of behaviour is found for SOI n-MOSFETs, for the whole temperature range considered [14]. As shown in Fig. 8, grounding the film in SOI does not remove the kink [14-15]. Conversely, the kink is lowered in bulk n-MOSFETs if the substrate is left floating. Using the twin-gate concept in SOI greatly removes the kink effect down to 4.2 K [16]. Little kink effect is observed in cryogenic bulk or SOI p-MOSFETs, in FD SOI devices, in dual-gate structures [17] or in depletion/accumulation mode n^+nn^+ SOI transistors. It has also been reported that the kink effect is reduced upon downscaling the device size [18]. However, pronounced kink effects have been observed in some deep submicron (0.1 μm) devices up to room temperature [19]. Finally, an empirical relationship has been demonstrated between the measured substrate current and the drain current kink (Fig. 9), which can be represented by [14]:

$$I_D = I_{D0} + \Delta I_{Dkink} \tag{7a}$$

$$\Delta I_{Dkink} \sim \sqrt{I_B} \tag{7b}$$

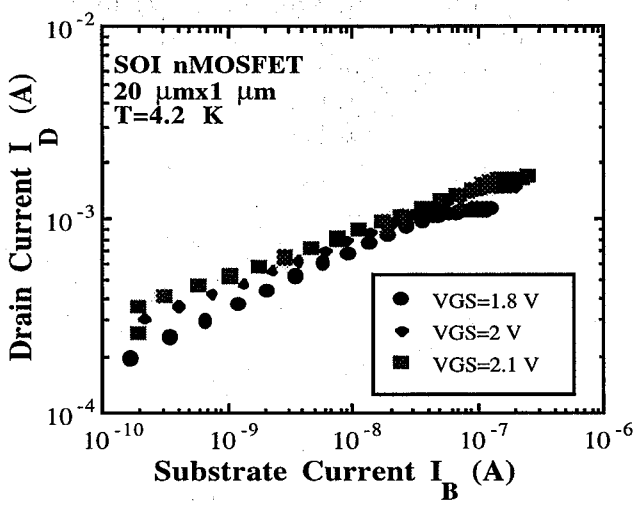

Fig. 9: Drain current versus substrate (film) current in the kink region, for a 20 μmx1 μm PD SOI nMOSFET with grounded body tie and corresponding with different gate voltages (after Simoen and Claeys[14]).

Charge-Coupled Devices

Operating CCDs at low(er) temperature offers some clear advantages. The thermally activated nature of the carrier emission (generation) lowers exponentially the dark current in a buried channel CCD. This improves on the CTI and the related noise. Moreover, lowering the temperature can deactivate a deep-level trap so that it no longer contributes to the CTI. Depending on the type of trapping levels present (their energy level) and on the operation conditions (clock frequency) some operation windows occur, where the CTI is minimum. This is particularly important with respect to hardening against space displacement damage.

However, entering the freeze-out regime (< 100 K) changes the dopant centers in the buried channel (P atoms) into trap levels and enhances significantly the CTI as illustrated in Fig. 10 [20-21], so that for scientific purposes this operation regime is not very promising.

The situation is slightly different for a surface channel CCD operated at low temperature. Since the interface traps show a continuous energy distribution, there will

always be interface states available around the surface Fermi level to interact with signal carriers. Of course, the surface generation current will reduce significantly, since only deep interface states near midgap can be considered as efficient generation centers. These are frozen out just below room temperature. From Fig. 11 it can be deduced that the minimum CTI occurs somewhere around 50 K [22].

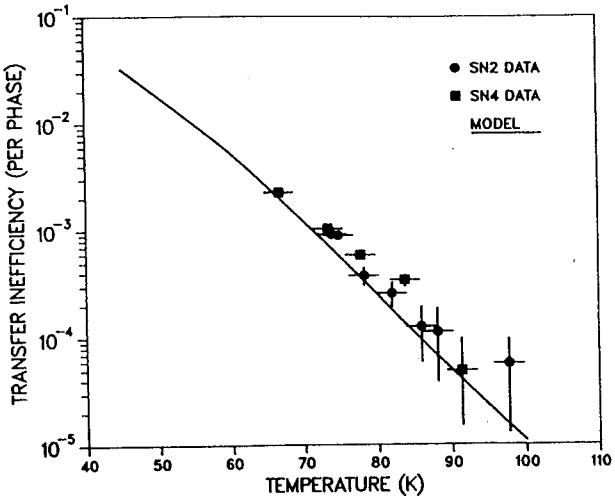

Fig. 10: Simulated dependence of the charge transfer inefficiency for the buried-channel CCD on temperature versus experimental data for two devices (after Banghart el al. [21]).

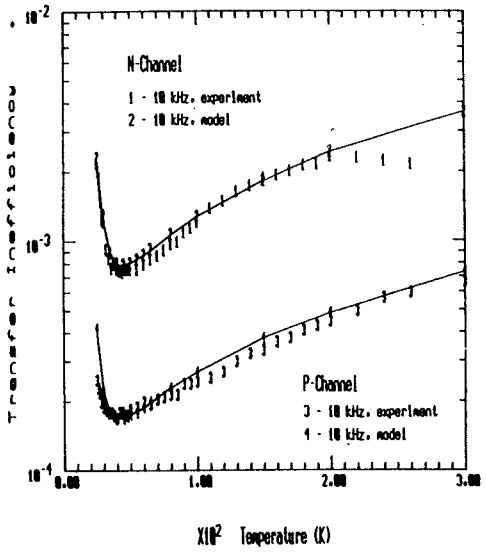

Fig. 11: Comparison between model calculations and experimentally observed CTI for n- and p-channel CCDs at 10-kHz clocking frequency (after Zetterlund and Steckl [22]).

JFETs

JFETs suffer severely from carrier freeze-out in the lowly doped channel. As a result, the transconductance reduces significantly below ≈ 100 K and is small at LHT. An example is shown in Fig. 12 [23]. JFETs are therefore hard to use at deep cryogenic temperatures. Attempts have been made to develop a 4.2 K compatible technology [24]. One of the major points is to increase the channel doping concentration to high values. The obtained free hole concentration (pFETs) versus temperature is shown in Fig. 13, for various channel dopings [24].

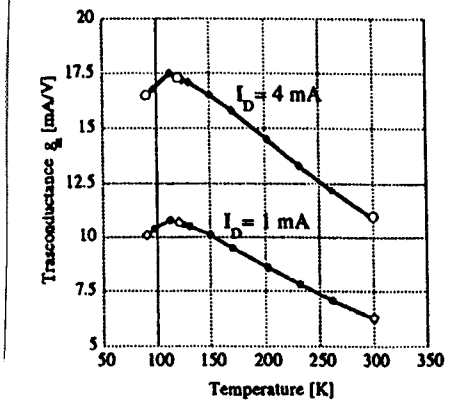

Fig. 12: Temperature behaviour of the transconductance g_m of a JFET (W/L=2500/3) before (white symbols) and after (solid black symbols) a 55 Mrad γ-ray irradiation (after Radeka et al. [23]).

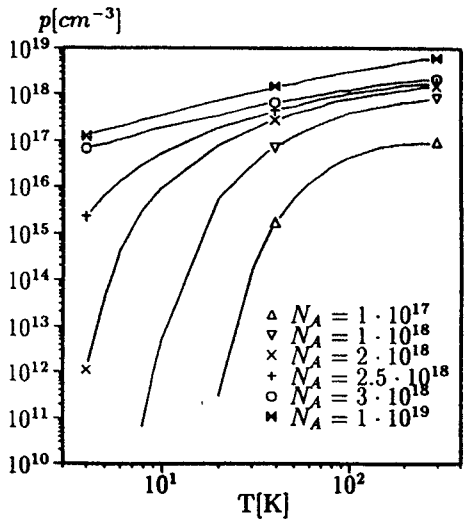

Fig. 13: Ionised dopants as a function of temperature for different acceptor concentrations (after Vollrath [24]).

Diodes and bipolar junction transistors (BJTs)

Since both the intrinsic and the extrinsic carrier generation in the depletion region of a junction diode freeze-out exponentially for lower temperature, the reverse diffusion and generation current drops likewise. Below 0 °C the leakage current of most junctions is almost negligible, except if there is a strong tunneling component, a mechanism which is known to be temperature-independent [25-26].

Another consequence of the freeze-out effect is the increase of the built-in potential of a diode, which is in first approximation given by:

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \qquad (8)$$

with N_A the acceptor concentration on the p-side and N_D the donor concentration on the n-side, respectively. For T--> 0 K the built-in potential should be close to the band-gap, i.e. ≈1 V.

The reduction of the average thermal carrier energy kT on the one hand and the increased potential difference on the other result at low temperature in a larger turn-on voltage for a forward biased diode. This can be inferred from Fig. 7 already, showing the turn-on potential of the source-substrate junction in a MOSFET at 300 K (≈0.3 V) and at 20 K (≈ 1 V). Another example is given in Fig. 14 [27].

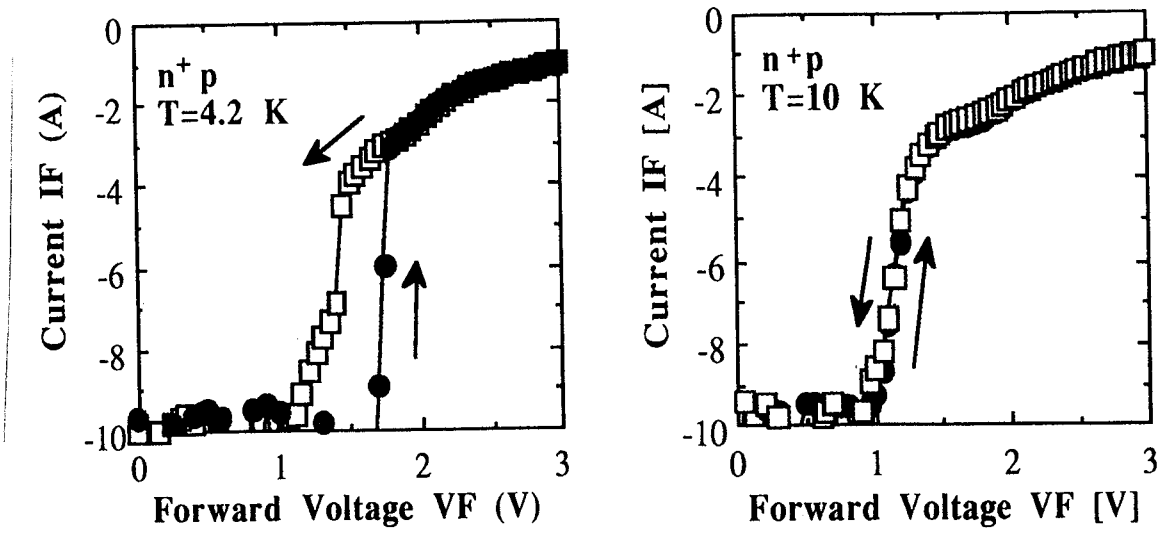

Fig. 14: Forward I-V characteristic of a Si n^+p junction diode fabricated in a 3 μm CMOS technology at 4.2 K (left) and at 10 K (right). The arrows indicate the sweep direction of the voltage (low-high or high-low) (after Simoen et al. [27]).

2.2.1.2. Degenerately-doped silicon.

In degenerately doped material, the ground-state of the doping levels is broadened to a narrow band which overlaps with the conduction or valence band edge. In principle, there will be always free carriers available for conduction (see e.g. Fig. 12). This is the basic reason why a MOSFET is still operating at the lowest temperatures: the n^+ source/drain regions can supply minority (or majority) carriers to flow in the channel.

n^+nn^+ Resistors

When the average thermal energy is dropping, the band-gap narrowing in the highly doped region becomes important. One consequence of this is that an n^+n contact no longer behaves ohmic at LHT but shows a potential barrier approximately equal to the bandgap narrowing in the highly doped region ΔE_G, which electrons have to overcome before being injected in the lowly doped n-region [28]. As a result, the I-V characteristic of a n^+nn^+ region is not linear (ohmic) but shows a threshold behavior, as shown in Fig. 15 [29]. If a gate is applied to such a lateral structure, one can operate the device as an accumulation mode transistor in the LHT range [29-30].

BJT

The bandgap narrowing in the heavily doped emitter region of a BJT is responsible for the current gain (β) degradation at low temperature, since [31-34]:

$$\beta = \exp(-\frac{\Delta E_{Ge}}{kT}) \qquad (9)$$

A typical behaviour in the range 77 K to 300 K is given in Fig. 16 [34], showing a drastic reduction of β for standard metal contacted BJTs. However, using a polysilicon emitter contact greatly improves the current gain at 77 K [31,34] and even at 4.2 K [35]. This opens up perspectives for cryogenic BiCMOS. Another very promising alternative is SiGe base Heterojunction BJTs [36], which operate satisfactorily down to LHT [37]. An example is shown in Fig. 17.

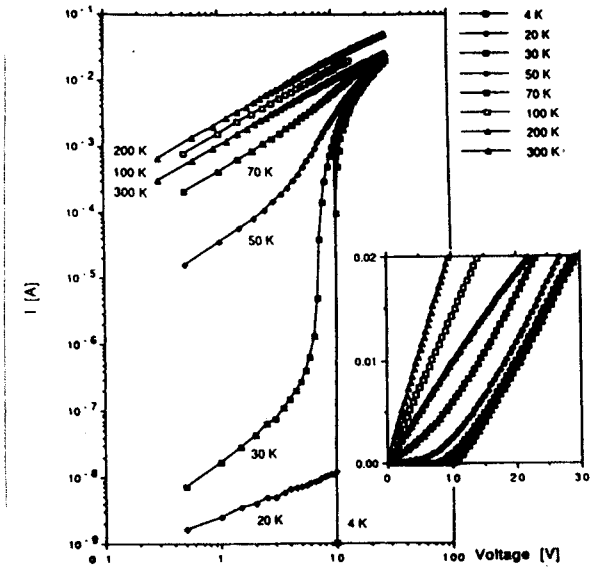

Fig. 15: Experimental I-V characteristic of a 80 μm Si p^+pp^+ resistor for different temperatures (after Simoen et al. [29]).

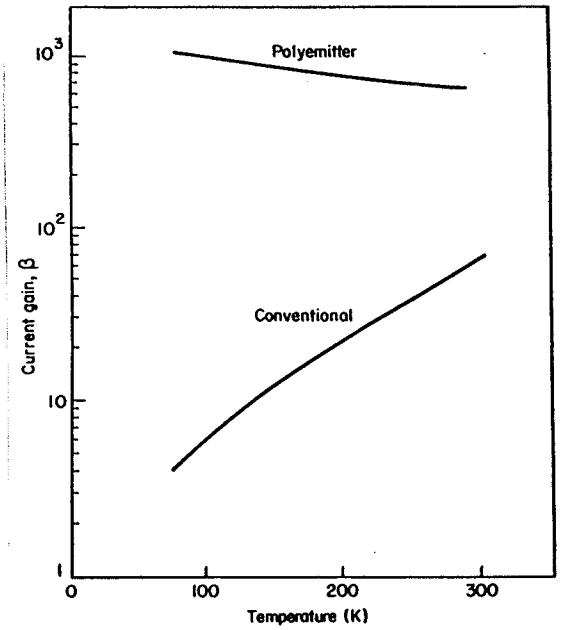

Fig. 16: Current gain, β, in polysilicon emitter BJTs designed for cryogenic operation at I_C=10 μA, compared with similar sized conventional BJTs under similar conditions (after Jayadev et al. [34]).

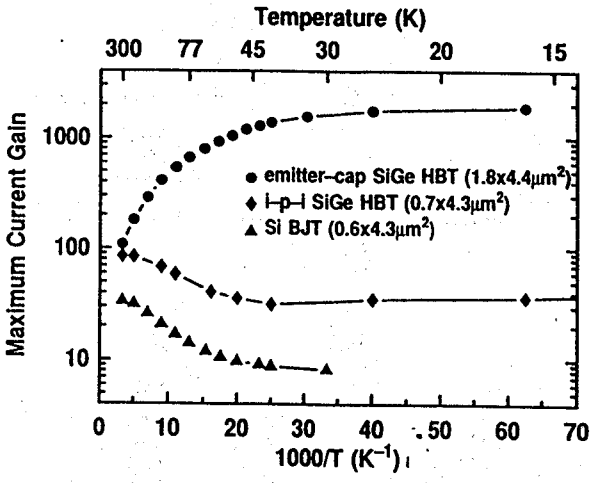

Fig. 17: Maximum current gain as a function of temperature for the emitter-cap SiGe HBT, the i-p-i SiGe HBT and the Si BJT (after Cressler et al.[37]).

One important advantage of the fact that the current gain of a standard BJT is dropping considerably with T is that the parasitic bipolar effects in MOSFETs in general reduce with lower operation temperature. This applies e.g. for the single-transistor subthreshold latch behaviour in SOI devices [38]. Improvement with cooling is also observed with respect to latchup in CMOS [39-40]. As can be derived from Fig. 18, the holding current I_H and the holding voltage I_H increases drastically with cooling to 77 K [41]. However, when entering the freeze-out regime, a drop in I_H (V_H) is noted in Fig. 18, indicating a higher susceptibility to latching. It is believed that the underlying physical mechanisms are quite different in the LHT range compared with the range above 77 K. Important mechanisms contributing to parasitic leakage may be the impurity breakdown of the substrate (well) regions induced by shallow-level impact ionisation (SII) [41].

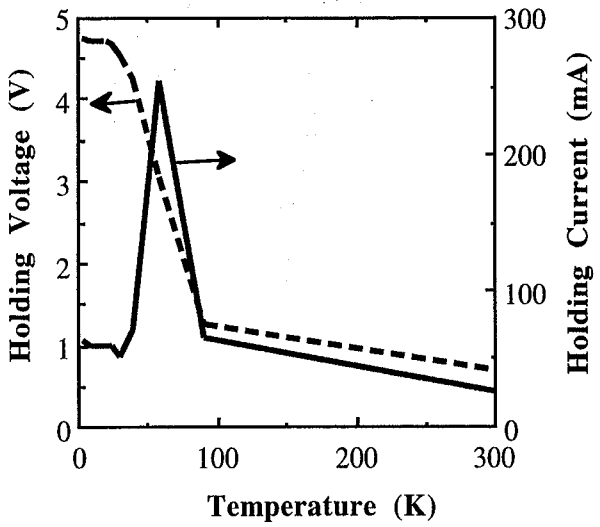

Fig. 18: Temperature dependence of the holding current for a 1.25 μm n-well CMOS technology (after Deferm et al. [41]).

2.2.2. Mobility at Cryogenic Temperature

The carrier mobility is determined by different scattering mechanisms, which show a specific temperature dependence. The total bulk mobility is generally given by Matthiesen's rule according to:

$$\mu^{-1} = \mu_L^{-1} + \mu_C^{-1} + \mu_N^{-1} + \mu_{ee}^{-1} + \ldots \qquad (10)$$

whereby μ_L is the mobility due to lattice (phonon) scattering, μ_C the mobility due to Coulombic or ionised impurity scattering, μ_N the mobility due to neutral center scattering, μ_{ee} the carrier-carrier scattering term, etc. At room temperature, the lattice scattering dominates, resulting in a mobility of the form [42]:

$$\mu_{Ln} = 1430\ \mathrm{cm^2/Vs}\ (\frac{T}{300\ K})^{-2.3}\ \text{(electrons)} \qquad (11a)$$

$$\mu_{Lp} = 480\ \mathrm{cm^2/Vs}\ (\frac{T}{300\ K})^{-2.2}\ \text{(holes)} \qquad (11b)$$

From eqs (11) follows that the mobility increases with lower temperature. However, since the other scattering mechanisms show a not so strong increase with 1/T, they start to dominate in eq. (10). Similar considerations can be developed for the inversion layer mobility in a MOSFET, whereby one should include the surface roughness scattering and scattering at charged interface states, which is given by [43]:

$$\mu = \frac{\mu_{0it}}{1 + \alpha_{it} N_{it}} \qquad (12)$$

with N_{it} the density of interface traps, μ_{0it} the zero N_{it} mobility and α_{it} an interface-state related scattering parameter.

A final parameter of importance is the impact of the electric field on the mobility. For sufficiently large fields, in excess of a few times 10^4 V/cm (n-type) and 10^5 V/cm (p-type) so-called velocity saturation occurs, whereby the carrier velocity saturates at its high-field limit v_{sat}.

2.2.2.1. Bulk mobility and velocity saturation.

The variation of the carrier drift velocity v_{ds} with electric field E_S is given by the following semi-empirical relationship [42]:

$$v_{ds} = \frac{\mu_0 E_S}{[1 + (E_S/E_C)^{\alpha}]^{1/\alpha}} \qquad (13)$$

with μ_0 the low-field mobility, E_C the critical field for velocity saturation. The exponent α is a fitting parameter, generally ranging from 2 to 5. The saturation velocity is next obtained from the critical drift field E_C, since $v_{sat}=\mu_0 E_C$. Both μ_0 and E_C are in principle temperature-dependent, so that v_{sat} increases upon cooling, as shown in Fig. 19 [44].

For deep submicron device structures, whereby the path a carrier has to travel approaches the average mean free path for scattering λ, the transport occurs under non-equilibrium conditions approaching the ballistic transport. In case only a few scattering events take place, so-called velocity overshoot can occur, whereby the carrier velocity v

becomes larger than v_{sat}. The carrier mean free path increases with lower temperature and is quite often represented by:

$$\lambda_{opt} = \lambda_0 \tanh\left(\frac{E_{opt}}{kT}\right) \qquad (14)$$

which is valid if the optical phonon scattering dominates. Hereby is E_{opt} the energy of the optical phonons (≈63 meV) and λ_0 the zero K mean free path. This implies that velocity overshoot in (deep) submicron device structures is more likely to occur at low temperature. Evidence for this in bulk components has been recently observed in the base transport of cooled BJTs [45]. This is a potential benefit of the low temperature operation, offering the possibility to have a larger maximum drive current, due to the velocity overshoot.

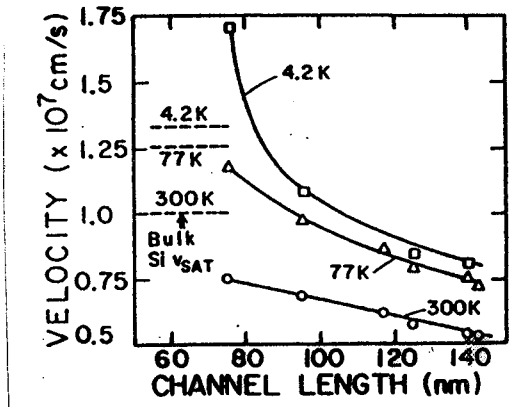

Fig. 19: Calculated average inversion-layer electron velocities of n-MOSFETs with different electrical channel lengths at 300, 77 and 4.2 K (after Chou, Antoniadis and Smith [44]). Also indicated are the bulk electron saturation velocities.

2.2.2.2. Inversion layer mobility and saturation

The occurrence of velocity overshoot in deep submicron inversion layers at low temperature is also illustrated in Fig. 19 [44]. The measured values for the velocity saturation as a function of temperature are represented in Fig. 20, for electrons [46]. For holes, a value of $7\pm1\times10^6$ cm/s has been reported at 77 K [47].

The quantity of interest for a practical MOSFET is the effective mobility μ_{eff} which can be extracted from an input I_D-V_{GS} characteristic in the linear regime. At room temperature, the effective mobility μ_{eff}, which is defined as:

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}} \frac{g_d(V_{GS})}{qN_S(V_{GS})} \approx \frac{L_{eff}}{W_{eff}} \frac{I_D}{C_{ox}(V_{GS}-V_T)V_{DS}} \qquad (15)$$

takes the form:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta^* (V_{GS}-V_T)} \qquad (16)$$

in strong inversion. Hereby is g_d the channel conductance ($\partial I_D/\partial V_{DS}$), N_S the inversion layer carrier surface density, C_{ox} the gate oxide capacitance per unit area and W_{eff}, L_{eff}

the effective device width and length, respectively. The generalised mobility attenuation factor θ^* is given by [50-51]:

$$\theta^* = \theta + \frac{C_{ox} R_{SD} W_{eff} \mu_0}{L_{eff}} \tag{17}$$

and is a measure of the reduction of the effective mobility with increasing normal field. The latter is physically due to the increasing contribution of surface roughness scattering to the carrier mobility. In writing eqs. (15) and (16) it is assumed that the source-drain series resistance is constant with V_{GS}-V_T (non-LDD type of MOSFETs) and that the gate overdrive voltage V_{GS}-V_T >>$I_D R_{SD}/2$.

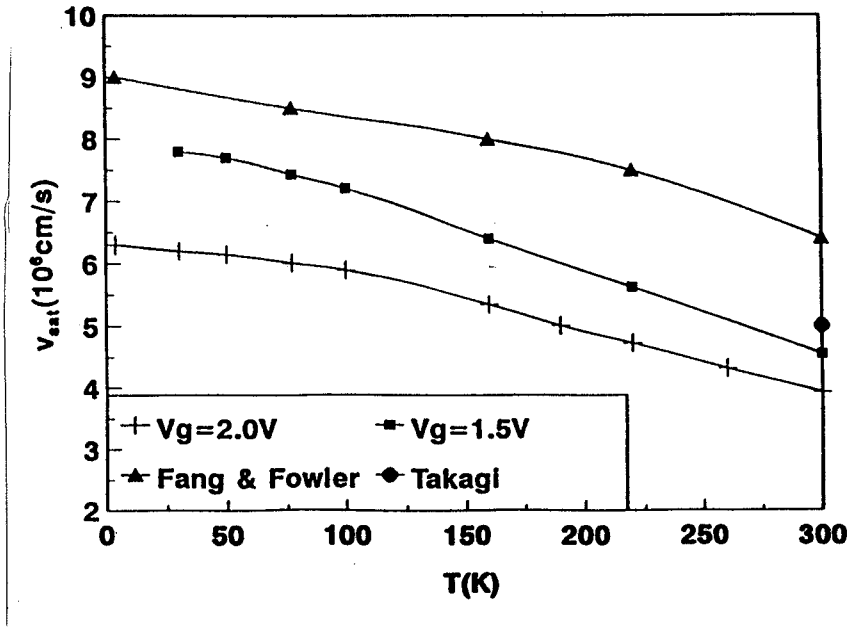

Fig. 20: Variation of the saturation velocity with temperature as obtained for two gate voltages (NMOS gate length L=0.8 μm). Results obtained by Fang and Fowler [48] and Takagi and Toriumi [49] are also shown for comparison (after Rais et al. [46]).

Operation at low temperature has a pronounced impact on the effective mobility, because of the different temperature and transverse field dependence of the respective scattering mechanisms. The situation is schematically represented in Fig. 21 [52]. For sufficiently large transverse electric fields, the effective mobility at room temperature can be represented by the so-called universal mobility law [52-54]. It turns out that if μ_{eff} is represented versus the effective normal electric field, given by:

$$E_{eff} = \frac{\eta Q_i + Q_d}{\varepsilon_{si}} \tag{18}$$

a universal curve is obtained, which is independent of substrate doping density, or substrate bias. Q_i is the inversion layer charge density and Q_d the depletion charge density. Hereby is the empirical factor η=1/2 for electrons and 1/3 for holes, at 300 K. The resulting effective mobility then reads:

$$\mu_{eff} = \frac{\mu_0}{1 + E_{eff}/E_c} \tag{19}$$

with μ_0 the zero field maximum mobility and E_c is a critical electric field.

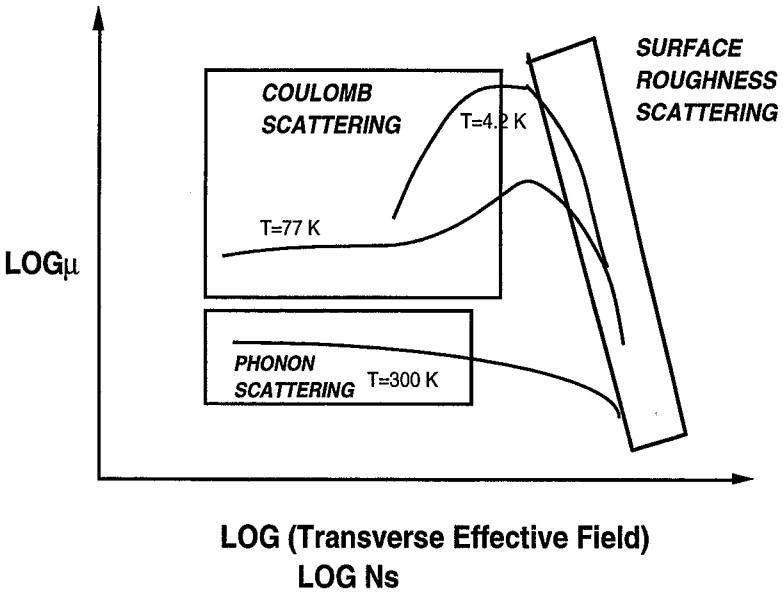

Fig. 21: Schematical representation of the temperature and gate voltage dependence of the inversion layer effective mobility of a MOSFET.

Early low-temperature studies revealed already that the parameter η is not a constant with temperature [52], but lies somewhere between 1/3 and 1, which points towards a change in dominant scattering mechanism upon cooling. More recently, detailed studies have been reported on the substrate and doping density dependence of the low temperature μ_{eff} [51,53-55], both for n- and for p-channel devices (Fig. 22).

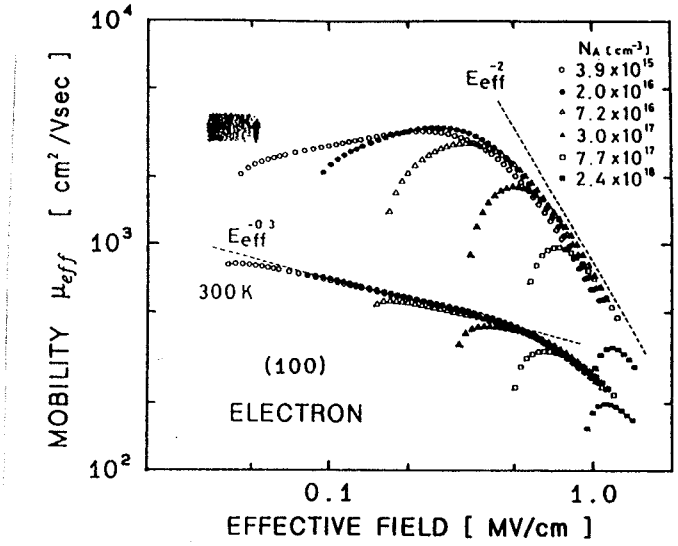

Fig. 22: Electron mobility in inversion layer at 300 K and at 77 K versus effective field E_{eff}, as a function of the substrate acceptor concentration N_A. Here, E_{eff} is defined by eq. (18), with η=1/2 (after Takagi et al. [54]).

In fact, Emrani et al. [50-51] conclude from these studies that the universal field dependence approach represented by eqs. (18) and (19) has no physical meaning at cryogenic temperature and should therefore not be used there.

Given the complex dependence of μ_{eff} with E_{eff} and temperature, extraction of the effective mobility at cryogenic temperature is not straightforward. One general approach has been derived by the Grenoble group [50-51] and is based on the empirical relationship between the function I_D^2/g_m and the gate overdrive voltage V_{GS}-V_T. For sufficiently large V_{GS}-V_T, the following applies:

$$\frac{I_D^2}{g_m} = \beta_m (V_{GS}-V_T)^n \tag{20}$$

whereby the coefficient β_m depends on θ^*. Physically acceptable values for the empirical exponent n are in the range 2 (300 K) to 3 (4.2 K). The effective mobility is shown to be [50-51]:

$$\mu_{eff} = \mu_g \frac{X^{n-2}}{1 + X^{n-1}} \tag{21a}$$

with $X=\theta(V_{GS}-V_T)$ and μ_g proportional to the maximum effective mobility through the relationship:

$$\mu_{max} = \mu_g \frac{(n-2)^{(n-2)/(n-1)}}{(n-1)} \tag{21b}$$

At the same time, the charge threshold voltage V_T at any temperature in the range 4.2 to 300 K can be derived from:

$$V_{Text}^* = V_T + \frac{1}{\theta^*} [\frac{(n-2)}{n}]^{n/(n-1)} \tag{22}$$

whereby θ^* is obtained from:

$$\theta^* = (\frac{n-2}{n})^{1/(n-1)} \frac{1}{V_{GSmax}-V_T} \tag{23}$$

V_{GSmax} is the gate voltage which corresponds to the maximum transconductance g_{mmax}. Since θ^* is a positive number and n becomes larger than 2 upon cooling, from eqs (21) and (22) follows that the linear extrapolated threshold voltage V_{Text} is slightly larger than the actual V_T at low T. In practice, it turns out that the exponent n starts to increase in the range between roughly 100 K and 200 K for n-channel devices, depending on the technology, while for p-MOSFETs, the change from 2 to 3 occurs between 20 K and 4.2 K. Physically speaking, the change of n from 2 to 3 points to a change in the dominant scattering mechanism upon cooling. Likewise, the bell-shaped μ_{eff} behaviour typically found at low temperature can be explained by assuming that μ_{eff} is an explicit function of the inversion charge Q_i, which in its most general form is represented by [51]:

$$\frac{1}{\mu_{eff}} = \frac{A}{Q_i^{n-2}} + BQ_i \tag{24}$$

whereby the coefficient A is a Coulomb scattering parameter and B a surface roughness scattering parameter.

From the obtained results shown in Fig. 23, it can be concluded that the mobility degradation factor increases significantly at cryogenic temperature, pointing to a larger impact of the surface roughness scattering, resulting in a stronger variation of μ_{eff} with E_{eff}. In fact, for large transverse fields, eq. (16) should be modified into [56]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\,(V_{GS}-V_T) + \theta_2\,(V_{GS}-V_T)^2} \qquad (25)$$

accounting for second order effects, e.g. a g_m which can become negative for large gate overdrives. This strongly suggests that at larger gate overdrives, the current-drive gain which is obtained by cooling a MOSFET is counteracted by the stronger transverse field dependence. One exception to this rule is the behaviour of nitrided oxides, which according to Fig. 24 show a larger 77 K transconductance at large $V_{GS}-V_T$ [57].

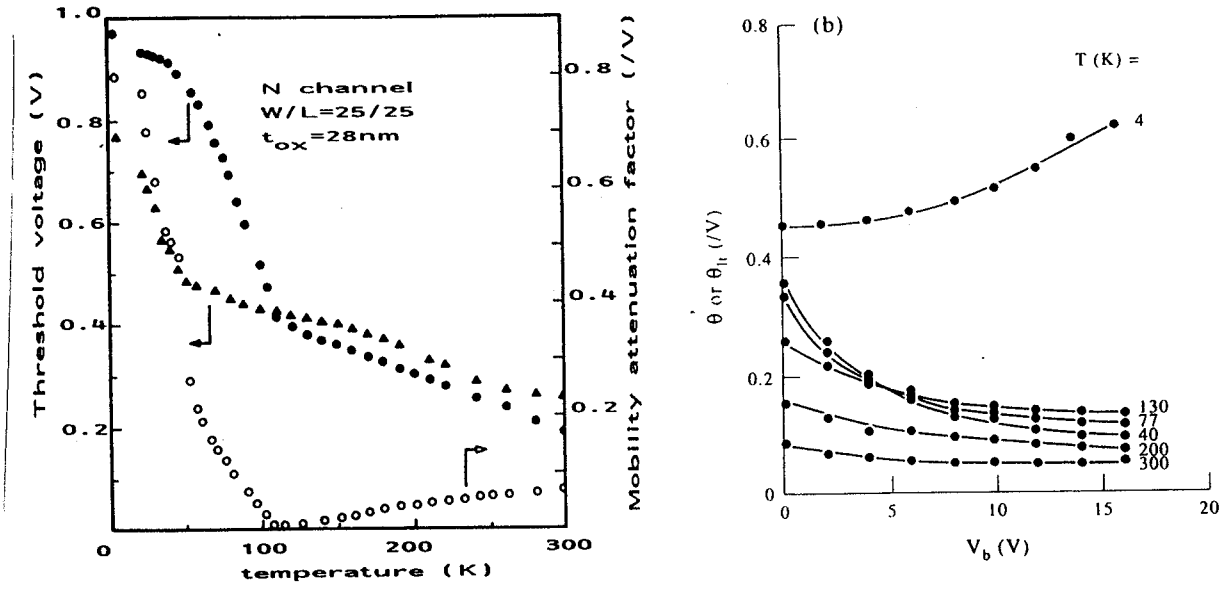

Fig. 23: Typical variations of the threshold voltage V_T (triangles) and V_{Text} (solid circles), and mobility attenuation factor θ (o) with temperature, for n-MOSFETs [50] (a) and variation of θ with substrate bias and temperature as a parameter for p-MOSFETs [51] (b). (After Emrani et al. [50-51]).

The so-called "universal" mobility law is in practice applicable to a broad temperature range, but breaks down if a high series resistance occurs [3,10]. This happens for LDD-type of MOSFETs. However, if R_{SD} can be extracted separately it is possible to apply the same procedure to the corrected channel resistance: $R_{chan}=R_{tot}-R_{SD}$. Using the same approach, the curves of Fig. 25 have been obtained showing again the power law behaviour at 77 K predicted by eq. (20).

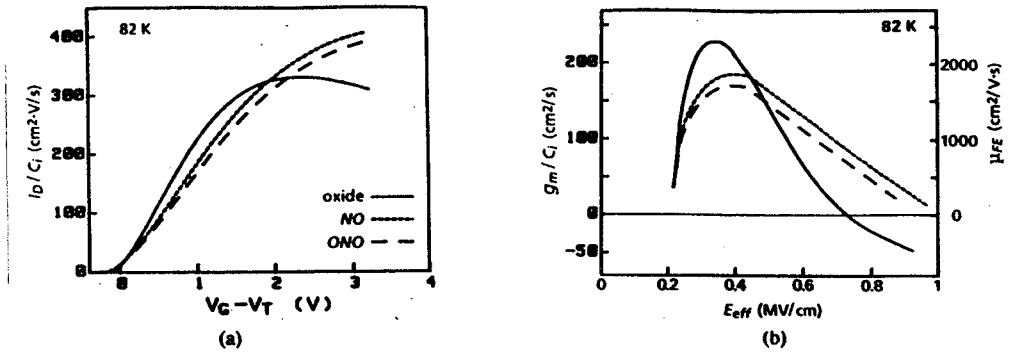

Fig. 24: (a) I_D/C_{ox} versus $V_{GS}-V_T$ and (b) g_m/C_{ox} and field effect mobility μ_{FE} versus E_{eff} at 82 K for the nitrided oxide (NO) and the reoxidized NO (ONO) n-MOSFET. No negative g_m in the high E_{eff} region is found for the NO or ONO devices at 82 K (after Hori and Iwasaki [57]).

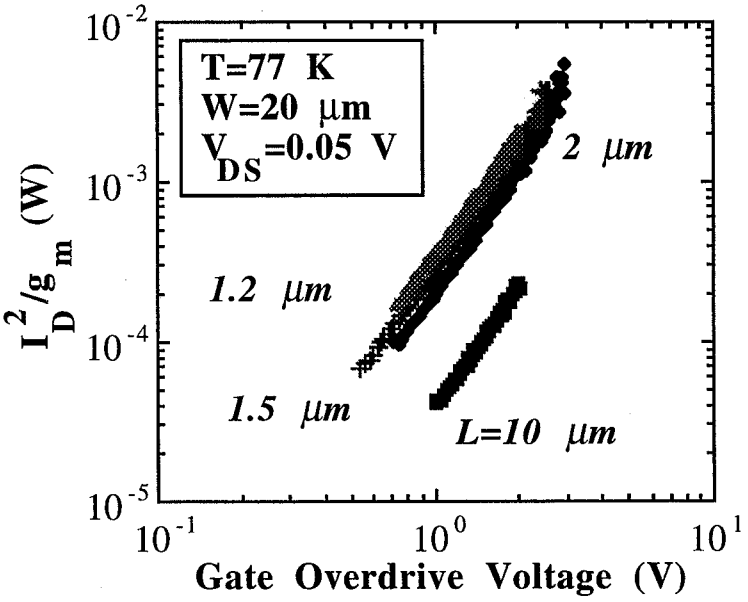

Fig. 25: Universal law for 0.7 μm LDD n-MOSFETs at 77 K, corrected for the gate voltage dependent series resistance (after Simoen and Claeys [10]).

A promising technological alternative is the use of SiGe channel p-MODFETs, which show a significant hole mobility enhancement upon cooling [58-60], as demonstrated in Fig. 26.

It should finally be remarked that radiation in general will result in a lower hole and electron inversion-layer mobility. This degradation will become more pronounced at lower temperature, where the interface-state and oxide charge Coulombic scattering becomes more important (Fig. 21). This can also be inferred from eq. (12).

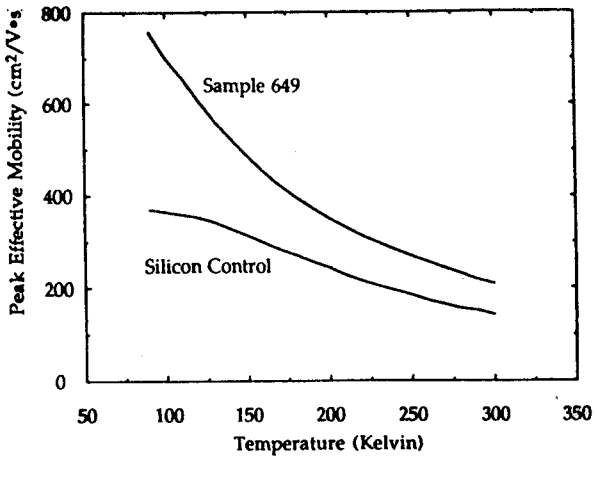

Fig. 26: Peak effective mobility versus temperature for a standard Si p-MOSFET and a SiGe channel p-MOSFET (after Garone, Venkatraman and Sturm [58]).

2.3. Low-Frequency Noise.

When designing a low-noise analog circuit, one of the key issues is the low frequency (LF) noise performance of the technology of choice. Comparing the equivalent input noise voltage e_n for comparable device area and currents, typical for amplifier operation, shows that a bipolar transistor stands out clearly compared with other Si transistor types (Fig. 27) [34]. Of course, a BJT has also an input current noise source i_n, whose impact depends on the input impedance and the collector current. In the next section, it will be discussed how lowering the temperature affects the LF noise for the different types of components/technologies.

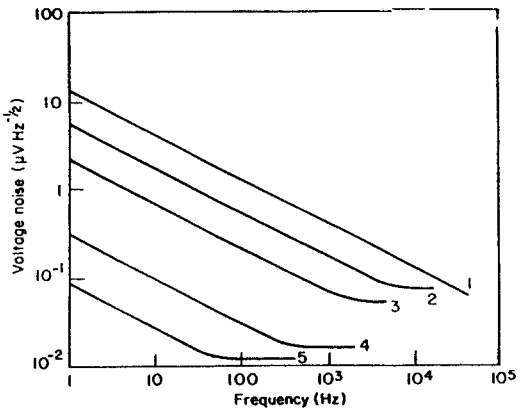

Fig. 27: 1/f noise in various silicon technologies at room temperature. MOS devices are operated in saturation; bipolar collector current ≈100 μA; MOSFET gate area and bipolar emitter ≈400μm^2. 1/ SOS; 2/ Si-n-MOS; 3/ Si-p-MOS; 4/ Si-JFET and 5/ Si-bipolar (after Jayadev et al. [34]).

BJTs

From §2.1 it has become clear that the only viable candidates for bipolar operation at cryogenic temperatures are polyemitter type of devices or HBTs with a SiGe base. Interest in this type of devices is growing quickly as they can be incorporated in a

BiCMOS technology which is very versatile from a viewpoint of mixed-mode/high-speed applications. To a lesser extent, the same applies for the cryogenic operation [36]. So far, a few results of initial low-temperature noise evaluation have been reported. An example is shown in Fig. 28 for polysilicon emitter BJTs [61], while Fig. 29 compares the LF noise spectrum of a standard BJT and a comparable HBT [62-63]. Overall, a weak temperature dependence is observed, which is comparable to the one observed for standard devices. It is expected that irradiation will increase the LF noise of polysilicon emitter BJTs at low base currents, since this 1/f noise is dominated by the peripheral surface-recombination related non-ideal base current I_{brec}. This radiation induced noise increase is speculated to be related to the radiation induced build-up of the interface trap density at the base-emitter surface depletion region covered by a thermal oxide. For small-area BJTs, it is anticipated that - provided new oxide traps are created - Random Telegraph Signals (RTSs) can be induced by total dose exposure. This is similar as for hot-carrier degradation, which is known to create RTSs in a broad temperature range [64-66].

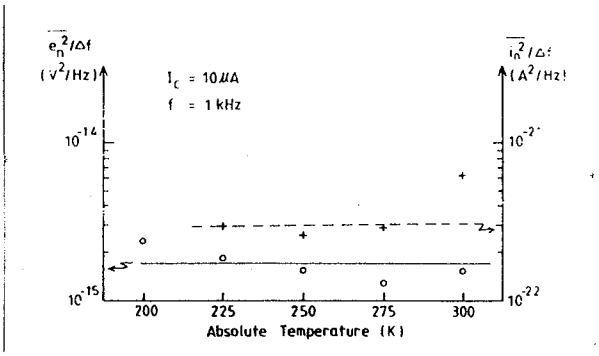

Fig. 28: The temperature dependence of $e_n^2/\Delta f$ and $i_n^2/\Delta f$ at a frequency f=1 kHz (I_C=10 μA) of a polyemitter BJT with interfacial oxide layer (after Lau et al. [61]).

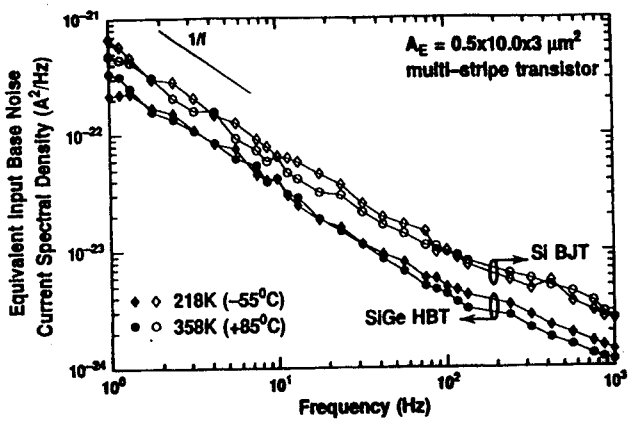

Fig. 29: Noise spectral density as a function of temperature at a frequency of 10 Hz (after Vempati et al. [62]).

Si JFETs

Looking at Fig. 27, second best on the list is a Si JFET. Such type of devices have shown excellent noise performance down to about 100 K [23]. However, when significant dopant freeze-out occurs in the channel, the LF noise generally shows a drastic

increase, as shown in Fig. 30. This means that for analog applications in the liquid helium temperature (LHT) range, JFETs are not a good candidate, inspite of technological modifications [24].

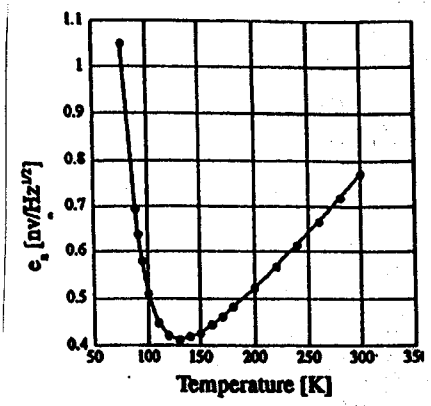

Fig. 30 Temperature behaviour of the equivalent input noise voltage density of an JFET based preamplifier (after Radeko, Citterio and Rescia [23]).

MOSFETs

The small-signal representation of a FET, including the input-referred current and voltage noise sources is represented in Fig. 31. Hereby is i_n the current noise source related to the presence of a gate current and e_n the input-referred equivalent noise source related to the flow of the channel current. A general expression for the latter source is given by [67-68]:

$$e_n^2 = S_{V_G}(f) = \frac{A_f}{f^\gamma} + \Sigma_{i=1}^{m} \frac{A_i \tau_{GRi}}{1 + (2\pi f \tau_{GRi})^2} + B_S \qquad (26)$$

and represented schematically in Fig. 32. As can be seen, eq. (26) contains different noise sources, whereby the first term corresponds to the flicker or 1/f noise and the second one to Generation-Recombination (GR) noise from different GR centres with relaxation times τ_{GRi}, respectively. For sufficiently small devices, with an area WxL ≤ 1 μm^2, so-called Random Telegraph Signals (RTS) caused by single interfacial oxide traps can dominate the LF noise. Finally, eq. (26) contains a white, frequency-independent noise term, which for MOSFETs is the thermal channel noise and corresponds to [69]:

$$S_{V_G} = e_n^2 = \kappa \frac{4kT}{g_m} \qquad (27)$$

with κ a bias-dependent parameter equal to 2/3 in strong inversion and to 1/2 in weak inversion. For short-channel devices and in saturation, one should take into account carrier heating effects, which leads to more sophisticated expressions for the thermal noise of a MOSFET [69-70]. From eq. (27), one can infer that the temperature will reduce the thermal noise and this due to the kT term and to the significant mobility increase at low temperature which applies down to the 4.2 K range.

The current noise source in Fig. 31 can be described by [68]:

$$i_n^2 = 2qI_G + \eta_n \frac{4kT}{g_m} C_G^2 f^2 \qquad (28)$$

One should hereby take into account - particularly for cryogenic operation - that the temperature in eqs (27) and (28) is to be considered as the channel, or active area temperature which is generally higher than the ambient temperature, due to self-heating.

I_G and C_G are the gate current and capacitance, respectively. The total equivalent noise voltage spectral density is then according to the scheme of Fig. 31 given by $e_n^2 + (Zi_n)^2$ plus possible correlation terms between the two sources. For standard MOSFETs, negligible gate current exists, so that the noise current source can be neglected in many cases.

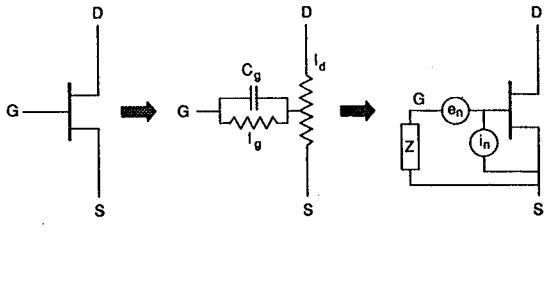

Fig. 31: Model for the low-frequency noise in field-effect transistors (after Kirschman [68]).

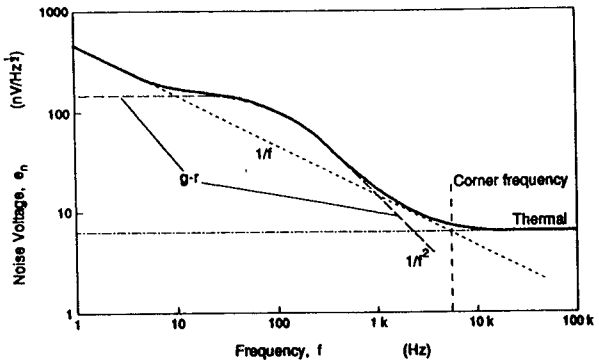

Fig. 32: A general FET noise-voltage spectrum illustrating the terms of eq. (26). Only one GR component, having a Lorentzian form is included (after Kirschman [68]).

Generally, the LF noise of a MOSFET is dominated by the 1/f term in eq. (26). Several models have been proposed, which roughly fall into two classes: the number fluctuation or ΔN and the mobility fluctuations or $\Delta\mu$ models, whereby some mixed variants, taking into account correlated mobility fluctuations have been developed recently. Different forms of the McWhorter ΔN theory for the 1/f noise of MOSFETs can be found in the literature. The resulting input-referred noise spectral density in linear operation is given by [71-72]:

$$S_{V_G} = \left(\frac{q}{C_{ox}}\right)^2 \frac{1}{WL\, f^{\gamma}} \frac{N_T(E_F)}{a_{tunn}} \qquad (29)$$

whereby a_{tunn} is a tunneling parameter for which several slightly different expressions can be found in the literature. One finds for instance [71]:

$$a_{tunn} = \frac{8\,\lambda_t}{kT} \qquad (30)$$

with λ_t the tunneling constant (order 10^8 1/cm). It is hereby assumed that only traps in an energy interval of kT around the surface quasi-Fermi level contribute to the fluctuations. For a constant interfacial oxide trap density kTN_T, eq. (29) predicts a more or less constant 1/f noise with temperature. Furthermore, according to eq. (29) no gate overdrive dependence of S_{V_G} in linear operation is expected if the McWhorter theory is valid.

The mobility-fluctuations based model predicts a linear increase of the 1/f noise in linear operation with the gate overdrive voltage V_{GS}-V_T. The corresponding input-referred noise spectral density is [73]:

$$S_{V_G}(f) = \left(\frac{q}{C_{ox}}\right) \frac{\alpha_H}{WLf} (V_{GS}-V_T) \qquad (31)$$

for long-channel devices. Hereby is α_H the Hooge parameter, first introduced to describe the flicker noise in homogeneous materials (resistors) as a bulk phenomenon [74-75].

Recently, a concensus between the two schools of thought is growing around a so-called unified flicker noise theory, which takes into account both number fluctuations and the correlated mobility fluctuations through carrier scattering [71,76-79]. The resulting normalised drain current noise spectral density takes the form [79]:

$$\frac{S_I}{I_D^2} = \frac{kT}{a_{tunn}\, WL\, f} \left(\frac{1}{N} + a_{scatt}\mu\right)^2 N_T(E_F) \qquad (32)$$

Hereby is N the carrier density per unit area and a_{scatt} the scattering coefficient associated with the trapped charge. Equation (32) is for instance also adequate to describe the 1/f noise in fully depleted SOI MOSFETs [80].

From the foregoing, it is clear that the study of the 1/f noise as a function of temperature can illucidate the underlying physical mechanism. An example of the variation with temperature is shown in Fig. 33 for an n-channel device [72]. In practice, little variation with both temperature and V_{GS} is observed, in good agreement with the McWhorter picture of eq. (29). The agreement with the number fluctuation theory extends into the saturation region. From this follows that the active oxide trap density in n-MOSFETs $kTN_T(E_F)$ ($/cm^2$) is constant in the range 4.2 K to 300 K. Because of this observation, the LF noise technique has been proposed to study the density of interfacial oxide traps as a function of E_F, close to the conducton band minimum at room temperature [71] and above the bottom of the conduction band at LHT.

The low temperature behaviour of the flicker noise of p-MOSFETs is completely different: both a strong variation with temperature and with gate bias (linear operation) is observed in Fig. 34 [72]. So far, different interpretations have been given to this fact. The first idea is that the LF noise of p-MOSFETs is better described by the $\Delta\mu$ expression (31) [72]. The derived α_Hs are in the range $4x10^{-7}$ to $8.1x10^{-5}$ [72]. An alternative interpretation is that for p-MOSFETs the density of interface traps in eq. (29) $kTN_T(E_F)$ varies significantly with E_F [81] or with V_{GS} and/or V_T. This reconciles the observations with the McWhorter picture and forms thereby the basis of an interface-state spectroscopy technique [71]. A final interpretation is based on the unified flicker noise theory of eq. (32). It has been demonstrated that the experimental 1/f noise behaviour with temperature of both n- and p-MOSFETs can be successfully explained by that model [78]. As such, the unified model provides the most complete picture for 1/f noise in MOSFETs to date.

Generation-recombination (GR) noise has been observed in low-temperature MOSFETs [82-84]. In linear operation, the GR noise is believed to be generated mainly by defect centres in the depletion region of the devices and as such can be used to study in a spectroscopic way technological problems. An example of a defect spectrum in function of the temperature is given in Fig. 35 for a p-MOSFET [84].

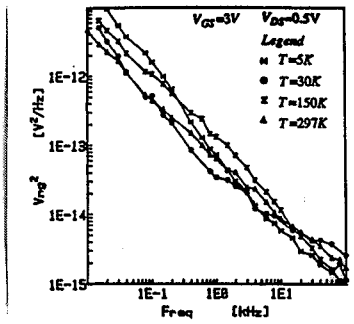

Fig. 33: Comparison of the n-MOSFET input-referred noise spectra at temperatures from 5 to 297 K (after Chang, Abidi and Viswanathan [72]).

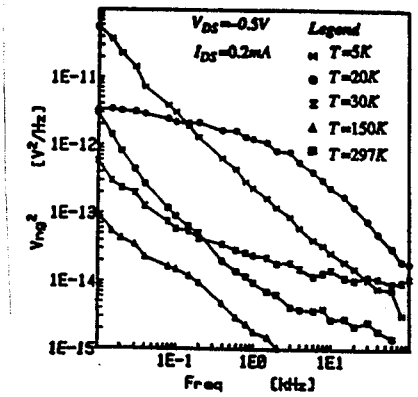

Fig. 34: Comparison of the p-MOSFET input-referred noise spectra at temperatures from 5 to 297 K (after Chang, Abidi and Viswanathan [72]).

In small-area MOSFETs, a single (oxide)trap can generate a bistable switching of the drain current passing through the channel, called RTS [85].The corresponding noise spectrum is Lorentzian, with a characteristic time constant (corner frequency) which is a strong function of temperature. Generally, the temperature variation of the capture and the emission time is used to determine the trap energy and the activation energy of the capture cross section. At very low temperatures (LHT range) some specific type of RTS behaviour can be observed, which is related to other types of carrier-trap interactions [86]. It should finally be noted that, since RTSs are generally associated with traps in the oxide near the interface, both hot-carrier degradation and irradiation can create new RTSs [87].

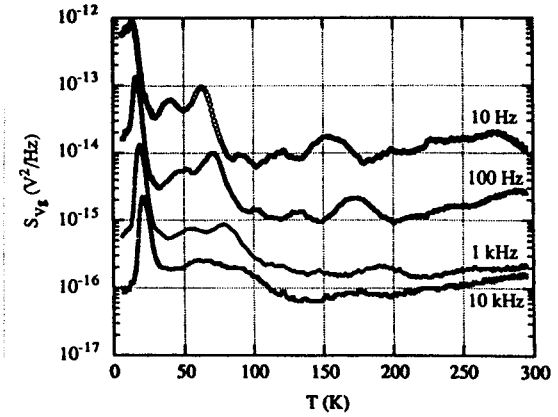

Fig. 35: LFN versus T scan for a p-MOSFET in the range 6-295 K. I_D=20 μA; V_{DS}=-1 V; W/L=100/5; t_{ox}=40 nm (after Scholz and Roach [84]).

A specific kind of GR noise can be encountered when operating a Si MOSFET in the drain-current kink region at low tempeature. In that case, the low-frequency noise generally shows a strong overshoot at constant frequency f [88], which may be several orders of magnitude higher than the background 1/f-like noise, observed in linear operation. This behaviour is typically found in bulk MOSFETs operated at liquid-helium temperatures [89-90] and in floating-body operated SOS and SOI MOSFETs [88] in a broad temperature range. The noise spectrum in the noise overshoot region becomes Lorentzian, i.e. typical for GR noise.

Phenomenologically, the LF noise overshoot in bulk MOSFETs at liquid-helium temperatures behaves as follows. The overshoot amplitude reduces with temperature, when going from 4.2 K to 20 K (Fig. 36), similar as the corresponding drain current kink. Above approximately 20 K, it disappears from observation. Applying a forward substrate bias, or a floating body likewise reduces the noise overshoot. Furthermore, the effect is far more pronounced for n-MOSFETs compared with p-channel devices. These observations suggest a tight connection with the static kink and hence with the multiplication-current generated near the drain. Another striking feature is that a hysteresis is observed in the noise overshoot at LHT (Fig. 37).

Summarizing, the kink-related LF noise overshoot originates most likely from GR fluctuations caused by deep-level traps in the depletion region of the MOSFET. Under this assumption, it can be modeled in a similar way as the GR noise which has been observed in linear operation. This results in the following expression for the normalized current noise spectral density [88]:

$$\frac{S_I}{I_D^2} = \frac{S_I(0)}{I_D^2} \frac{\tau}{1 + (2\pi f t)^2} \tag{33a}$$

with :

$$\tau = \frac{C}{I_B} \tag{33b}$$

Hereby is C a semi-empirical constant. Equation (33b) demonstrates the tight connection between the static kink and the LF noise overshoot, with the substrate current I_B generated at the drain as binding element. It has been shown that eqs (33) provide a sound basis for a good qualitative modeling of the noise overshoot, both for bulk and SOI MOSFETs, as illustrated in Fig. 38. The model correctly reproduces the observed frequency and device area WxL dependence of the amplitude, which is given by [88]:

$$\Delta S_I(f) = g_m^2 \frac{q^2 N_T w_d}{C_{ox}^2 WL} \frac{1}{4\pi f} \tag{34}$$

with C_{ox} the gate oxide capacitance per unit of area, w_d the part of the depletion region where the GR events take place and N_T the density of active GR centers. For LHT operation, N_T corresponds to the doping density. The 1/L and 1/f dependence of the amplitude have been verified experimentally. At the same time, it has been demonstrated that the position of the noise overshoot maximum shifts parallel with the saturation voltage V_{DSAT}, again emphasising the relationship with the avalanche-multiplication near the drain. A yet poorly explored regime is the LF noise behaviour in the subthreshold latch region for SOI MOSFETs. It is anticipated that a similar increase in the LF noise magnitude will occur. The basic mechanism may, however, be significantly different, taking into account the parasitic lateral bipolar operation and the associated noise.

Finally, it has been found that room temperature exposure to γ-irradiation leads in some cases to a reduction of the noise overshoot in SOI n-MOSFETs [91]. No low temperature data are available in this respect.

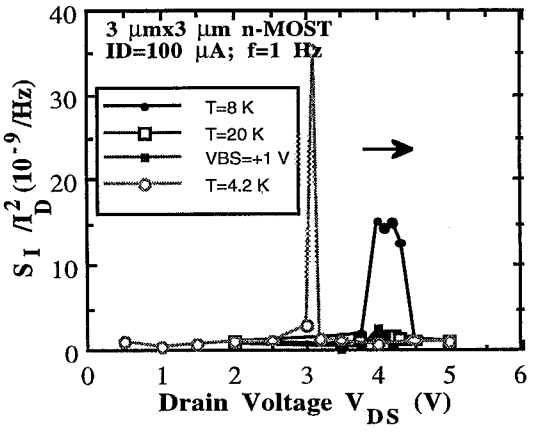

Fig. 36: Normalized LF noise overshoot for a 3 μmx3 μm bulk n-MOSFET, operated in the liquid-helium temperature range (after Simoen and Dierickx [90]).

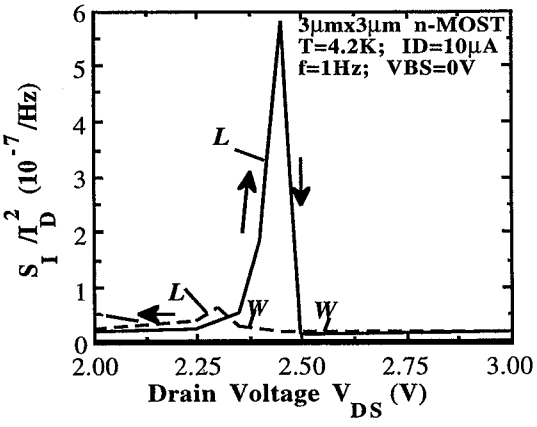

Fig. 37: Hysteresis in the LF noise overshoot. The arrows indicate the direction of variation of the drain voltage (after Simoen and Dierickx [90]).

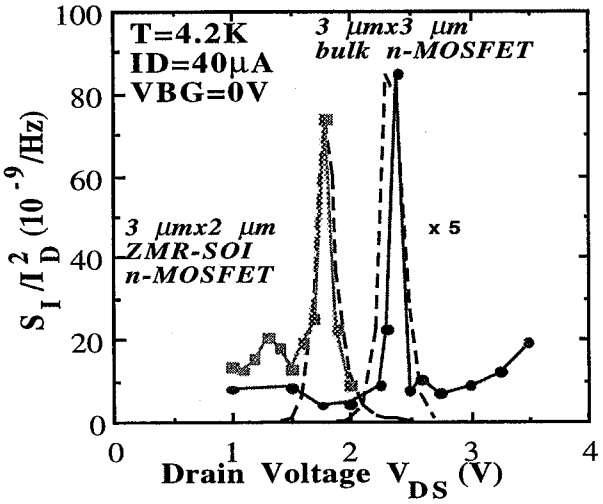

Fig. 38: Comparison of the experimental noise overshoot with the model of eq. (33) (dashed lines), for a PD SOI and a bulk n-MOSFET at 4.2 K.

Noise aspects of cryogenic Si circuits.

Most cryogenic analog applications are in the field of detection/sensing of infrared, optical or nuclear radiation. One class of devices often used for this purpose are CCDs. Modern CCD technologies are based on n-type buried-channel MOSFETs, because of their low noise behaviour. The main sources of noise in a CCD are [92-93]: photon shot noise; transfer noise; output stage noise and reset noise.

The output stage noise is dominated by the input-referred noise of the output transistor, as shown in Fig. 39, which has been discussed in the previous section. Reset noise or kTC noise (C the output capacitance, where the signal charge is loaded) originates from the uncertainty in the reset level (Fig. 40) and can be elimininated by using the so-called correlated double sampling technique (CDS). In the CDS scheme, the reset level is

sampled and subtracted from the signal sample to obtain a true estimate of the signal charge packet size [92].

Below 50 K approximately, the reset noise increases drastically (Fig. 41) and relies heavily on the method of resetting used. The increase is related to the impact of the interface states and can be utilised to estimate N_{it} [94]. It has furthermore been demonstrated that the LF noise of a CCD increases after irradiation with γ-rays or high energy ions [92,95], which raises the question of device hardening if space (or military) applications are envisaged.

For the read-out of IR focal plane arrays, quite often CMOS-based multiplexer circuits are used [96]. Particularly for deep-cryogenic space-applications, like the Infrared Space Observatory (ISO) mission [96], severe constraints are imposed for the power consumption and the low-frequency noise of the read-out electronics, which operates at the same temperature as the detectors, i.e. in the range 2 to 10 K. An example of the noise equivalent power (NEP) of the Cryogenic Read-out Electronics (CRE) used in the ISO satellite is given in Fig. 42 [96]. The read noise is limited to 200 electrons. Such low values are necessary, since the photocurrent of the long-wavelength IR detectors is small.

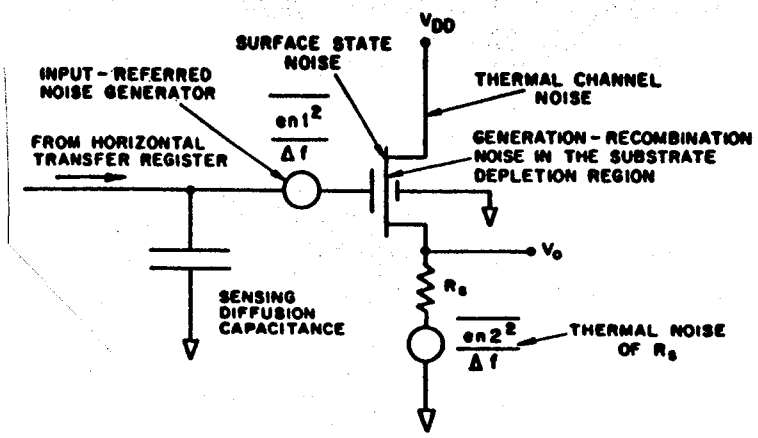

Fig. 39: Output stage noise sources (after Haslett [92]).

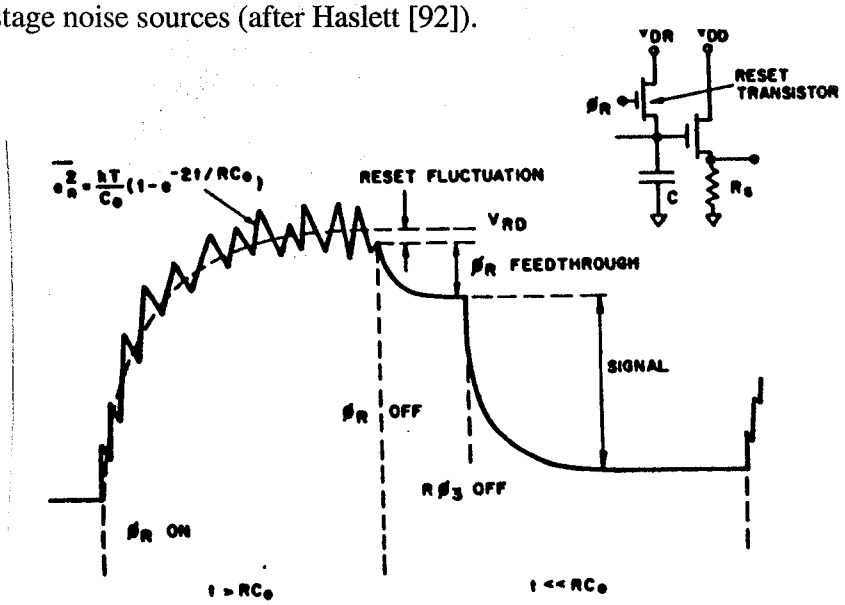

Fig. 40: Origins of reset noise (after Haslett [92]).

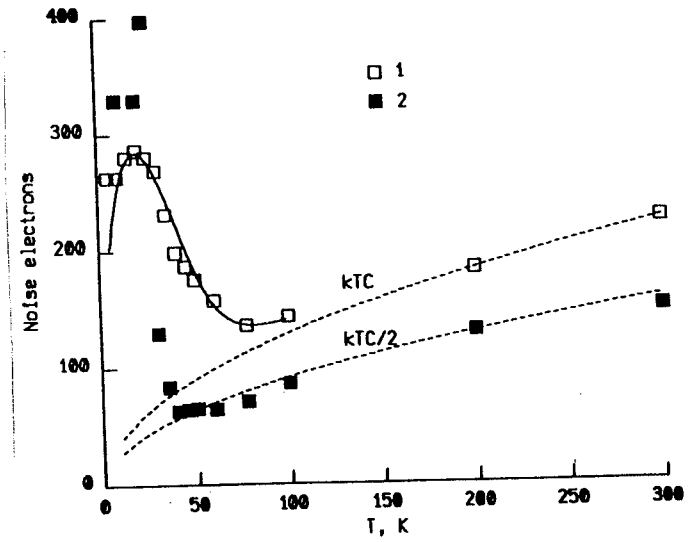

Fig. 41: Reset noise versus T. Measured reset noise (squares): 1- conventional method of reset; 2 - fill-and-spill method of reset. Solid line - calculated reset noise for the conventional method. Dashed line - the calculated level of kTC noise for both methods (after Bock [94]).

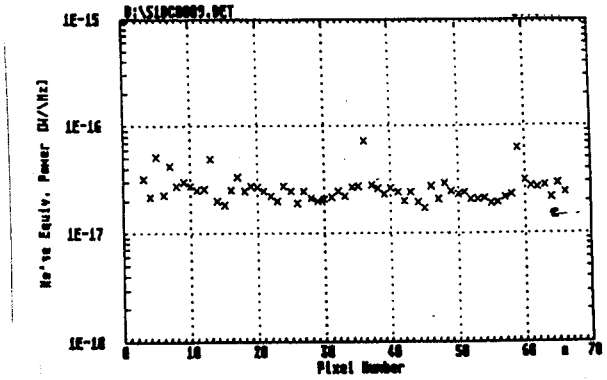

Fig. 42: NEP measured at 4.48 K and corresponding to the output of a 64 pixel Si:Ga detector array. Pixel size 310x370x1800 μm. The integration time is 587 ms and the photon flux 9.27x10^7 /cm s (after Dierickx et al. [96]).

2.4. Reliability and Stability Aspects.

In the foregoing it has become clear that CMOS isby far the current technology of choice for the fabrication of cryogenic Si electronics. Therefore, most of the studies with respect to the stability of the device operation and reliability at low temperature have been devoted to MOSFETs. This will be the main part of this section. First, the transient behaviour at low temperature will be briefly discussed. Next, the impact of hot-carrier (HC) and homogeneous degradation at cryogenic temperature (mainly LNT) is reviewed. At the end, the available information regarding BJTs will be summarised.

MOSFETs

In the foregoing, it has already been mentioned that the cryogenic operation of Si devices is quite often accompanied by transient and hysteresis effects, especially in the freeze-out regime. In the case of a MOSFET the freeze-out will first of all affect the formation of the depletion region at the reverse biased drain junction and in the substrate adjacent to the channel. Since ionization at liquid helium temperature can become quite slow, the response of a MOSFET to a change in V_{DS} or V_{GS} will be characterised by long time constants τ_{ion}. An example of the ionization time constant for B and In is shown in Fig 43 [97], indicating that at 4.2 K time constants in the range of seconds and higher are not extraordinary, even if account is made for the field-assisted ionization effects. On the other hand, for increasing temperature steady-state will be established faster, whereby the time constant at sufficiently high temperature is determined by the ground-state energy of the dopant level. As can be derived from Fig. 43, the deeper the dopant level, the longer the time constants will be (compare e.g. In with B).

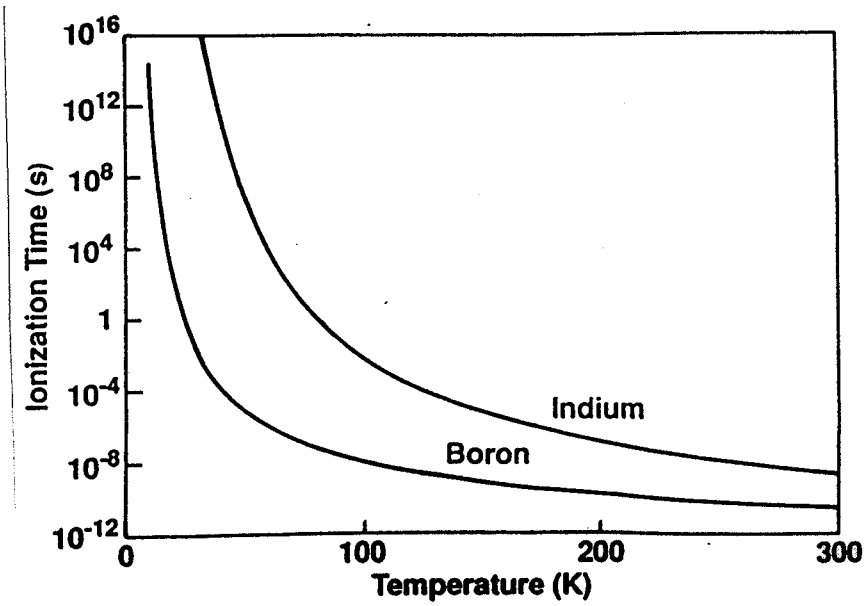

Fig. 43: Thermal ionization times versus temperature for boron and indium. (after Foty [97]).

The transient response of Si bulk MOSFETs at liquid helium temperature has been extensively treated in the literature [98-99]. Assuming that the ionization of the shallow dopant atoms proceeds exponentially in time, e.g. following:

$$N_A^-(t) = N_A\,[1-\exp(-\frac{t}{\tau_{ion}})] \qquad (35)$$

it can be demonstrated that the threshold voltage of a MOSFET responds to a step in bias or a pulse, according to [98]:

$$V_T(t) \approx V_T(0) + \frac{\sqrt{2q\varepsilon_{si}}}{2C_{ox}} \frac{\Delta N_A^-}{N_A^-(0)} [1-\exp(-\frac{t}{\tau_{ion}})] \qquad (36)$$

with $V_T(0)$ the initial threshold voltage at time zero and $\Delta N_A^- = N_A - N_A^-(0)$ the total change in ionised acceptor density (a p-type substrate in an n-MOSFET is assumed and full ionization is expected for infinite time t-->∞). For a not too large transient amplitude, the drain current transient will also be exponential with time and obeys:

$$I_D(t) \approx \frac{W}{L} \mu_n \frac{C_{ox}}{2} [V_{GS}-2V_T(t)] V_{GS} \qquad (37)$$

with $V_T(t)$ given by eq. (36). Equation (37) has been derived for the saturation regime. In linear operation, the V_{GS}-V_T dependence of the drain current immediately shows the same time variation of V_T, whatever its magnitude is. The quasi-exponential nature of the I_D transient at 4.2 K is shown in Fig. 44

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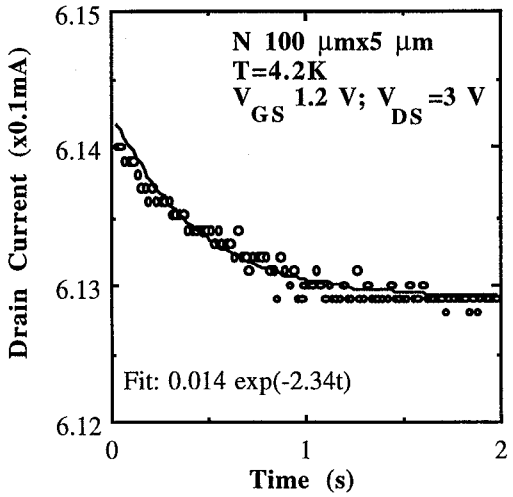

Fig. 44: Exponential I_D transient at 4.2 K in a 100 µmx5 µm n-MOSFET, after applying a voltage step to the gate and the drain from 0 V to 1.2 V and 0 V to 3 V, respectively.

Thermal ionization is very unlikely (very slow, see also Fig. 43) to happen at 4.2 K. However, for sufficiently large V_{DS} and I_D, shallow-level impact ionization is possible. For V_{DS} below V_{DSAT}, primary channel carriers may gain sufficient energy to impact ionise an occupied dopant atom, while for $V_{DS} \geq V_{DSAT}$ band-to-band ionization will occur, followed by the injection of holes in the substrate (for an n-MOSFET). The latter can interact in turn with the frozen-out dopants at the edge of the depletion region, causing what can be called a Forced Depletion Layer Formation (FDLF) [100]. Since there exists two sources of impact ionization, namely, the shallow impact ionization (SII) by channel carriers and the secundary SII by multiplication-generated holes, a different behaviour can be expected. This is reflected in the clockwise and counterclockwise hysteresis observed in a MOSFET at 4.2 K (Fig. 45). The counterclockwise hysteresis is related to the FDLF mechanism and substantiated by the dependence of the observed time

constants τ_{FDLF} on V_{GS} and V_{DS} (Fig. 46) [100]. These time constants have been experimentally derived by measuring the response of the MOSFET on a gate voltage square-wave. The model fitted in Fig. 46 is given by:

$$\tau_{FDLF} = \frac{K_1}{I_D} \exp\left(\frac{K_2}{V_{DS}-V_{DSAT}}\right) \qquad (38)$$

Hereby are K_1 and K_2 empirical coefficients. The correlation with the substrate current generated near the drain is substantiated by the calculated loci of equal FDLF time constants, shown in Fig. 47 and obeying the condition [100]:

$$V_{DS}-V_{DSAT} = \frac{V1}{\ln(V2\tau_{FDLF}I_D)} \qquad (39)$$

Equation (39) points out that they are parallel to the loci of constant V_{DS}-V_{DSAT}.

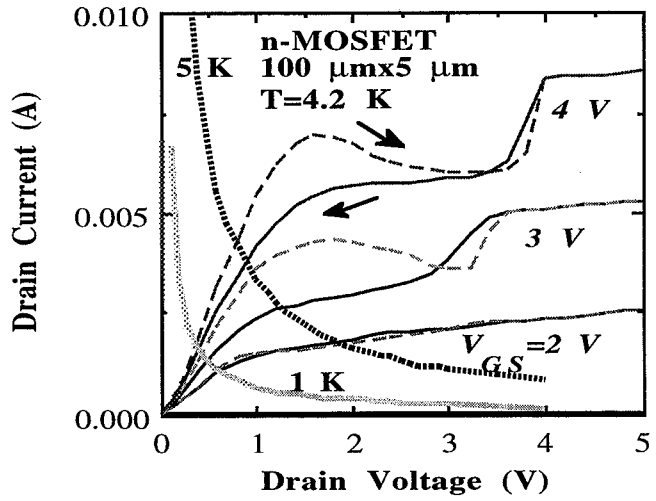

Fig. 45: Output characteristics of a W=100 µm and L=5 µm n-MOSFET at 4.2 K, for a low-to-high and a high-to-low voltage sweep, indicated by the arrows. A clear ∞-shaped hysteresis is discernable. Also indicated are the estimated limits for a ΔT=1 K and ΔT=5 K self-heating of the channel due to the drain current flow at 4.2 K. (after Simoen and Claeys [99]).

Transient behaviour in linearly operated SOI MOSFETs has been observed in a much wider temperature range than for bulk MOSFETs, well above 77 K [101-102]. This is again related to the slow thermal generation rate of carriers, resulting in a transient response on a voltage pulse, beit at the front or the back gate. An example is given in Fig. 48, showing the response of a PD 0.7 µm SOI n-MOSFET to a back-gate bias pulse [102]. The application of the positive bias pulse at low temperature drives all free carriers from the film region, leaving behind a fully depleted body, called the charge cavity. Since the thermal generation of carriers is very slow at 77 K or 4.2 K, the body can remain in its fully depleted metastable state for a long time (minutes at 77 K to hours at 4.2 K). The resulting threshold voltage is larger than before the application of the pulse. This effect has been called the Multistable Ccharge Controlled Memory effect (MCCM), since various metastable states can be achieved, depending on the amplitude of the applied back- or front gate bias pulse [102]. Potentially, a 1 transistor memory cell can be envisaged exploiting this effect at low temperature. The initial low state can be reached

again through the injection of carriers, either optically (which opens a potential for optical detection), or e.g. through a high V_{DS} hot-carrier injection [102].

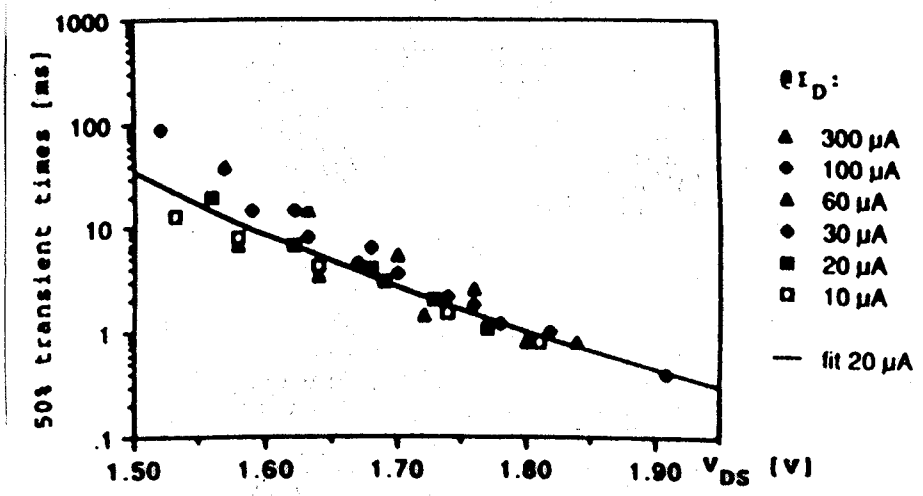

Fig. 46: FDLF time constants versus V_{DS}. (after Dierickx et al. [100]).

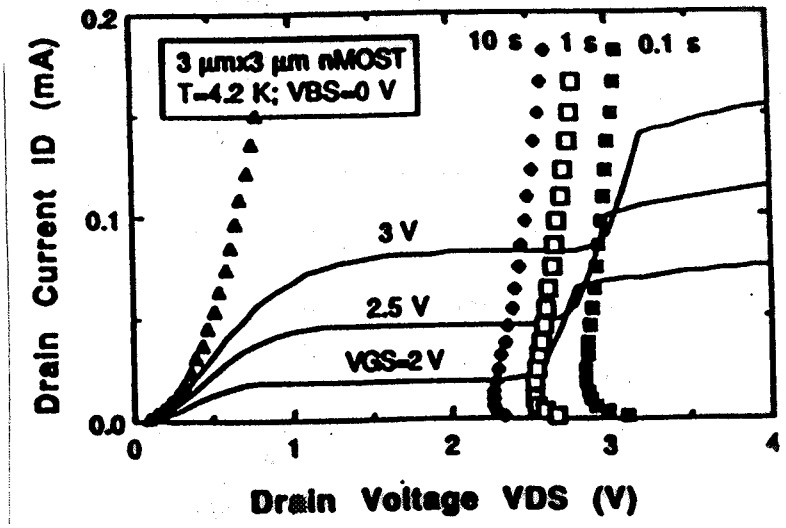

Fig. 47: Loci of time constants, corresponding to τ_{FDLF} =10 s, 1 s and 0.1 s. Also shown is the calculated V_{DSAT} (triangles) for a 3 µm x 3 µm n-MOSFET at 4.2 K. (after Simoen and Claeys [98]).

The HC degradation in Si MOSFETs is related to the occurrence of avalanche multiplication in the high-field region near the drain, when the device operates in saturation. Cooling in principle increases the number of ionization events experienced by a hot carrier per unit of distance travelled, since the multiplication rate:

$$\alpha_{n,p} = \alpha_{n;p}^{\infty} \exp(\frac{-\beta_{n;p}}{E}) \qquad (40)$$

increases with lower temperature (subscript n for electrons; p for holes). The impact ionization (II) coefficients $\alpha^{\infty}_{n;p}$ and $\beta_{n,p}$ are a function of the electric field and can be considered as, respectively, the impact ionization rate for very high fields and a critical field for II.

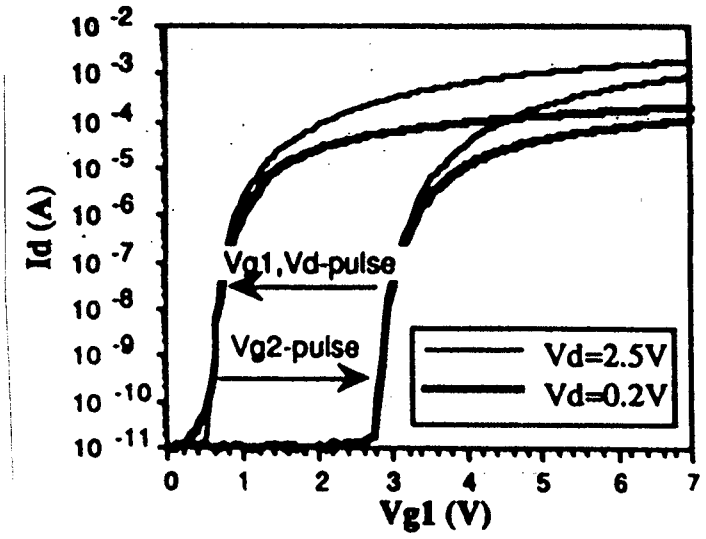

Fig. 48: The multistable charge controlled memory (MCCM) effect at 77 K. (after Tack and Claeys [102]).

With respect to the temperature dependence of the ionization coefficients α^{∞} and β, a few expressions have been proposed in the literature, which are generally based on an optimal fit to the available literature data [12]. For n-type Si one finds for instance [103]:

$$\alpha_n^{\infty} = 7\text{x}10^5\ \text{cm}^{-1}\ (0.57 + 0.43\text{x}(\frac{T}{300\ \text{K}})^2) \qquad (41a)$$

$$\beta_n = 1.23\text{x}10^6\ \frac{\text{V}}{\text{cm}}\ (0.625 + 0.375\text{x}(\frac{T}{300\ \text{K}})) \qquad (41b)$$

For the low-temperature dependence of the hole impact ionization coefficients, the MINIMOS simulation program of Selberherr contains the following [103]:

$$\alpha_p^{\infty} = 1.58\text{x}10^6\ \text{cm}^{-1}\ (0.58 + 0.42\text{x}(\frac{T}{300\ \text{K}})^2) \qquad (42a)$$

$$\beta_p = 2.04\text{x}10^6\ \frac{\text{V}}{\text{cm}}\ (0.6 + 0.33\text{x}(\frac{T}{300\ \text{K}})) \qquad (42b)$$

Comparing the model with the available literature data [104-106] yields the results of Fig. 49a. The α_p corresponding to eq. (42) is represented in Fig. 49b. Note first of all that the impact ionization rate increases upon cooling, reflecting an increase of the

carrier mean free path with lower temperature. In other words, the carriers loose less easy energy through optical phonon collisons and therefore have a larger probability to undergo an II event, in spite of the increase of E_G. Another important trend is that for higher fields the ionization rates become less temperature dependent.

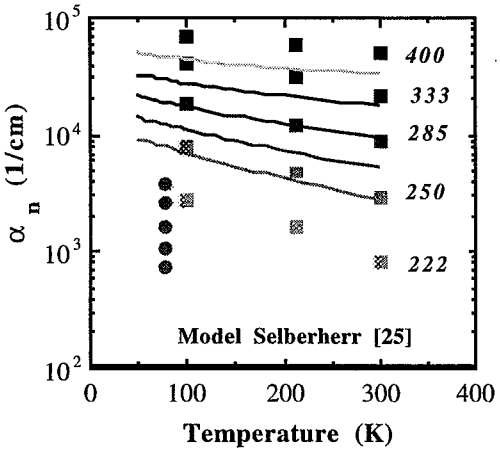

Fig. 49a: Theoretical electron impact ionization rate α_n according to eq. (41) [103] (lines), compared with experimental data points, obtained by Lee et al. [105] (squares) and by Takayanagi et al. [106] (circles) at 77 K. The field is in kV/cm.

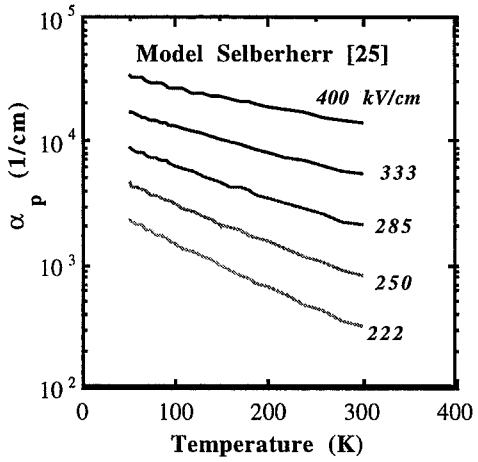

Fig. 49b: Theoretical hole impact ionization rate vs temperature, according to eqs. (42) [103]. The fields are in kV/cm.

Based on the increase of the II rate upon cooling, it is inspected that the substrate current generated near the drain by impact ionization also increases at low temperature. This is in first approximation indeed observed, as shown for example for 77 K in Fig. 50 [107]. However, note that for sufficiently low drain bias V_{DS} the I_B at 77 K is lower than at RT - this effect is called the cross-over behaviour of the substrate current. For deep submicron transistors, it has been observed that this cross-over region extends to the whole practical bias range in Fig. 51 [108]. Summarising this: in principle, if the substrate current is a good measure for the device lifetime, the HC degradation problem should become worse at LNT, except for low V_{DS} (low power) and for deep submicron technologies.

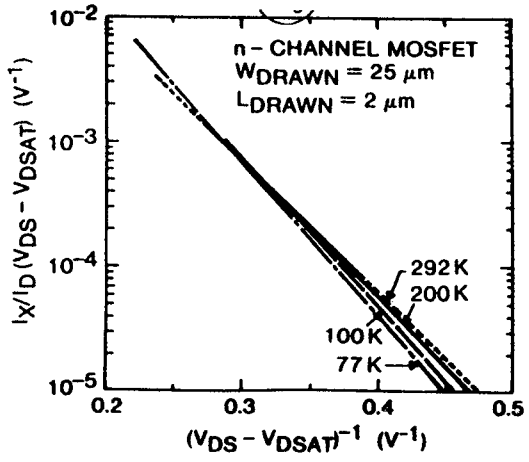

Fig. 50: Log [$I_B/I_D(V_{DS}$-$V_{DSAT})$] versus 1/(V_{DS}-V_{DSAT}) with temperature as a parameter (after Lau et al. [107]).

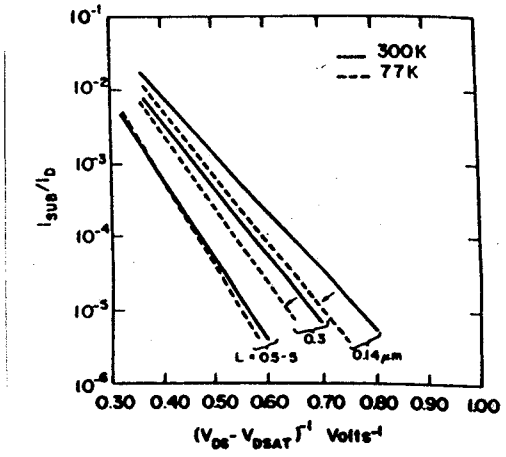

Fig. 51: Plots of I_B/I_D versus $1/(V_{DS}-V_{DSAT})$ for 0.14 μm<L<5 μm n-MOSFETs, at room temperature and 77 K. Note the enhanced reduction of the substrate current generation at low temperature for short-channel devices (after Shahidi, Antoniadis and Smith [108]).

Early HC degradation studies revealed that for n-MOSFETs the change of the device parameters (Δg_m, ΔV_T,...) follows a power law with stress time t, so that one can write [109-113]:

$$\frac{\Delta g_m}{g_m} = C\, t^n \qquad (43a)$$

$$\Delta V_T = C'\, t^n \qquad (43b)$$

n having typically a value in the range 0.4 to 0.6, independent of the stress temperature. This indicates that the fundamental degradation mechanism remains the same at all temperatures, for the same stressing conditions. An example of the transconductance degradation is shown in Fig. 52. It can be seen that the degradation becomes worse with decreasing temperatures. Typically, the degradation increases by a factor 3 up to 10 for 77 K stress compared to room temperature. This is what is generally expected from the stronger carrier heating effects described in the previous sections. Based on the increase in substrate current, one can already do some rough predictions of the HC lifetime at e.g. 77 K and estimate the maximum allowable supply voltage for low temperature operation [114].

Maximum degradation in classical non-LDD n-MOSFETs is observed for a stressing bias corresponding to the point of maximum substrate current generation, i.e. for $V_{GS} \approx V_{DS}/2$. This is also true for a cryogenic stress with respect of the change in g_m [115], but not the case if ΔV_T is used as a lifetime estimator (Fig. 53). In the latter case, the largest degradation at 77 K is found for a stress with $V_{GS} \geq V_{DS}$. This corresponds to a favourable condition for Channel Hot Electron (CHE) injection. On the other hands, hot holes will be injected for $V_{GS} << V_{DS}$. For intermediate values, e.g. the maximum substrate current point, both holes and electrons can be injected in the oxide, close to the drain.

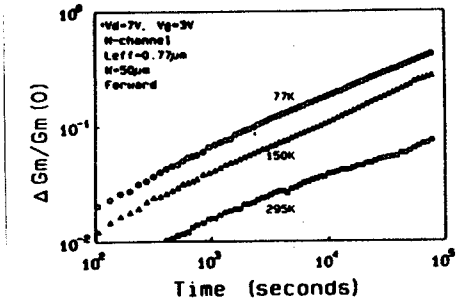

Fig. 52: The degradation with stress time of the transconductance in n-channel MOSFETs during hot-electron injection at different temperatures. (after Tzou et al. [112]).

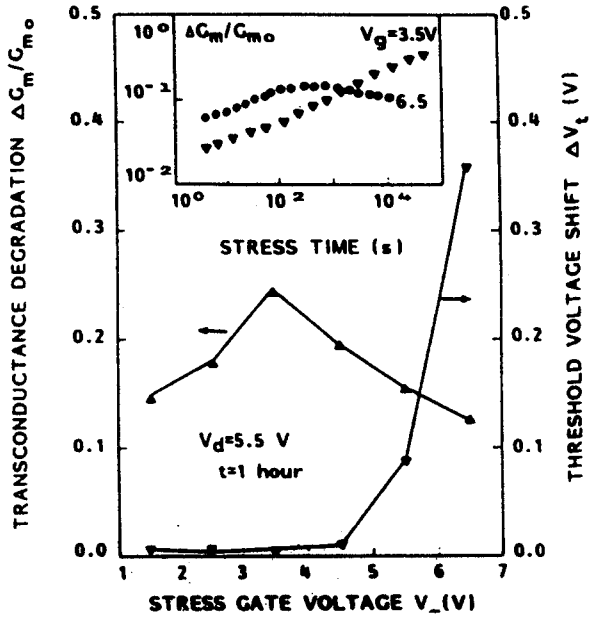

Fig. 53: Maximum transconductance degradation and threshold-voltage shift versus gate voltage after 1-h stress at 77 K with V_{DS}=5.5 V. The inset shows the maximum g_m degradation versus stress time for V_{GS}=3.5 and 6.5 V respectively. (after Nguyen-Duc et al. [115]).

The application of HC degradation leads to an asymmetrical damaging of the interface and oxide properties close to the drain. As a consequence, the linear MOSFET characteristics show a pronounced asymmetry after sufficient HC stress. This means that there will be a difference between the I_D-V_{GS} measured in Forward (F) or in Reverse (R) operation, i.e. with source and drain interchanged. This effect becomes more pronounced for 77 K stress, as shown in Fig. 54 [116]. In many cases the low temperature degradation is studied by measuring the R operation input characteristics.

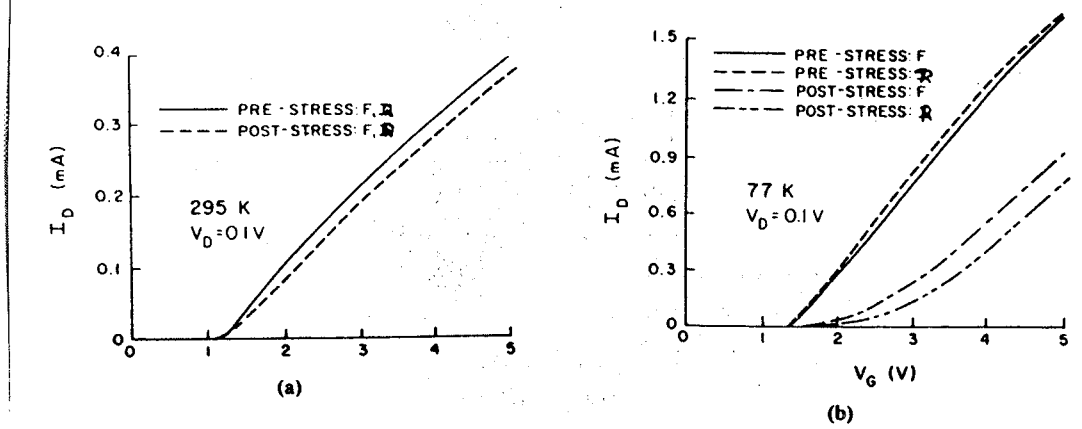

Fig. 54: Drain current of an n-channel MOSFET as a function of gate voltage for V_{DS}=0.1 V (a) at room temperature and (b) at 77 K, for Forward (F) and Reverse (R) mode operation. (after Von Bruns and Anderson [116]).

Extensive studies [113,116-117] point out that not only is the degradation for the same stressing conditions worse at low temperature, but also that the same amount of degradation has a stronger effect at low temperature. This is illustrated in Fig. 55, showing the relative reduction of g_m as a function of temperature, for an LDD n-MOSFET stressed at 78 K [117]. Several physical mechanisms and models have been advanced to explain this feature. Device simulations have demonstrated that the carrier concentration at low temperature is more sensitive to the surface potential variations, which are related to the localised HC stress induced charge near the drain. Additionally, since Coulomb scattering effects become dominant for cryogenic operating conditions, the presence of trapped charge and/or more interface traps near the drain will have a stronger impact on the mobility. From simulations with a localised charge near the drain follows further that one can expect even an overshoot in g_m [115]. This was experimentally verified for a 77 K stress and can be qualitatively explained by the fact that for a stressed n-MOSFET, the transconductance is governed by the damaged region, which has, however, a much shorter length (range 0.1 μm).

There exists an empirical relationship between the substrate current I_B generated during the HC stress and the device lifetime τ of an n-MOSFET, which is defined as the stress time corresponding to a 10 % degradation. It takes the general form:

$$\tau = A\, I_B^{-k} \qquad (44)$$

with k≈2.9. The same behaviour is observed for n-MOSFETs stressed at low temperature [111-112]. The observed k-value is in first approximation temperature independent, as follows from the data shown in Fig. 56. This can be explained by the fact that k equals the ratio Φ_B/E_i, which is the ratio of the oxide injection barrier to the energy threshold for impact ionisation. This function is only weakly dependent on temperature [112]. Moreover, the pre-factor A in eq. (44) is thermally activated with an energy of 39 meV [112].

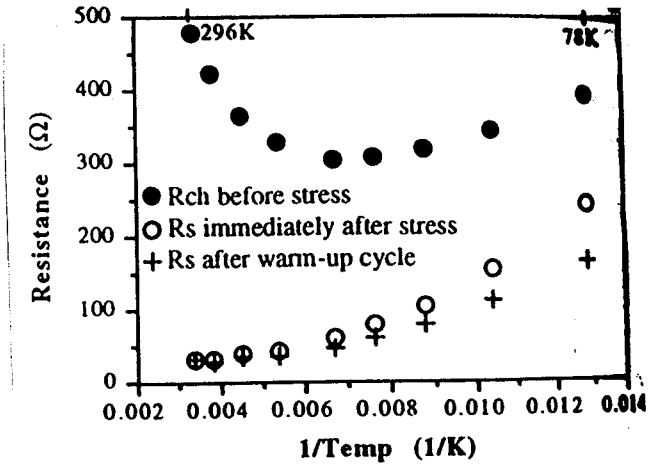

Fig. 55: Relative reduction of the transconductance versus 1/T. The device was stressed once at 78 K, with V_{DS}=7 V and V_{GS} at I_{Bmax} for 1000 s. W/L=11/0.75. (after Song et al. [118]).

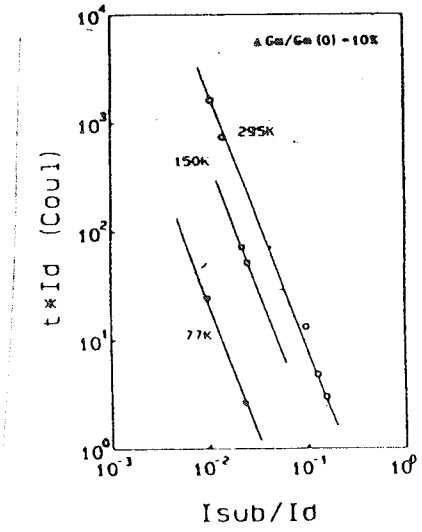

Fig. 56: The device lifetime (10 percent degradation in the transconductance) versus I_B/I_D at different temperatures. (after Tzou et al. [112]).

Figure 56 may lead to the conclusion that the substrate current is a good monitor for lifetime estimation of n-MOSFETs operating at cryogenic temperatures. However, this is only true for non-LDD CMOS technologies. As will be seen in a later section, for submicron LDD MOSFETs there is no clear relationship between the degradation and I_B. Therefore, for modern technologies other criteria need to be considered. The same applies for the HC degradation of p-MOSFETs. Although p-channel devices are less prone to HC degradation, because of the lower multiplication rates (and hence lower I_B), one should take into account that the stress behaviour is completely different. For these devices the behaviour with stress time is rather logarithmic, i.e. it follows a $\ln(1+\frac{t}{t_{ox}})$ dependence, saturating for larger t [118-119]. The parameter T_{ox} depends on the degradation

conditions and on the transistor type. It has been suggested to use a gate-current based lifetime monitoring for p-channel devices instead of using I_B [120].

Although there are only a few studies reported of p-MOSFET degradation at cryogenic temperature [113], they show a similar time dependence as at room temperature (Fig. 57). Typical results are summarised in Fig. 58, showing an opposite surface-oriented dependence for n- and p-MOSFETs [121].

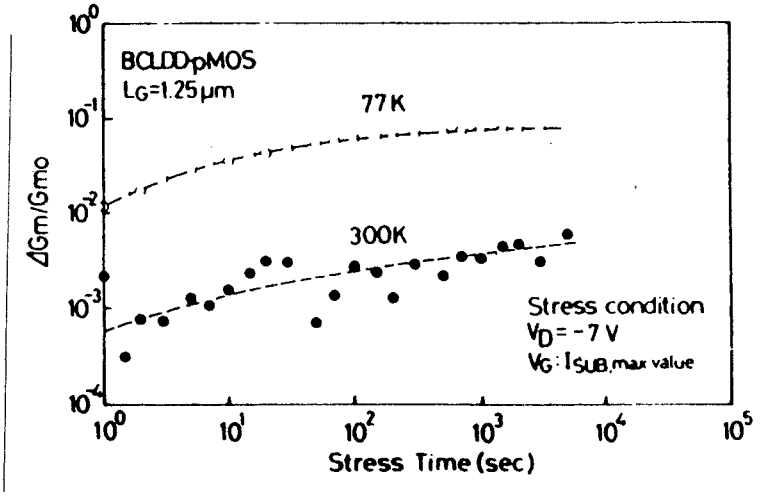

Fig. 57: Stress time variation for g_m degradation of a buried-channel LDD p-MOSFET. Gate bias stress was set at a value providing maximum substrate current. After stress g_m was measured at $|V_{DS}|$=0.1 V. (after Aoki et al. [113]).

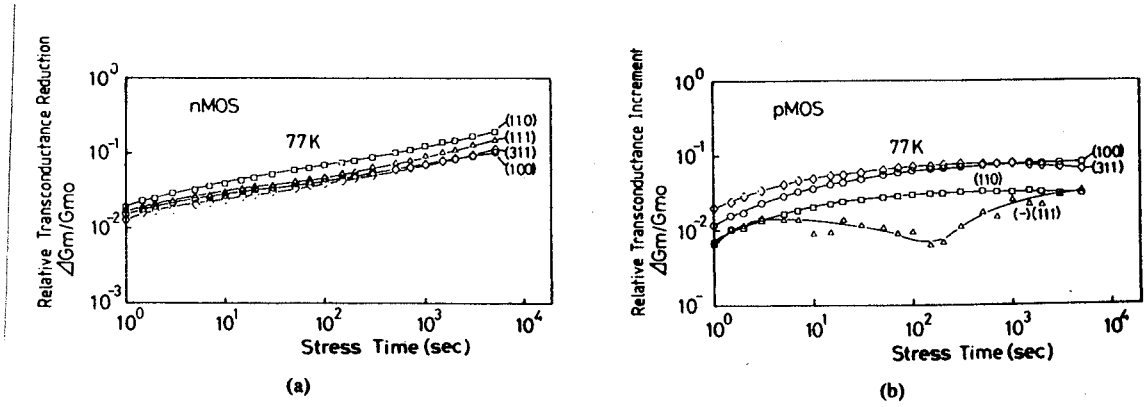

Fig. 58: Relative transconductance change as a function of the stress time at 77 K for n-MOS (a) and for p-MOS (b) transistors, with the surface orientation as a parameter. The gate length and width are 1.25 μm and 15 μm, respectively. After stress, g_m is measured at V_{DS}=0.1 V. (after Aoki et al [121]).

HC degradation at 4.2 K reveals a number of typical phenomena. First, conductance peaks have been observed in g_m before and after stress in the subthreshold regime (Fig. 59) [122]. Although several physical mechanisms have been advanced to explain this phenomenon, the available evidence strongly suggests that the peaks are related to discrete interface traps, which, upon changing charge state, control the current flow through the inhomogeneous channel.

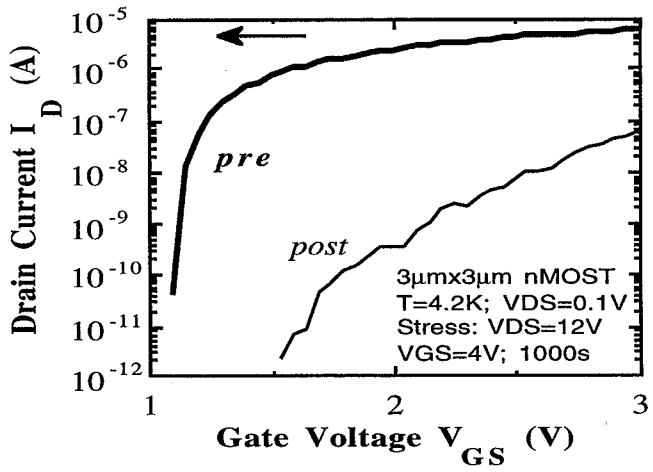

Fig. 59: Conductance peaks observed in linear operation at 4.2 K after the application of HC stress.

Reversible (transient) and irreversible changes have been observed due to stress at 4.2 K, both in bulk [122] and in SOI n-MOSFETs [123]. The observed changes strongly depend on the biasing conditions during 4.2 K stress. An example is given in Fig. 60: for symmetrical stress conditions (V_{GS}=V_{DS}), a reduction of V_T and an increase of the maximum transconductance has been found for bulk n-MOSFETs, opposite to the high-temperature degradation behaviour. These effects are related to the hot-carrier related forced depletion layer formation mechanism explained in the previous section. Both trapping and hot-carrier assisted ionization change the depletion charge near the drain during stress, resulting in a reduction of it.

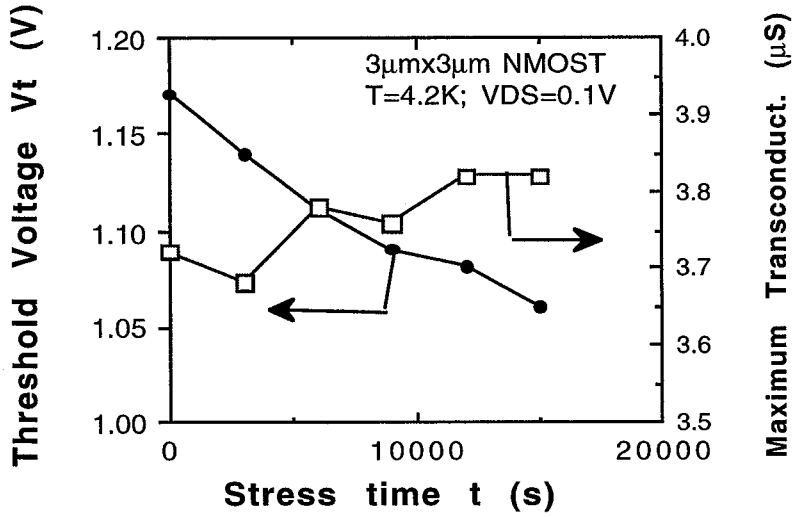

Fig. 60: Degradation of the threshold voltage and of the maximum transconductance of a stressed n-MOSFET at 4.2 K, as a function of stress time. W/L=3/3 and during stress: V_{GS}=2.5 V and V_{DS}=5 V. (after Simoen and Claeys [122]).

An expected increase in V_T and a reduction of g_{mmax} is observed for strongly asymmetrical stresses, i.e. with V_{DS} >> V_{GS} [122]. The output curves are degraded as well, in the pre-kink region of Fig. 61, whereby the kink is larger and starts for lower V_{DS} after stress. This is explained by the HC-stress-induced increase in the substrate

current noted in Fig. 61 right and by the $\sqrt{I_B}$ dependence of the kink amplitude. From the universal $I_B/I_D(V_{DS}-V_{DSAT})$ plot at 4.2 K, it is concluded that the electron mean free path λ_e has reduced from 9.3 nm (pre-stress) to 7.1 nm after stress. This could be related to the enhanced Coulombic scattering by the trapped charge, both in the substrate and in the oxide/interface [122]. A similar result is obtained for p-MOSFETs stressed at 4.2 K, with in this case a λ_h-reduction from 4.3 nm to 3.1 nm [124].

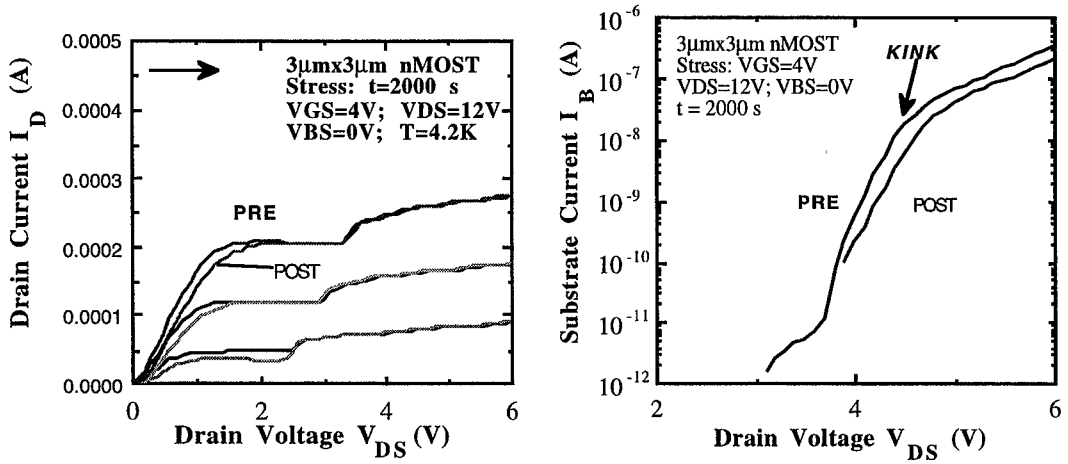

Fig. 61: Degradation of the 4.2 K output characteristics (left) and substrate current I_B-V_{DS} at V_{GS}=5 V and V_{BS}=0 V (right) of a stressed 3µm x 3 µm nMOSFET. Stress was for 2000 s with V_{DS}=12 V and V_{GS}=4 V. (after Simoen and Claeys [122]).

Down scaling Si technologies and low temperature operation generally increase HC degradation effects. The combination of both is expected to pose serious reliability problems. Therefore, several techniques of hardening the interface have been intensively explored. Beside a reduction of the supply voltage, other more technological ways have been proposed to reduce HC phenomena. One fortuitous circumstance for down scaling is that the gate oxide thickness reduction leads to an increased lifetime, both at room temperature and at 77 K . This is shown in Fig. 62, giving the device lifetime at 300 K and 77 K for 15.2 and 5.2 nm oxides, respectively [125]. The improvement is related to the fact that the injection and therefore the trapping efficiency drops significantly for thinner oxides.

Another way to make thin oxides more robust against hot-carrier injection is the use of so-called nitrided (N_2O), or reoxidized nitrided oxides (ONO). In most cases, both at room temperature and in the liquid nitrogen temperature range, an improvement has been noted [126-128]. This is illustrated in Figs 63a (n-channel) and 63b (p-channel MOSFETs). The interface hardness increase is 4 to 10 times, with an optimal N_2O anneal at around 2% nitrogen incorporation at the Si-SiO_2 interface [128]. However, the presence of an increased density of electron traps related to the incorporation of H, inherent for NH_3, may give rise to some additional problems [127]. It has for instance been demonstrated that the gate-induced drain (GIDL) leakage current increases more severely after 77 K stress for an ONO device compared with a standard SiO_2 n-MOSFET.

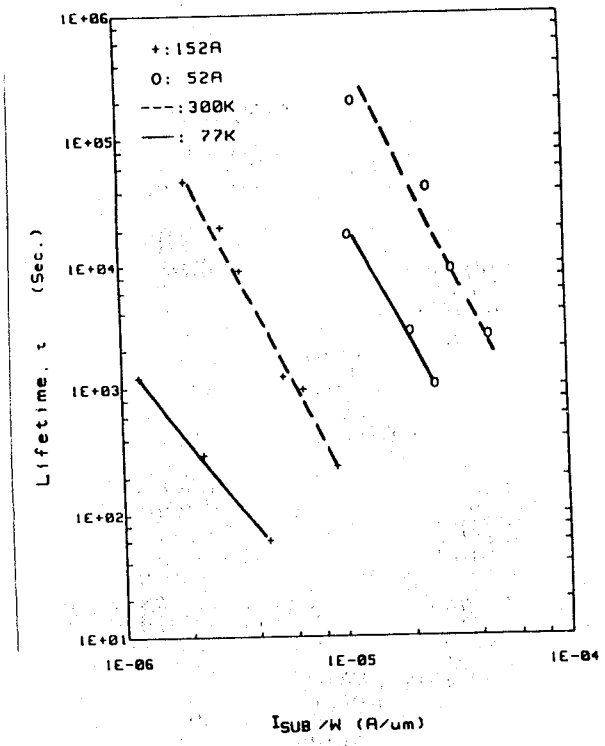

Fig. 62: Device lifetime τ versus substrate current per unit width I_B/W for 5.2 and 15.2 nm gate oxide n-MOSFETs at 77 and 300 K. W is the channel width and L_{eff}=0.75 μm. (after Ong et. [125]).

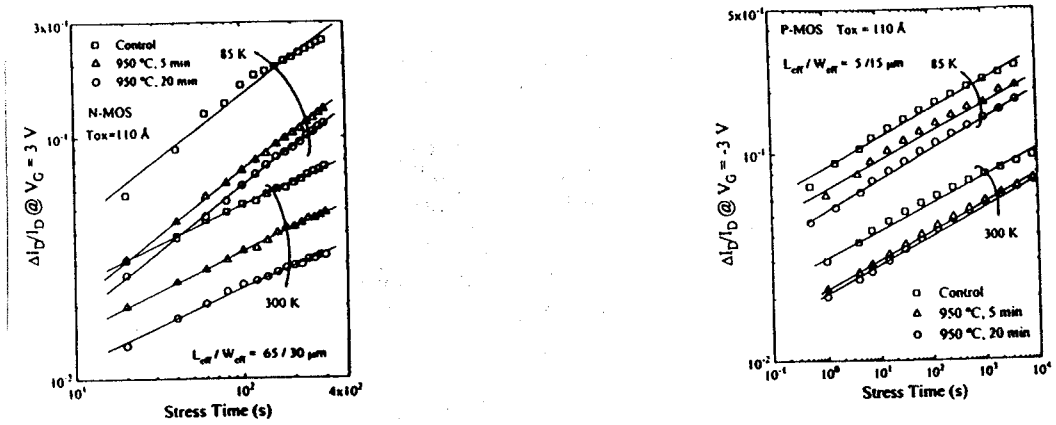

Fig. 63: Percent increase in the drain current for devices stressed around maximum I_B at both 300 K and 85 for n-(a) and p-MOSFETs (b) with ONO and standard SiO_2 (control) gate oxides. (after Ma et al. [128]).

For submicron technologies, the use of LDDs has considerably increased the reliability and lifetime, by lowering the maximum field and hence the avalanching near the drain. This has been successfully demonstrated for 77 K operation as well [113,117,129-132]. The main degradation mechanism is the electron trapping in the spacer oxides, which enhances the parasitic source-drain series resistance. Due to carrier freeze-out at 77 K, the impact of this phenomenon is larger than at room temperature [129-132]. There

exists no simple relationship between for instance the substrate current as a monitor and the resulting HC damage of LDD n-MOSFETs [130-131]. As a consequence, the maximum damage has not been observed to correspond with maximum I_B and shows no straightforward dependence on the LDD design, i.e. the doping density. Figure 64 shows that the device lifetime of LDD n-MOSFETs has a thermally activated behaviour, corresponding with different activation energies, depending on the stress conditions [117].

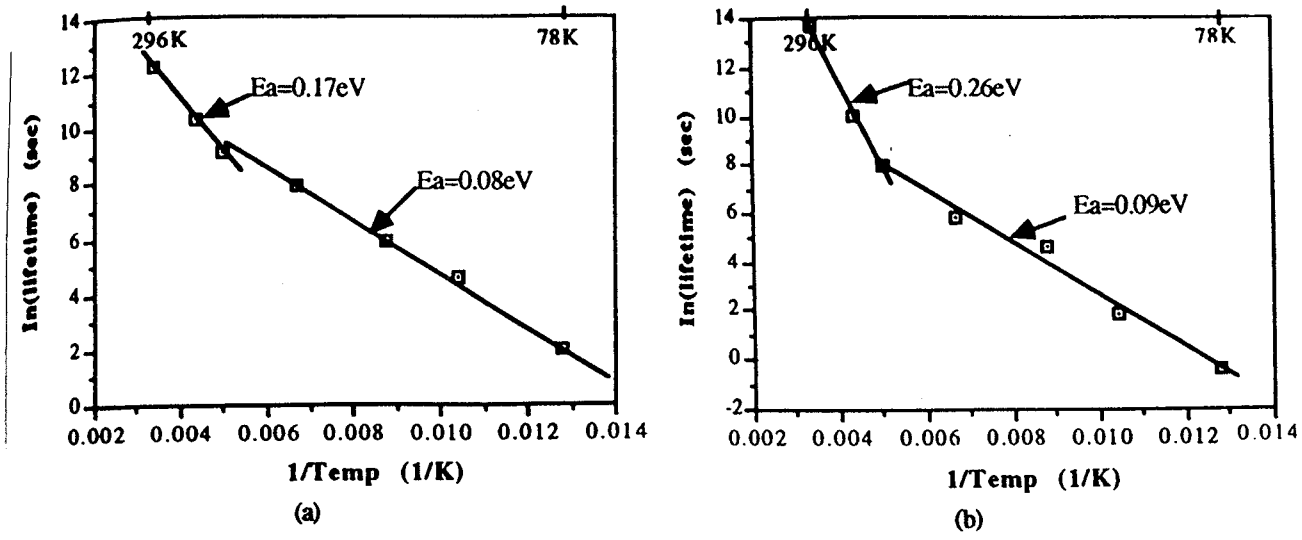

Fig. 64: Device lifetime versus 1/T. The device was stressed (a) at V_{GS} at I_{Bmax} and (b) $V_{GS}=V_{DS}$ with $V_{DS}=7$ V. W/L=11/0.75. (after Song et al. [117]).

Figure 65 points out that maximum V_{GS} stress yields a stronger degradation than I_{Bmax} stress, whereby a clearly larger degradation is observed at 78 K. Although the g_m reduction follows a classical type of power law, the exponent is typically much smaller, compared with the values of 0.4-0.6 found for non-LDD devices [111-112] and thus indicative for the creation of interface traps. The temperature dependence of the degradation of the series resistance, due to HC stress, is illustrated in Fig. 66. It can be concluded that carrier freeze-out in the LDD regions pronounces the stress-induced increase of R_{SD} [117].

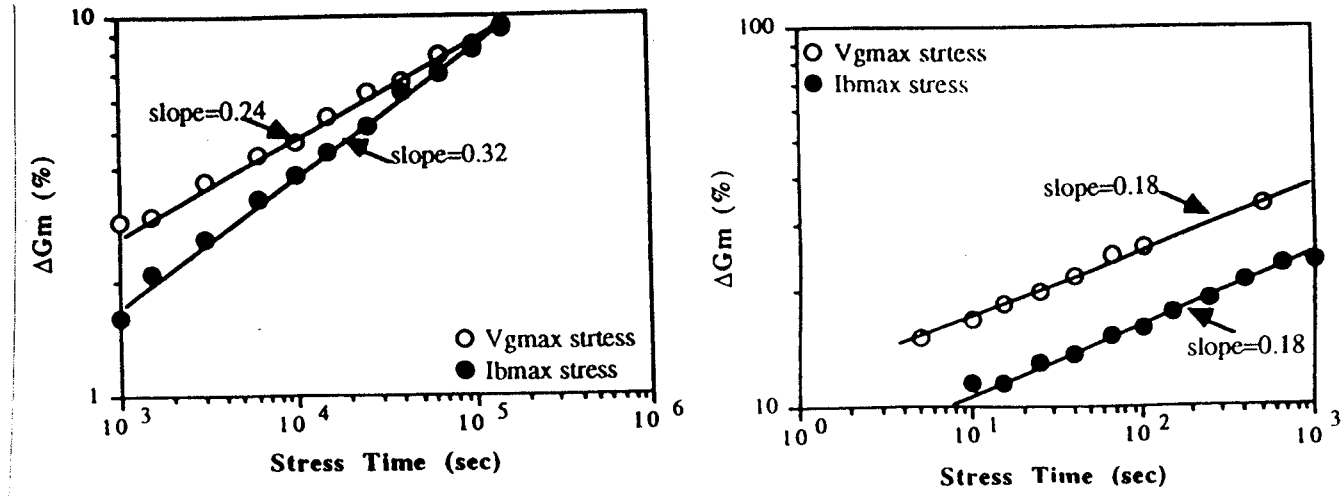

Fig. 65: Δg_m versus stress time. The n-MOSFETs were stressed at (a) 296 K and (b) 78 K with $V_{DS}=7$ V. W/L=11/0.75. (after Song et al. [117]).

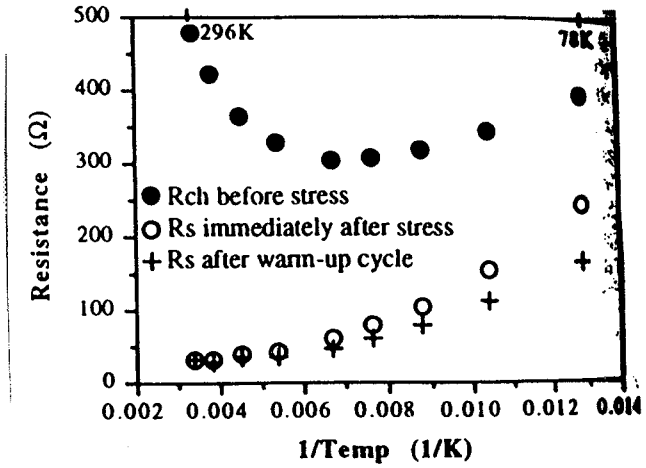

Fig. 66: Channel resistance (R_{chan}) and hot carrier induced series resistance (R_{SD}) versus 1/T. The n-MOSFET was stressed at 78 K with $V_{GS}=V_{DS}=7$ V. W/L=11/0.75. (after Song et al.[117]).

It has to be remarked that the LDD n-MOSFET lifetime versus the inverse drain voltage shows a two-slope (two degradation mechanisms) behaviour at 77 K (Fig. 67) [133], emphasising that one needs to stress the devices near the desired operation voltage for lifetime estimation at 77 K

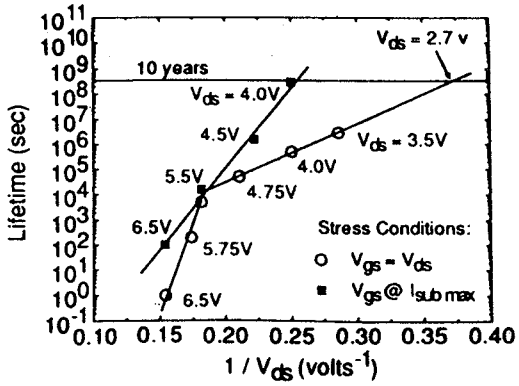

Fig. 67: Lifetime versus $1/V_{DS}$ for 25 μm x 1 μm n-MOSFETs at 77 K. A 10% degradation in maximum transconductance is used to define the device lifetime. For all drain biases, electron injection ($V_{GS}=V_{DS}$) leads to a shorter lifetime. A two slope behaviour is evident for this stress condition. (after Hwang et al. [133]).

In many applications, the devices and circuits are operated under switching or ac conditions. For practical purposes it is therefore important to assess the HC degradation for ac stressing, since one can not simply extrapolate dc results to estimate a circuit's lifetime. From the available results of ac stressing in the liquid nitrogen temperature range, it has been concluded that while dc stressing may impact strongly on the transistor performance, circuits are less prone to HC degradation [134-135].

It should finally be remarked that because of its thermally activated nature, electromigration is not a reliability problem for 77 K operation.

Besides the strongly non-homogeneous HC injection, the gate oxide can also be degredad by so-called homogeneous injection from the substrate (SHE). At higher field strengths in the dielectric, injection of hot carriers across the interface barrier occurs through Fowler-Nordheim (FN) tunneling. Injected charge drifts in the oxide field towards one of the electrodes. Oxide degradation occurs through carrier trapping by pre-existing traps, by the creation of new oxide traps for sufficiently energetic carriers and by charge multiplication (avalanching).

The charge trapping in an oxide is generally described by the following first-order model [136-138]. Assuming a single-trap species of cross section σ and density per unit area N_T, the trapped charge density as a function of time is given by:

$$N(t) = N_T\,[1-\exp(-\sigma N_{inj})] \tag{45}$$

where the injected density is given in terms of the injected current density J_{inj}:

$$N_{inj}(t) = \frac{1}{q}\int_0^t J_{inj}(t')dt' \tag{46}$$

The trapping of the electron flux is spatially uniform over the oxide thickness t_{ox}, as long as $\sigma N_T \ll 1$. The resultant shift in threshold (or flat-band) voltage is then given by:

$$\Delta V_T = \frac{q}{2}\frac{N_T}{C_{ox}}\,[1-\exp(-\sigma N_{inj})] \tag{47}$$

Hereby is the measured gate current I_G a good measure of the injected flux, since:

$$I_G = I_{inj}\,[1-\sigma N_T \exp(-\sigma N_{inj})] \approx I_{inj} \tag{48}$$

From eq. (48) follows that the change in I_G (or I_{inj}) with time is a good approximation for the trapping efficiency $(I_{inj}-I_G)/I_{inj}$ of the gate insulator [139].

Electron trapping following substrate hot electron injection (SHE) at low oxide fields and low temperatures in SiO_2 has been investigated since the late 70ties [139-141]. From these studies, an increase of the trapping efficiency is found, as shown in Fig. 68 [141]. This depends on the processing conditions: H_2 annealed oxides show a lower trapping efficiency than non-annealed ones [140]. There is furthermore a power law dependence on the oxide thickness, as illustrated in Fig. 69. Most likely, pre-existing neutral or repulsive trapping centres (probably water or OH-related species) with an electron capture cross section in the range 2×10^{-18} cm^2 (30 K) to 4×10^{-18} cm^2 (300 K) are responsible for the observed trapping at low temperature [140]. The orders of magnitude increase in the efficiency upon cooling is thought to be related to the fact that the energetic position of these traps is rather shallow: 2 activation energies of 23 and 4 meV have been determined [140], indicating that at higher temperatures, thermal re-emission reduces significantly the number of trapped electrons.

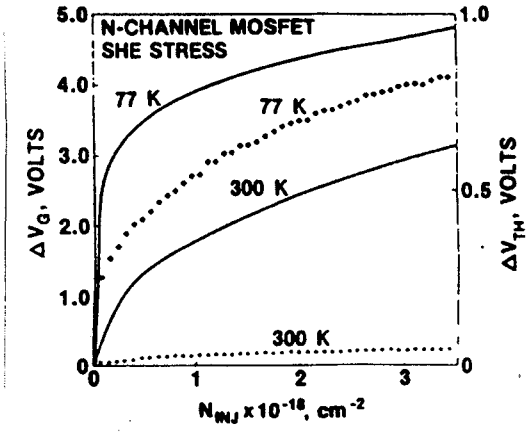

Fig. 68: voltage shift ΔV_G (solid lines) and threshold voltage shift ΔV_T (dotted lines), during SHE stress for two temperatures. (after Gildenblat et al. [141]).

Beside the trapping of electrons by already existing "background" centres, new traps can be created upon the injection of energetic electrons (or holes) in the oxide. These new traps reside either at the interface or in the bulk of the dielectric. The trap creation in both the bulk of the oxide and at its interfaces depends on the presence of hot electrons in the oxide [142-143]. This has been derived from the fact that the created trap distribution as a function of the field at the injecting electrode closely follows the hot electron energy distribution. A threshold energy for trap creation by hot electrons of 2.3 eV has been found, which corresponds to a minimum oxide field of ≈1.5 MV/cm, for oxides thicker than ≥10 nm [142-143]. Another important finding is that the creation of new interface and bulk oxide traps closely follows the amount of trapped electrons or holes during SHI (or FN stress) [144]. Chen et al. [145] have proposed a model for the creation of electron traps, involving the recombination of an electron-hole pair, which leads to the breaking of Si-O or Si-H bonds and the creation of new trap species. The corresponding electron cross section of the generated neutral traps is in the range $5x10^{-16}$ cm^2, a value observed down to 77 K. A similar picture, involving the trapping of a hole, followed by the trapping of an electron has been suggested as an important interface-state generation mechanism.

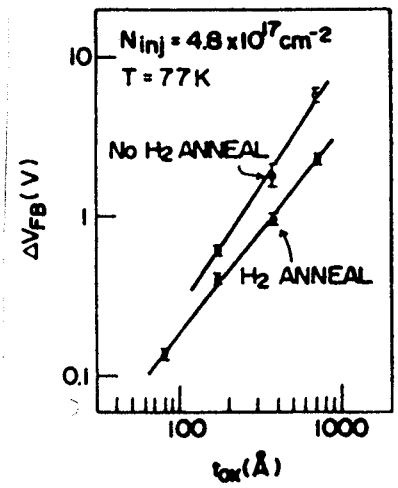

Fig. 69: Dependence of flat-band voltage shift on oxide thickness for a given N_{inj}. T=77 K. (after Itsumi et al. [140]).

Fundamental studies involving the vacuum emission of hot electrons from thin oxides demonstrate that the hot electron distribution is hardly affected by the temperature [144]. However, for temperatures below ≈150 K, trap creation by SHE is suppressed [142], particular for higher E_{OX} in the FN tunnelling regime. This is most likely due to the fact that the trap generation not only involves hole/electron trapping causing bond breaking, but probably some defect reconfiguration, or diffusive motion of a H species, which requires some thermal energy, i.e. following an Arrhenius type of law with temperature.

SHI of hot holes at 77 K has also been studied in some detail and compared with hole-trapping induced by ^{60}Co γ-irradiation [146]. First of all, it is noted that the injection of holes at 77 K is less efficient than at 300 K, due to a phenomenon called back-tunnelling, which becomes more pronounced at cryogenic temperature. On the other hand, the trapping efficiency increases roughly by a factor 3 or more at 77 K and increases for lower E_{OX} as illustrated in Fig. 70. A trapping efficiency close to 1 is derived for low E_{OX} from extrapolating the data in this figure. Typical cross sections are in the range $4x10^{-14}$ cm^2 (300 K) and $\approx 10^{-13}$ cm^2 at 77 K. The increase in trapping efficiency is thus nearly completely explained by the increase in σ upon cooling. It is therefore believed that - at least for hole trapping - no shallow traps are responsible [146]. Furthermore, there is a strong similarity between the hole trapping behaviour and the subsequent formation of interface traps at low temperature, confirming earlier results on D_{it} formation upon electron injection [146]. A close-to-linear relationship exists between the injected charge and the increase in the density of interface traps D_{it}, both at 295 and at 77 K (Fig. 71). Furthermore, a strong E_{OX} dependence is noted for the interface state trap generation efficiency as well, whereby for fields above 4 MV/cm little difference is found between room temperature and 77 K [146], giving rise to values in the range 0.01 eV^{-1} per injected hole.

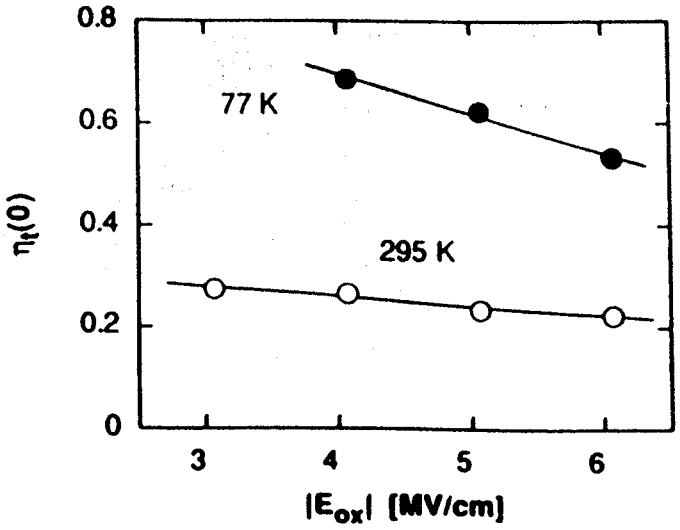

Fig. 70: Initial trapping efficiency as a function of oxide field, for trapping at both 295 and 77 K. A linear field dependence has been assumed. (after Van den bosch et al. [146]).

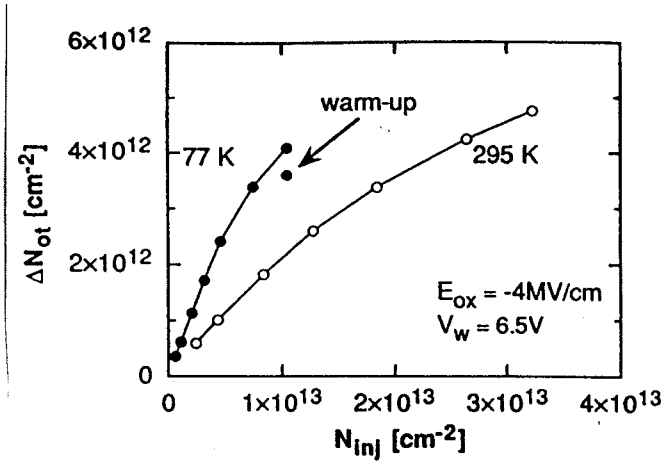

Fig. 71: Interface trap generation versus injected fluence for two identical injection experiments at 295 and 77 K, respectively. (after Van den bosch et al. [146]).

Studying the density of interface traps as a function of the anneal temperature, after a hole-injection experiment at 85 K, leads to the following conclusions. During the isochronal anneal, few additional traps are formed at T<200 K (Fig. 72). Furthermore, the creation of additional traps strongly depends on the polarity of the oxide field, similar as for 77 K γ-irradiated MOS structures [146]: for positive E_{OX}, a significant increase in D_{it} is noted in Fig. 70. At 77 K, SHI is about an order of magnitude more efficient in the creation of interface traps than irradiation.

The results of Fig. 72 suggest that there are probably two fundamental interface-state generation mechanisms, following hot-hole injection. These may be related to the observation that there are two kinds of trapped holes after injection [147-148]: "near-interfacial trapped holes", lying in a distance of 2 to 7 nm from the interface and "interfacial trapped holes" lying within 1.5 nm from the interface. The latter are believed to become "prompt" interface states, upon the capture of an electron [147-148]. As will be discussed in more detail in the next paragraph, several models have been proposed for the trapped-hole related interface-state formation, involving H^+ and neutral H species, which may be relevant depending on the gate oxidation technology, the oxide field and the injection conditions, and the temperature.

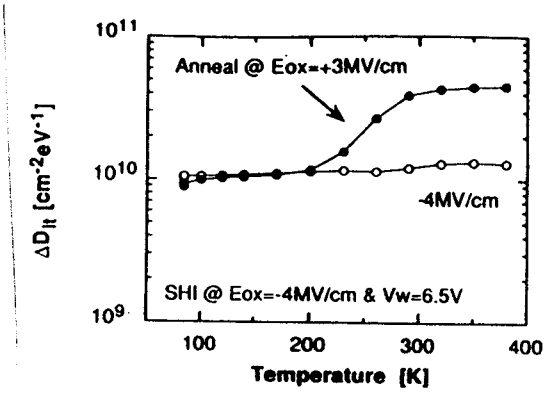

Fig. 72: Cumulative interface trap density as a function of anneal temperature, after SHI at 85 K (a fixed injection oxide field of -4 MV/cm), for both anneal oxide field polarities. The reference level is the density before SHI. (after Van den bosch et al. [146]).

High-field tunnelling (FN) injection yields at first sight an opposite result as low-field SHE injection: the trapping efficiency reduces upon cooling [142-143,149-150]. This is illustrated in Fig. 73 for the range 4.2 K to 373 K [142], showing that the electron trapping efficiency drops upon cooling, for sufficiently large E_{OX}. This drop is significant between 300 K and 77 K and shows little variation below that. Furthermore, the observed reduction of electron trapping correlates well with the retardation of MOS breakdown upon cooling [149-150], as shown in Fig. 74. From this figure follows that at least two activation energies can be defined, if one accepts an Arrhenius law for the charge density to breakdown, of the form:

$$N_{inj}^{(BD)} \propto \exp(\frac{E_A}{kT}) \qquad (49)$$

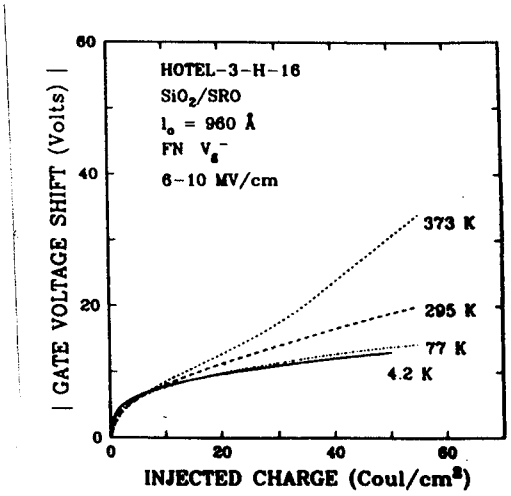

Fig. 73: Magnitude of the gate voltage shift due to trapped electrons as a function of injected charge at various temperatures from 4.2 K to 373 K on MOSFETs with a 96 nm gate oxide. Electrons were injected and sensed by constant-current FN tunnelling . (after DiMaria and Stasiak [142]).

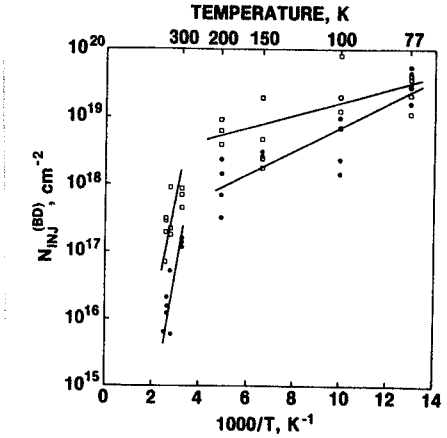

Fig. 74: Inverse temperature dependence of the $N_{inj}^{(BD)}$ for Al gate MOS capacitors fabricated on p-type substrates (closed circles) and n-type substrates (o). (after Huang et al. [151]).

Relevant literature data are summarised in Table I. It can be seen that an one-order of magnitude reduction is observed for E_A at low temperatures. From these data, it is clear that if the Arrhenius approximation is followed, one can not simply extrapolate the high-temperature data, to describe the gate oxide breakdown in the liquid-nitrogen temperature range or below. This activated behaviour also strongly supports the trap-generation breakdown model and is in contrast with models assuming impact ionization as the main cause [149]. Further support comes from the role of hydrogen in the TDDB of gate oxides: while background trapping can improve upon H-incorporation (see Fig. 69), trap creation and breakdown are enhanced.

Table I: Literature data for the activation energy, defined in eq. (49) of gate oxide breakdown.
*Based on the creation of interface states after FN tunnelling flat-band shift.

Gate Material	T_{OX} (nm)	Temp. range	E_A (eV)	Refs
polysilicon	3-30	77,300 K	0.017	Harari [150]
polysilicon	10	77,300 K	0.022	Modelli &Ricco [149]
Al	20	77-200	0.035 (p) 0.023 (n)	Huang et al. [151]
		300-393	0.39 (p) 0.35 (n)	
Al	20	180-300	0.070 (p)	Sakashita et al.* [152]
		77-180	0.005	

Several extensive studies of the oxide and interface trap creation due to FN injection mainly at 77 K can be found in the literature [142-143]. The global picture, derived from these studies as established by DiMaria and summarised in Fig. 75, resolves the apparent controversy between the low-field and the high-field trapping characteristics at low temperature. There are at least three trapping components to be considered. First, the background electron trapping is uniform across the oxide thickness and is related to energetically deep traps, which are water or OH related and have a fairly low cross section for electron trapping. This component hardly changes with temperature. A second background component (related to pre-existing traps) is due to shallow traps, which are believed to reside close to the cathode. Chemically speaking, they are thought to be related to a deficiency of oxygen at the Si-SiO_2 interface (O-vacancies). As shown above, this trapping becomes only important at low temperature, because no thermal re-emission from the shallow levels happens. In other words, trapped electrons are frozen there. This explains the more efficient electron trapping observed for SHI at low fields. Finally, the trap creation close to or at the interfaces is suppressed strongly below $\leq$150 K. This is most likely because of the thermally activated nature of some of the steps involved.

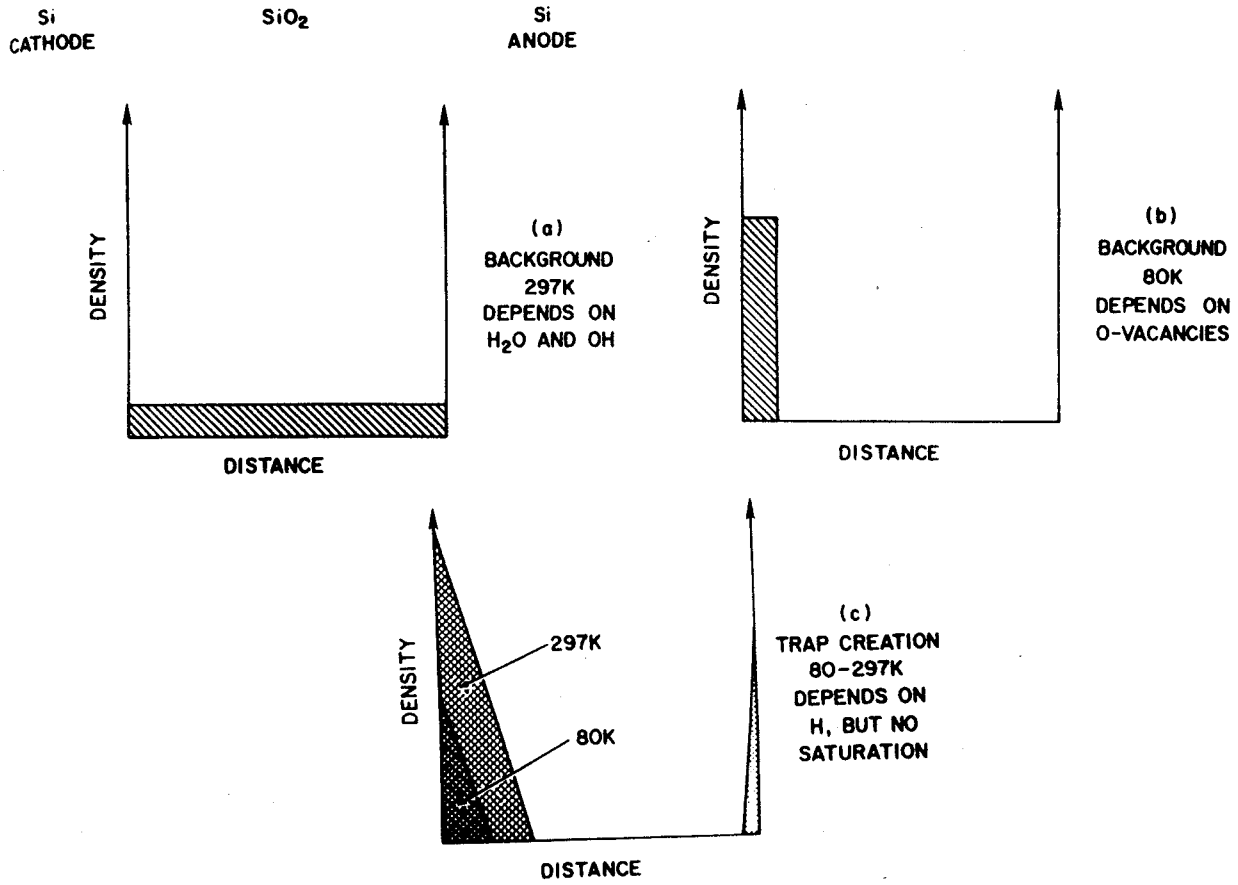

Fig. 75: Schematically representation of spatial density of various components of trapped charge build-up in SiO_2 under electron injection conditions from the cathode-oxide interface. (after DiMaria [143]).

BJTs

Down scaling of modern BJTs is achieved by a shrinking of the device dimensions, which is accompanied by an increase of the doping in the base region. This results in increased electrical fields at the base-emitter junction, when a reverse bias is applied. This can occur during the operation of BiCMOS circuitry [153], which is a concern, due to the occurrence of avalanching and the subsequent injection of hot carriers in the passivation oxides covering the base-emitter junction surface. Therefore, constant-current stress studies have been applied to BJTs, resulting into the following model for the HC stress increase of the base current at room temperature [153]:

$$\Delta I_B = D\, J_C^a\, I_R^b\, t^c \qquad (50)$$

with t the stress time, J_C the collector current density, I_R the reverse-stress current and D, a, b and c semi-empirical constants.

The same model applies for the description of the degradation at liquid nitrogen temperatures (LNT) [154], whereby the ΔI_B at 110 K is about one decade larger than at 300 K, for the same stressing current. This is shown in Fig. 76. The time exponent c is ≈0.5 at 300 K and increases to 0.58 at 110 K. However, the extrapolated degradation of a BiCMOS inverter after 10 years of operation is a factor two better at 110 K. This is due to the much smaller current gain at 110 K [154]. The role of hot hole injection in the degradation of advanced BJTs both at room temperature and at 77 K has been pointed out by Neugroschel et al. [155]. The primary hot holes, rather than the secondary hot holes generated by these primary hot holes or thermally generated, are responsible for the degradation of the common-emitter forward current gain of submicron npn bipolar transistors.

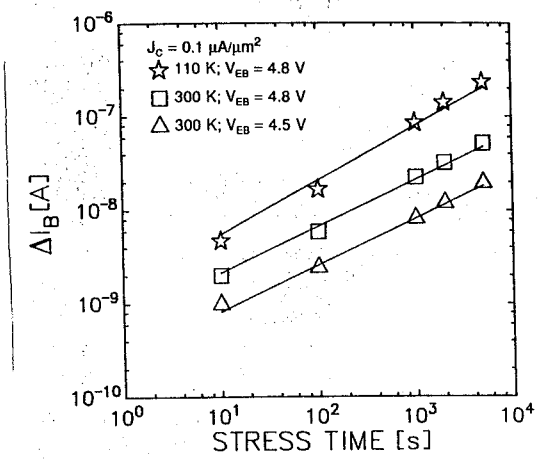

Fig.76: Degradation of I_B for different stress conditions. The reverse-current was the same for the 110 K, V_{EB}=4.8 V and the 300 K, V_{EB}=4.5 V stresses. ΔI_B at 110 K is about four times larger than at the room temperature for the same reverse voltage stress, and about 10 times larger for the same reverse stress current. (after Burnett and Hu [154]).

2.5. Self-Heating

It should finally be mentioned that for sufficiently large currents, self-heating of a Si device can take place at cryogenic temperatures [156-157]. This results from the fact that on the one hand the thermal conductivity of Si reduces in the liquid-helium temperature range, so that the heat capacitance drops drastically upon cooling. As a result, the lattice temperature may become much larger than the ambient temperature due to Joule heating, for sufficiently large currents. This gives rise to hysteresis in the I-V curves, of resistors, MOSFETs...Additionally, it generates a negative output conductance for MOSFETs operated at cryogenic temperature, due to the temperature dependence of the effective mobility. The associated problems are more pronounced for SOI devices compared with bulk. On the other hand, the current flowing through a co-integrated Si resistor can be used as a local temperature probe, for nearby silicon components, provided a proper calibration has been performed [157-158].

Chapter 3

RADIATION EFFECTS AT CRYOGENIC TEMPERATURES

The space radiation environment is generally composed of high energetic particles (protons, electrons, ions,...) and photons [159-160]. Upon its path through the different layers of an electronic component (metal, passivation dielectric, gate dielectric, silicon substrate,...), the energetic particle (photon) looses energy according to a number of mechanisms. With respect to performance degradation, one can distinguish roughly between ionization damage, displacement damage and single particle (or event) effects, which may have a transient (temporary) or a more permanent (hard) nature. This results in a number of degradation effects, like charge trapping, the creation of interface traps at the Si-SiO_2 interface, a reduction of the mobility, single event upset (SEU) and latch-up in CMOS (SEL). The main displacement damage degradation effects can be summarised as: increased resistivity and even type inversion for high-resistivity Si nuclear-radiation detector material, increased dark (leakage) current in junction devices and CCDs, reduced minority carrier lifetime in bipolar devices (solar cells), etc.

In case of ionization damage in oxides, a long-term transient behaviour is typically observed at room temperature, so that one can distinguish between prompt effects and more permanent degradation. The same applies to some extent also for bulk (displacement) damage. Since most of the underlying physical and chemical processes are thermally activated (diffusion of species, recombination or pairing,...) this transient annealing effect can be enhanced by (temporarily) operating the device at elevated temperatures (e.g. 100 ^{o}C). Low temperature operation on the other hand, mostly aggravates the radiation effects, explaining the emphasis which has been put on hardening efforts for such applications as focal plane array read-outs, and scientific CCDs.

In order to guarantee a successful operation for the expected time in a radiation environment, in many cases special measures have to be taken to make the components more resistant (radiation tolerant or hardened). In the following, several measures will be discussed for hardening MOS based technologies, especially for low temperature applications. Beside technological changes, one can also adapt the design, generally at the expense of the integration density.

3.1. Basic Mechanisms at Cryogenic Temperatures

This sections discusses some fundamental aspects related to both ionization damage and displacements damage in silicon in order to get a better insight on the possible influence by going over to a cryogenic operation of the components. The impact of the radiation on the device performances is treated in more detail in the next section.

3.1.1. Ionization damage

Radiation damage in Si-based components is of primary concern for the oxide properties. The response of a radiation-hard SiO_2 insulator to a short radiation pulse is dominated by the creation of free electron-hole pairs and their transport through the oxide. It is assumed hereby that the initial creation of pairs only depends on the total ionization energy deposited and not on the nature of the incident particle. Due to the presence of the oxide field, the created electrons and holes will be immediately separated. While the transport of the highly-mobile electrons which escape initial recombination is nearly instantaneous (they are swept by the oxide field in typically a few ps even at cryogenic temperatures), the low-mobility holes have to migrate through the oxide, as depicted in Fig. 77 [161]. The fraction of holes surviving the initial recombination (hole yield $f_y(E,E_{ox})$) strongly depends on the incident energy E, particle and the field E_{ox} [161-163], as shown in Fig. 78 for 80 K irradiation. This yields a positive charge in the

dielectric which leads to an initial flatband shift in the MOS structure. The latter is given by [162]:

$$\Delta V_{FB} = \Delta V_{ot}(t=0) = -3.23 \times 10^{7}\, f_y(E, E_{ox}) \frac{D_\phi\, t_{ox}^2}{I_{eh}} \qquad (51)$$

with D_ϕ the radiation dose in rads(SiO_2) and I_{eh} the mean ionization energy. A uniform radiation and hole generation across the thickness of the oxide is assumed in writing eq. 51 [161-162].

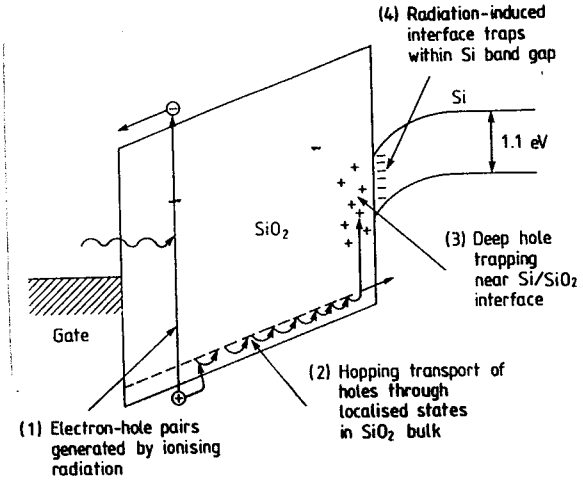

Fig. 77: A schematic representation of basic radiation effects in SiO_2 (after Oldham et al. [161]).

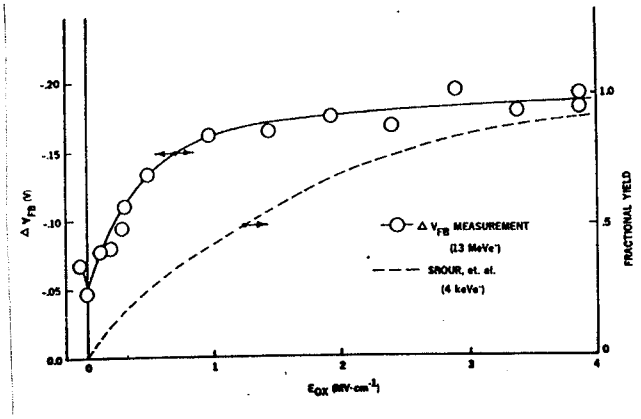

Fig. 78: Flatband voltage shift, ΔV_{FB}, normalized to 2×10^3 rad(SiO_2) per pulse in MOS capacitors irradiated at 80 K as a function of the electric field, E_{OX}, in the oxide layer. The corresponding hole yield expressed as a fraction of the calculated maximum based on 18 eV/pair is also shown (after Boesch Jr and McGarrity [162]).

After creation and separation by the field, the remaining holes undergo a highly time-dispersive field- and temperature-dependent transport towards the negative interface. This leads to the short-term recovery of the flat-band voltage shift, depicted in Fig. 79, provided that the hole-trapping efficiency is smaller than 50 %, which is the case for most thermal oxides. It is for instance quoted that in a hard oxide 50 % of the holes will reach the interface in about 10 μs in a 30 nm oxide, irradiated with E_{OX}=1MV/cm at room temperature [163]. In a hard oxide, most of the holes will leave the oxide and only a few percent will remain trapped near the interface. This results in a significant recovery shortly after the end of the irradiation. For soft oxides on the other hand, a large fraction of holes

gets trapped in pre-existing traps near the negative interface, so that the short-term recovery is only partial and significant long-term annealing will follow (Fig. 79). The holes are trapped in levels typically some 0.3-0.4 eV above the oxide valence band. The time-dispersive hole transport is strongly temperature and E_{ox} dependent and can be described by [163]:

$$t_{1/2} = t^{0}_{1/2} \exp\left(\frac{E_{ox}(E_{ox})}{kT}\right) \qquad (52a)$$

$$E_{ox}(E_{ox}) = E^{0}_{ox} - b_{ox}E_{ox} \qquad (52b)$$

with E_{ox} the field dependent activation energy for the hole transport. In eq. (52a) is $t_{1/2}$ the time required for half of the ΔV_{ot} recovery to occur. Below 100 K, the activated behaviour implies that the holes are essentially immobilised for the first few thousands of seconds, explaining the substantial ΔV_{ot} after cryogenic irradiations.

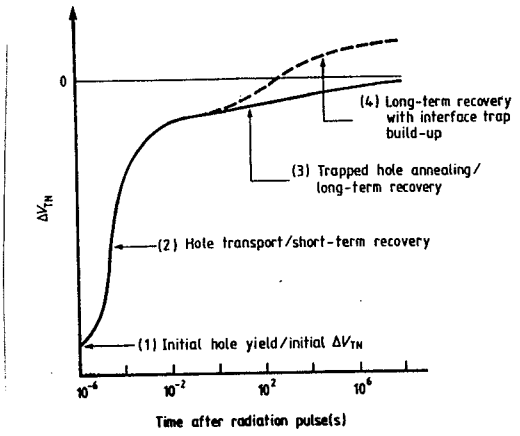

Fig. 79: Time-dependent threshold voltage recovery of n-channel MOSFETs. The labeled regions correspond to Fig. 77 (after Oldham et al. [161]).

Finally, the holes trapped near the negative interface undergo a long-term annealing behaviour which occurs with an ln t dependence (Fig. 79). Different mechanisms have been proposed, which are based on either tunneling of electrons from the substrate followed by recombination or compensation, or tunneling of the holes out of the oxide. This long-term hole removal is generally accompanied by the formation of interface traps (N_{it}). Since the charge associated with the N_{it} formation is opposite to the trapped hole charge, this will lead to the rebound phenomenon indicated in Fig. 79 (n-channel devices), whereby the long-term annealed threshold voltage becomes more positive than the pre-rad value. While for soft oxides, the interface state formation can be used as a kind of in situ hardening effect compensating the positive trapped hole charge, rebound is a highly undesirable effect for standard MOS devices. At cryogenic temperature, the N_{it} formation is strongly suppressed, as will be discussed in the next section, so that there is no rebound problem there [161,163]. It should finally be remarked that the initial flatband voltage shift through hole charging is in first instance proportional to the radiation dose D_ϕ, as expressed in eq. (51). This is confirmed by the experimental results of Fig. 80 obtained at 80 K for different oxide types [162]. Note that in this figure, no difference is observed between room temperature hard and soft oxides, indicating that hardening for cryogenic operation requires other measures. Only at high total dose, a saturation behaviour is observed, which will be discussed in more detail in the next section.

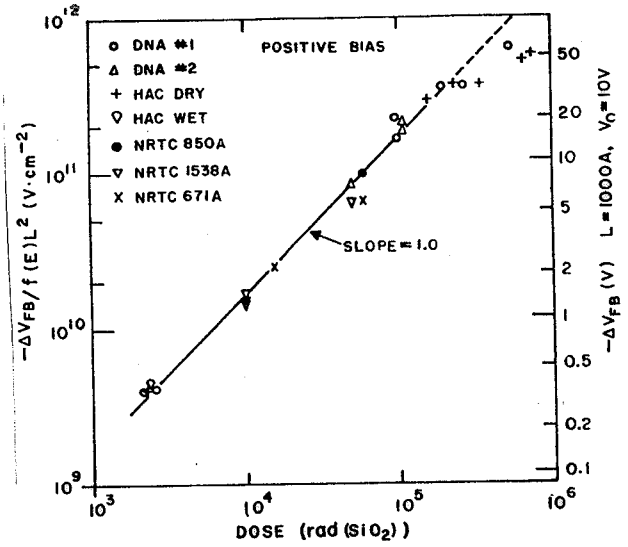

Fig. 80: Flatband voltage shift, ΔV_{FB}, normalized to field-dependent charge yield, f_y and oxide thickness t_{ox}, in various MOS capacitors irradiated at 80 K as a function of total dose delivered to the SiO_2. The equivalent ΔV_{FB} for a capacitor under 10 V bias is also shown (after Boesch Jr. and McGarrity[162]).

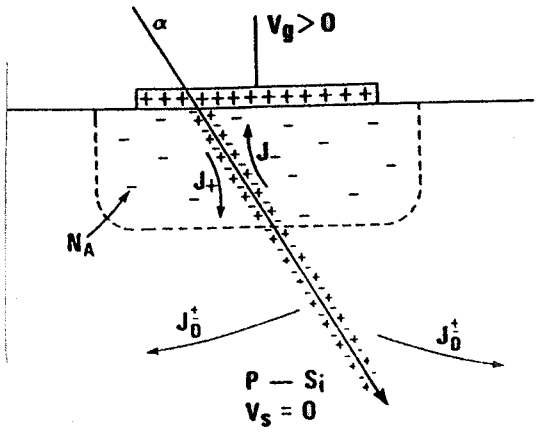

Fig. 81:. Schematic illustration of impinging ionised particles on the active device area, indicating single event upsets (SEU). V_{GS} and V_{BS} are the gate and substrate bias, respectively (after McLean and Oldham [165]).

For bulk silicon bipolar junction devices, some specific degradation mechanisms are induced by ionisation damage through a charged particle or photon. Of particular concern is the so-called single event upset (SEU), which has become a major reliability issue for dynamic NMOS and static CMOS memories. The basic mechanism is illustrated in Fig. 81 [164-166]. A single high energy particle can strike a critical node of the device, leaving behind an ionised track passing through the device well area or storage capacitor. Depending on the operation bias, the well is inverted or depleted. The created electrons will be swept towards the positive node, and the positive charge will move away from the gate in Fig. 81. If the well (storage node) is already filled with electrons, no change of state (bit flip) will occur. However, initially empty wells may now become partially filled

with electrons. If enough electrons are collected, the well changes state and a bit flip (soft error) occurs. An important device parameter is the critical charge or number of electrons associated with the difference between the "0" and the "1" state. Depending on the used technology and design rule, typical charge packets are around 10^5-10^7 electrons. As an illustration it can be mentioned that a 5 MeV alpha-particle generates about 1.5×10^6 electron/hole pairs along its track. Device scaling strongly increases the SEU sensitivity. Similar considerations hold for high-energy ion (or radiation) induced latch-up, schematically represented in Fig. 82 [167], which is to be considered as a permanent effect.

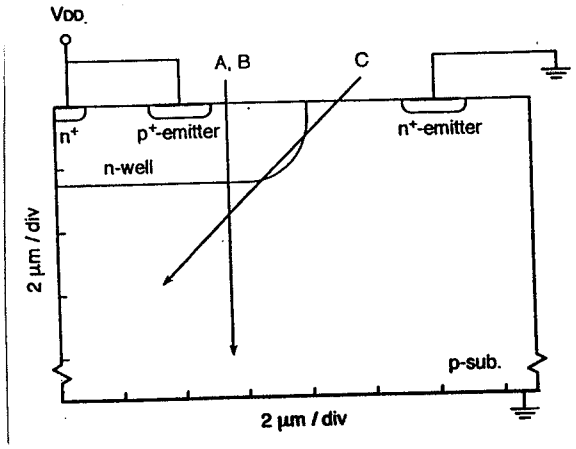

Fig. 82: Cross-sectional view of an n-well CMOS structure for two-dimensional simulation. A,B are ions impinging at 90° on the device (normal incidence) and C is a charged particle under inclined incidence (after Iwata and Ohzone [167]).

3.1.2. Displacement damage.

For high energy photons, ionization is the main energy loss mechanism, although lattice damage can also be created, for energies much larger that the Si atom binding energy (a minimum photon energy of 170 keV is required). This displacement stems from energetic back-scattered Compton electrons which form their own damage cascade. For high-energy ions, the total energy loss is also composed of an ionising and a non-ionising part (Fig. 83). The largest fraction of the deposited energy is again carried away by ionization of the material. A small part (10^{-3}), however, goes into Coulombic or elastic nuclear interactions with lattice atoms and for even higher energies non-elastic nuclear processes occur. In the latter case, the energetic particle is absorbed by a silicon nucleus, which induces the emission of energetic nucleons (alpha particles, photons) and the associated nuclear reactions/decay. In all cases, a Si atom is knocked from its lattice site, whereby the primary recoil or knock-on atom receives part of the particle energy and may cause further displacements upon its path through the lattice, resulting in damage cascades or clusters. The energy loss versus energy is depicted in Figs 84 and 85 for high-energy protons [168-169]. While the ionising energy loss is described by the LET function, the non-ionising energy loss is generally described by the NIEL factor [170], which is shown in Fig. 85 for H^+ in Si, in function of proton energy. As will be discussed later, the NIEL turns out to be proportional to the average degradation of Si devices, if the latter can be expressed through one single electrical parameter and can thus be used in practice for damage predictions [170]. A maximum ionization loss versus NIEL ratio is obtained for 10 MeV protons in Fig. 84. Note also that for energies above ≈100 MeV the NIEL for protons is nearly independent on the particle energy. This is related to the dominance of the nuclear interactions, which show an essentially constant interaction cross section with energy, for that range.

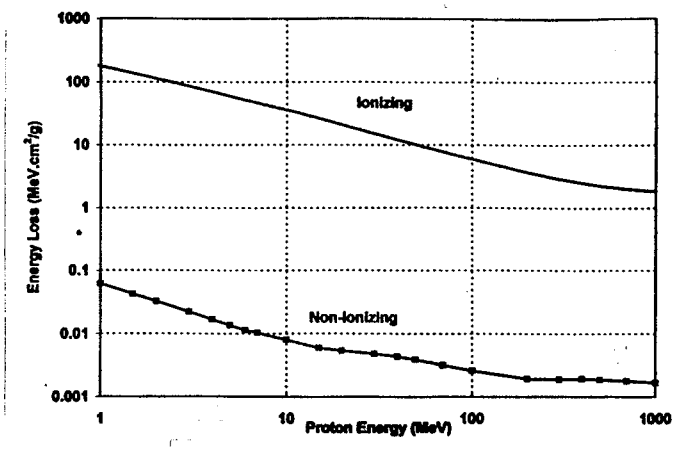

Fig. 83: Non ionising energy loss (NIEL) and ionising energy loss (i.e. LET), calculated by TRIM, versus proton energy (after Hopkinson, Dale and Marshall [169]).

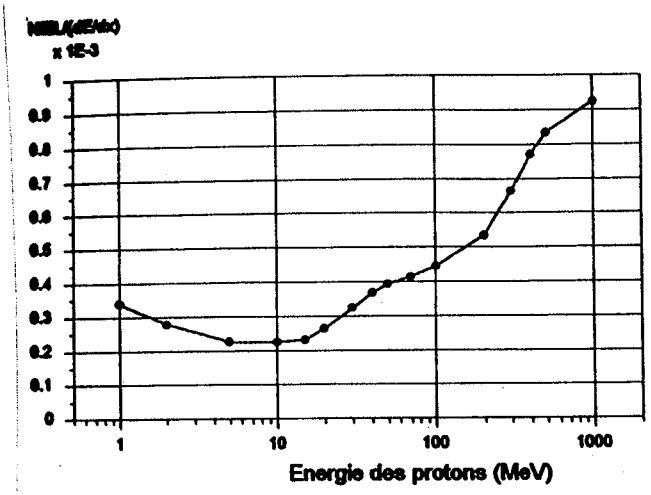

Fig. 84: Variation of the ratio NIEL/ionization energy loss in function of the proton energy (after Buisson et al. [168]).

The effect of elastic non-ionization damage is that a Si atom is knocked from its lattice site and moves in an interstitial (non-lattice) position, with the creation of a vacancy-interstitial pair as a result. This requires on the average a displacement energy between 15 to 40 eV. The primary knock-on or recoil Si atom has generally a large kinetic energy and can generate secondary displacements and hence a collision cascade. The incident ion looses gradually its energy by multiple displacements along its track, whereby most of the energy is lost in the final part, which falls in a narrow interval around the projected range R_p. This which is a sensitive function of the incident energy E_p and of the target material and particle mass. As a consequence, vacancy-interstitial pairs are formed up to a certain depth in the silicon, whereby the concentration is nearly homogeneous in the "tail" region of the track and shows an asymmetric peak near the end (range). These vacancy profiles can be accurately simulated with Monte-Carlo based techniques, like for instance the TRIM code [171]. The program can also be used for a more complex radiation environment like in the case of the fission products of a ^{252}Cf source, which is quite frequently used for the study of SEU related problems in memories. In this case, both alpha's (≈6 MeV) and other heavy fractions (79 MeV Ba and 104 MeV Mo) are emitted, with different energies, resulting in a double vacancy peak,

shown in Fig. 86. The first peak nicely corresponds with the measured damage profiles on Si n^+p junction diodes, which are accessible to the Deep Level Transient Spectroscopy (DLTS) and leakage current measurements [172]. For high-energy electrons, on the other hand, the created damage is quite homogeneous along its track.

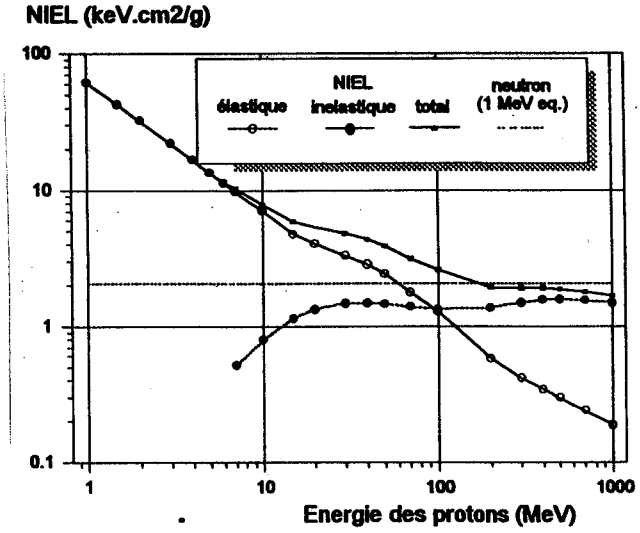

Fig. 85: Variation of NIEL as a function of the proton energy in silicon (after Buisson et al. [168]).

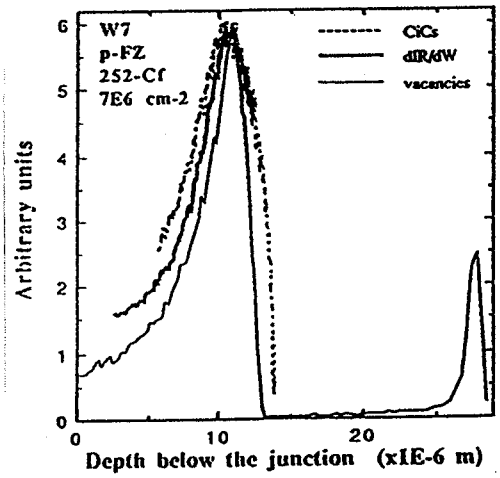

Fig. 86: Depth profile of the derivative of the leakage current with respect to depth for an n-type FZ diode after irradiation using a ^{252}Cf source (fluence $3.92x10^6$ p/cm^2). Superimposed are the interstitial carbon/substitutional carbon (C_i-C_S) related deep level profile obtained on a p-type diode exposed to a fluence of $7x10^7$ p/cm^2 and the damage depth profile obtained with TRIM assuming perpendicular incidence (after Vanhellemont et al. [172]).

Although the primary interstitials and vacancies are highly mobile at room temperature, the largest fraction recombines shortly after their creation. Only a few % escape typically and diffuse from their point of origin, whereby several interactions can take place [173,174]. The vacancies react in principle with the donor atoms (P, As,...) to create the E-centres in n-type silicon; with oxygen, which results in the well-known A-centre and with other vacancies giving rise to e.g. the divacancy V-V, which has four charge states, separated by three levels in the silicon bandgap. The interstitials I interact predominantly with the acceptor atoms (B, Al,...) in p-type silicon, resulting in interstitial B_i (kick out reaction); with carbon, to create C_i-C_S pairs, or C-O complexes in Cz

material, etc...Secondary defect reactions involve e.g. interstitial C_i atoms which pair with P atoms in n-type Si, to create a set of metastable defect levels [175]. It should be remarked here that both the V and I remain mobile at low temperatures. In fact, it is believed that the interstitial is unstable down to 4.2 K, while the vacancy diffusion halts below ≈100 K. The exact temperature depends on the charge state of the point defects, in other words on the doping type and density (Fermi level position).

The deep-level parameters of the major stable (on a relatively long-term time scale) irradiation defects after room temperature irradiation in silicon are summarised in Table II and III, respectively and the corresponding typical DLT-spectra are shown in Figs 87 and 88. The n-type spectrum covers roughly the upper half of the band-gap, from E_C-0.1 eV at 77 K up to E_C-0.55 eV at 300 K, while the lower half is represented by the p-type spectrum. The data shown in the tables have been derived from DLTS measurements.

Table II: Deep-level parameters for the major irradiation induced deep levels in n-type silicon, after room temperature exposure (after Hallén et al. [176]).

Defect Centre	Band-gap Enthalpies (eV)	c_n (cm^3/s)	c_p (cm^3/s)	T interval
V-O (E1)	0.164	$1.4\times10^{-8}\ xT^{0.5}$	$8\times10^{-8}\ xT^{0.7}$	80-108 K
V-V$^{=/-}$(E2)	0.225	$1.6\times10^{-12}\ xT^{1.4}$	7×10^{-7}	105-155 K
V-V$^{-/o}$(E3)	0.421	$5.4\times10^{-9}\ xT^{0.4}$	$2\times10^{-6}\ xT^{-0.3}$	182-266 K
P-V (E4)	---	$1.3\times10^{-11}\ xT^{0.5}$	---	182-266 K

Table III: Deep-level parameters for the major irradiation induced deep levels in p-type silicon, after room temperature exposure (after Hallén et al. [176]).

Defect Centre	Band-gap Enthalpies (eV)	c_n (cm^3/s)	c_p (cm^3/s)	T interval
V-V$^{o/+}$ (H1)	0.194	$>>c_p$	$2.1\times10^{-9}\ xT^{0.2}$	104-146 K
C_i-C_S or COV (H2)	0.339	$5.1\times10^{-23}\ xT^{5.2}$	$1.2\times10^{-10}\ T^{0.61}$	160-238 K

The c_n and c_p in Tables II and III are the capture rate for electrons and holes, respectively. They are defined as:

$$c_n = N_T(\Phi)\ v_{th}\ \sigma_n \qquad (53a)$$

$$c_p = N_T(\Phi)\ v_{th}\ \sigma_p \qquad (53b)$$

whereby the trap density N_T increases with the irradiation fluence Φ. These capture rates are very important for the recombination lifetime in silicon [177-178].

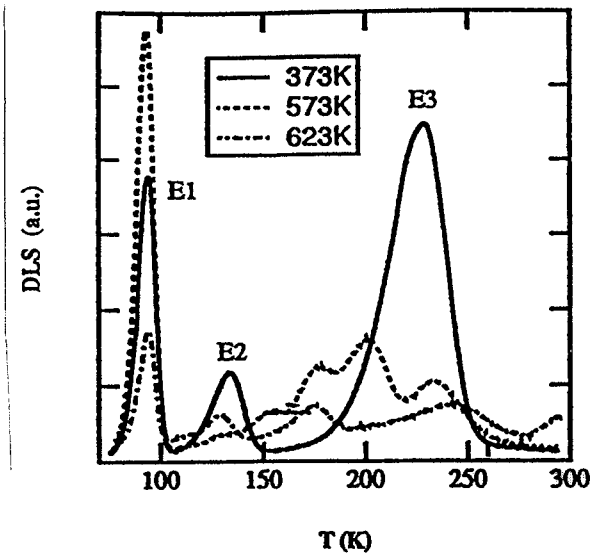

Fig. 87: DLT-spectrum of room-temperature irradiated n-type silicon.

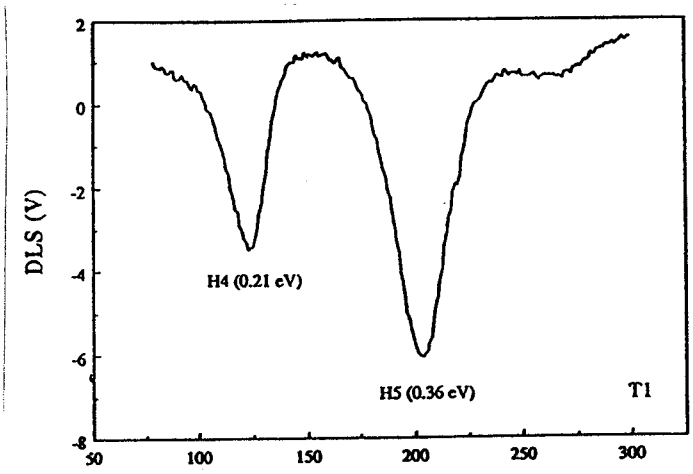

Fig. 88: DLT-spectrum of room-temperature irradiated p-type silicon.

Early displacement damage studies have revealed that the single isolated vacancy is stable (and frozen in - not mobile) below roughly 100 K [179]. This means that one can expect other radiation defects to be formed for low temperature irradiations, which has been confirmed on both n- [179] and p-type Si [174]. Generally, the low-temperature irradiation induced centres anneal out at higher temperatures. It is believed that at least three main annealing stages exist between 4.2 K and 300 K [174]. On the other hand, the room temperature radiation defects are stable up to at least 400 K [180]. It has furthermore been demonstrated that the introduction rate R_T of the defects ($=\partial N_T/\partial\Phi \approx \Delta N_T/\Phi$ since the trap density increases generally proportional to the fluence) increases with increasing temperature. For example, in p-type silicon, the introduction rate for 1 MeV electrons increases from 9×10^{-3} cm^{-1} at 90 K, to 2.6×10^{-2} cm^{-1} at 200 K and to 3.6×10^{-2} (cm^{-1}) at 300 K [174]. Typical values for room temperature irradiations are in the range 10^{-2} to 10^{-3} cm^{-1} for high-energy γ-irradiations [181], and in the range 1 to 10 cm^{-1} for high energy protons [182], $\approx$5 cm^{-1} for 1 MeV neutron [183] and ion [172] irradiation. This large difference is in first instance due to the mass of the incoming

particle (photon). The higher the mass, the more efficient the energy is transferred to the target material, for the same kinetic energy. This also explains the smaller range for heavier particles in silicon. Conversely, to obtain the same radiation damage with lighter particles, one needs a correspondingly higher fluence. It should be remarked here that the introduction rate is strongly affected by a number of material parameters and experimental conditions. Without giving further detail, it should be emphasised that the quality of the starting material, the growth technique (FZ,Cz,epi,...), the doping density, etc. can have a strong impact on the final damage [172,181,182]. This also applies for example for the case of silicon solar cells, intended for space applications [184]. Another factor of interest may be the doping density and or bias during the irradiation. More fundamentally, it is believed that the position of the Fermi level during the irradiation is of key importance for the resulting damage profiles [185-186]. This is explained by considering the impact of the charge state of the vacancy on its diffusion behaviour. Such behaviour has been observed in a broad temperature range for the irradiations, from 15 K up to 400 K.

The creation of displacement lattice damage in silicon has a significant impact on the electrical properties of the material. Following Srour and McGarrity [187], the following basic electrical degradation effects can be distinguished:

* generation of e-h pairs
* recombination of e-h pairs
* trapping of carriers
* compensation of donors and acceptors
* tunneling of carriers

which are also schematically represented in Fig. 89. It is furthermore assumed that the radiation-induced trap concentrations are sufficiently small for the standard SRH theory to be applicable. Recent degradation studies, however, have indicated that for high(er) N_T's introduced by high fluence neutron exposure other non-SRH transitions (e.g. between two adjacent deep levels) can become of importance as well [183].

Consequently, important parameters like the resistivity, the mobility, the generation and recombination lifetimes will be affected. A change in the resistivity results generally from a combination of two effects [188-191]: one, a removal (reduction) of the free carriers takes place, which results from different mechanisms: direct removal of dopants from active lattice sites by interaction with the created V and I giving rise to complexes (E-centre), or dopants in an interstitial site (B_i). Furthermore, the presence of deep levels causes a trapping of the free carriers and has also an impact on the overall Fermi level position, especially if the corresponding charge compensates for the dopant charge. In extreme cases, so-called type inversion (from n- to p-type) occurs in high-fluence irradiated high-resistivity silicon detector material [192-193]. In the high-energy limit, nuclear interactions come into play, whereby silicon atoms (or others) can be converted into a dopant atom. This is not only the case for neutron irradiations but occurs for example for MeV protons as well [194].

Secondly, due to the introduction of (charge) scattering centres, the carrier mobility can be reduced [195]. An example is given in Fig. 90, showing the variation of the free carrier density and the mobility at 200 K as a function of 17 MeV proton fluence [195].

From a bulk device operation viewpoint, perhaps the most important effect is the degradation of the carrier recombination lifetime τ_r. For detector-type and optoelectronic devices (solar cells) where a high lifetime (long diffusion length) is essential, displacement damage is of great concern. Alternatively, high-energy particle irradiation for local lifetime control is now a common practice [196-198]. Generally, the degradation of the recombination lifetime proceeds linear with fluence, for not too high fluences and is described by a so-called damage coefficient described by [172,180,182,184,191]:

$$K_\tau = \frac{\partial(\frac{1}{\tau})}{\partial\Phi} \approx (\frac{1}{\tau(\Phi)} - \frac{1}{\tau_0})/\Phi \qquad (54)$$

with τ_0 the initial recombination lifetime.

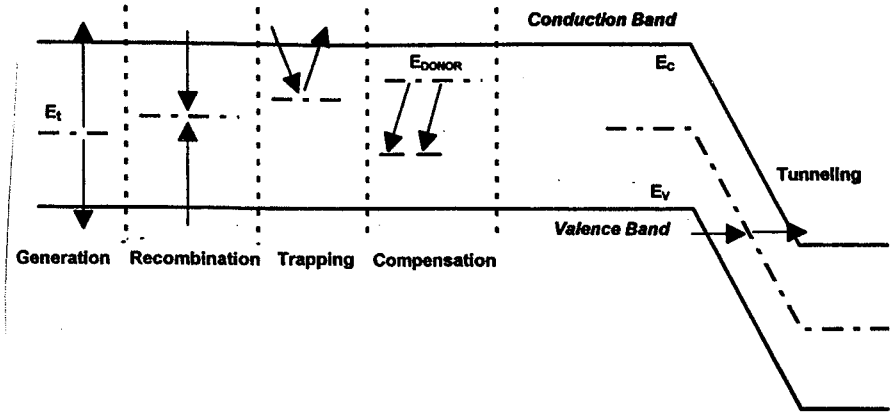

Fig. 89: Illustration of the five basic effects of a radiation-induced defect level (E_T) on the electrical performance of a device (after Srour and McGarrity [187]).

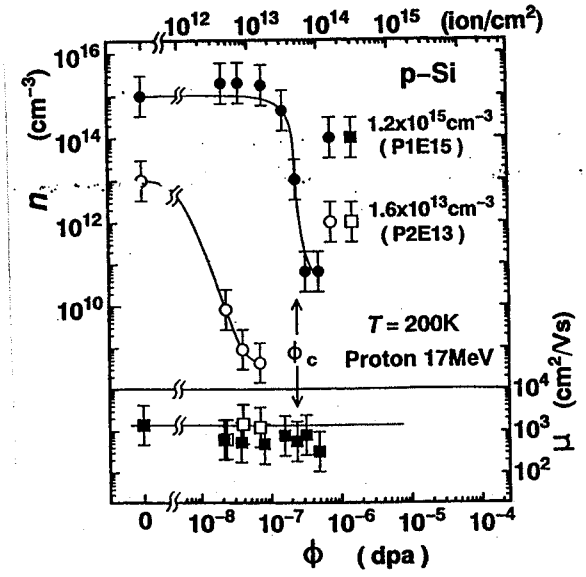

Fig. 90: Irradiation fluence dependence of the carrier density $n(\Phi)$ and the hole mobility $\mu_h(\Phi)$ at 200 K, for 17 MeV proton irradiated Si (after Amekura, Kishimoto and Saito [195]).

For low-injection measurement conditions, the recombination lifetime corresponds in first order to the minority carrier lifetime. In case that j independent recombination levels are active, with respective concentrations N_{Ti} and minority capture cross section σ_i, τ_r can be described by [178-180,182]:

$$\frac{1}{\tau} = \Sigma_{i=1}^{j} N_{Ti}(\Phi)\, \sigma_i\, v_{th} \qquad (55)$$

From eqs (54) and (55) follows that the lifetime damage coefficient is given by the weighed sum of the introduction rates R_{Ti} [191].

One pertinent question to address is which of the dominant radiation induced levels in Tables II and III is the dominant one for practical device operation. Numerous studies over the years have resulted in somewhat conflicting answers. However, nowadays there is a consensus that the low-level injection lifetime at room temperature in standard doped n-type irradiated silicon is governed by the $V\text{-}V^{-/o}$ centre (single negative charged divacancy) [178,182,197], while for high injection, the A centre takes over. This is illustrated in Fig. 91, which represents the calculated lifetime as a function of temperature for a typical 300-K-radiation induced divacancy concentration. More recently, the dominance of the V-V centre as a lifetime killer has been inferred for p-type Si as well [182].

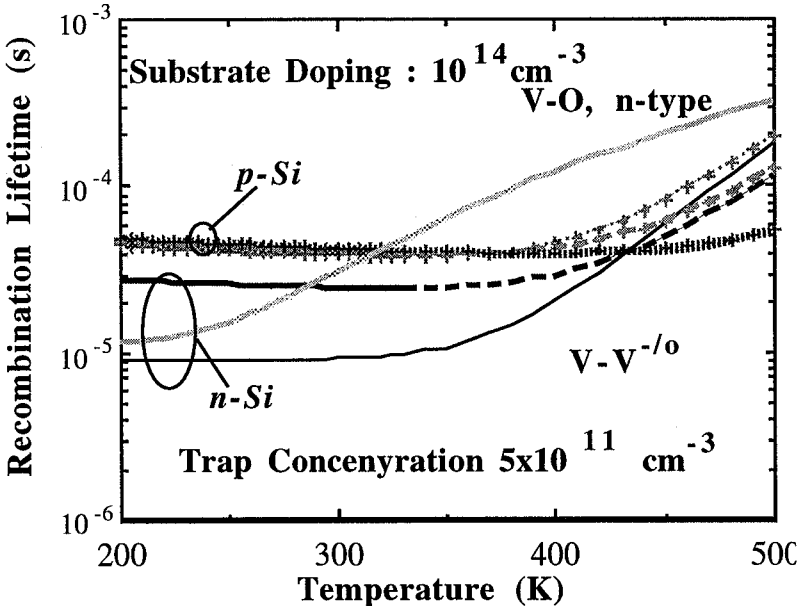

Fig. 91: Calculated recombination lifetime in high-energy proton irradiated n- and p-type silicon, using the parameters for $V\text{-}V^{-/o}$ and V-O of Table II. A substrate doping density of 10^{14} cm^{-3} is assumed and a radiation induced trap density of $5x10^{11}$ cm^{-3}.

The fact that the recombination lifetime reduces with radiation fluence also implies that the generation lifetime τ_g and hence, more importantly perhaps, the reverse current of a silicon diode (depletion region) increases after irradiation. Before irradiation, there exists a tight connection between the two lifetimes [178,199]. In first approximation and for not too asymmetric cross sections, the following relationship holds [199]:

$$\frac{\tau_g}{\tau_r} = \exp\frac{|E_T - E_i|}{kT} \qquad (56)$$

For good quality silicon and processing, typical lifetime ratios are in the range 50 to 100 [178], yielding an effective level position of around ±100 to 120 meV from the intrinsic level E_i. After high-energy proton irradiation and for p- and n-type FZ silicon a similar value has been reported [182]. In that case, one can easily demonstrate that the generation lifetime damage coefficient K_A is proportional to K_τ. Taking into account that the reverse generation current is proportional to $1/\tau_g$, leads to the conclusion that the leakage current damage coefficient K_A is in first order proportional to K_τ, as shown in Fig. 92 for 10 MeV proton irradiated n- and p-FZ silicon diodes. This also follows from the data of Table IV. Hereby is K_A defined as [200]:

$$K_A = \frac{\partial J_A}{\partial \Phi} \qquad (57)$$

Table IV: Damage coefficients for n- and p-type FZ diodes corresponding to a 10 MeV proton irradiation (after [182,200]).

Substrate	K_τ ($cm^2/\mu s$)	K_A ($nA/10^{10}$ p)	R_T (1/cm)
n-FZ	5.2	1.5	E_C-0.23eV:3.2 E_C-0.42eV:5.4
p-FZ	3.5	0.8	E_V+0.19eV:4.4 E_V+0.36eV:10.5

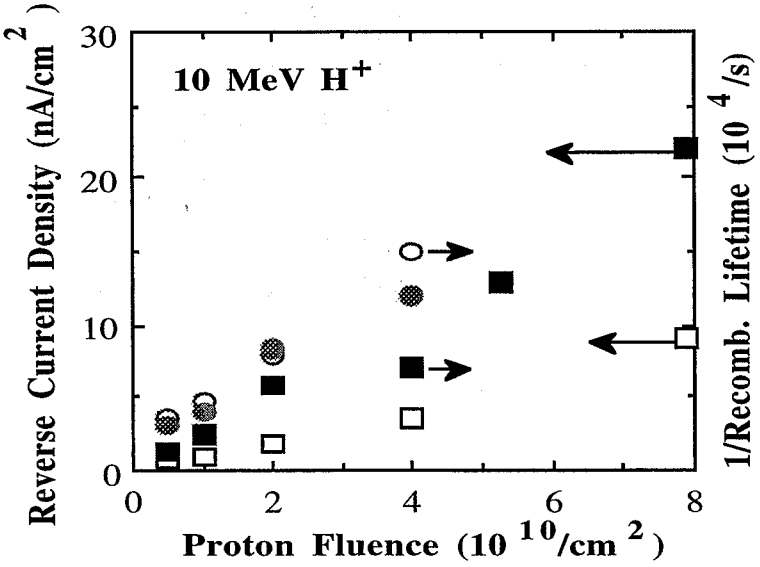

Fig. 92: Degradation of the reverse current density and the inverse recombination lifetime at 296 K, 6 V reverse bias of 1 mm^2 p- (squares) and n-FZ (circles) Si diodes as a function of 10 MeV proton fluence (after Simoen et al. [200]).

It should finally be remarked that during the four decades of radiation effect studies, huge amounts of data have been gathered, most of them related to neutron damage (pure displacement) and γ-irradiation (predominant ionisation damage). The case of other energetic particles is somewhat less documented, because of the unavailability of the appropriate radiation source and/or the high cost and timely nature of the experiments. One way to benefit from the existing data bases is to use so-called susceptibility charts [201] whereby the vulnerability of a certain group of circuits or technologies is splitted up according to ionisation and displacement damage. In general, as explained above, both types of damage will occur for a certain energetic particle. The ionisation damage tolerance has then been derived from γ-exposures and the displacement damage from neutron experiments. This leads to the kind of charts like Fig. 93 [201]. In the same figure, the calibration curves for protons in the range 14 to 800 MeV are displayed as well, which yield a good first-order estimate of the proton effects on Si circuits.

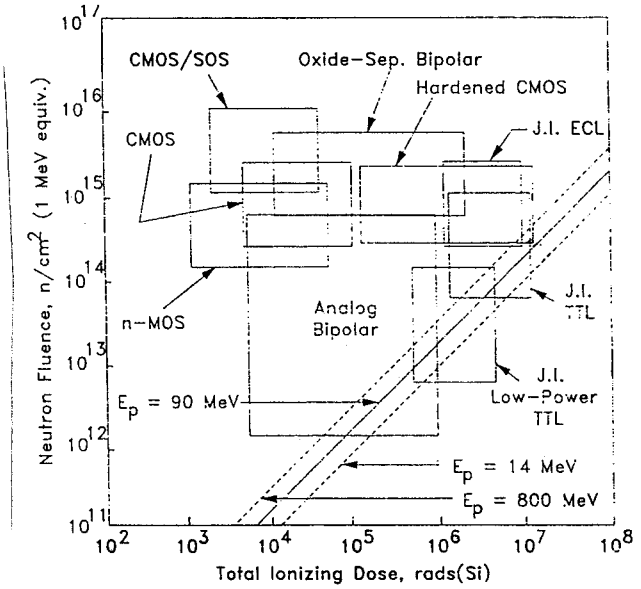

Fig. 93: Schematic representation of the circuit susceptibility, with proton effects (after Raymond and Petersen[201]).

3.2. Ionisation Damage Effects in Devices and Circuits.

From section 3.1.1, it is clear that the ionisation damage effects can be divided in transient (fast) phenomena (charging, latch-up, SEU) and more or less permanent (slow) effects, which evolve on a much larger time scale. For MOS devices, the charging of the dielectric upon exposure to radiation is of paramount importance. Again, one can distinguish charging (hole-trapping) effects and effects related to the conversion (creation) of trapped holes into interface traps, which is a lengthy process. In order to separate both phenomena so-called charge separation techniques have been developed [202-204], which separate the threshold voltage shift due to trapped oxide charge, from the contribution due to interface state generation. Perhaps the most popular is the method developed by McWhorter and Winokur, which is illustrated in Fig. 94 [204]. The shift in the threshold voltage due to interface traps ΔV_{Nit} is related to the stretchout voltage V_{so}, which is given by [204]:

$$V_{so} = V_{th} - V_{mg} \qquad (58)$$

Hereby is V_{mg} the gate voltage at midgap (Fig. 94). ΔV_{Nit} is then given by:

$$\Delta V_{Nit} = (V_{so})post-(V_{so})pre \qquad (59)$$

which is the difference between the post- and the pre-irradiation stretchout. As can be seen, the V_{so} generally increases after irradiation, as does the subthreshold slope and N_{it}. The corresponding increase in N_{it} is then:

$$\Delta N_{it} = \frac{\Delta V_{Nit}\, C_{ox}}{q} \qquad (60)$$

The contribution of trapped-oxide charge is in principle independent of the gate voltage and thus corresponds to the horizontal shift of the linear characteristic of Fig. 94. In other words:

$$\Delta V_{ot} = (V_{mg})post - (V_{mg})pre \qquad (61)$$

and:

$$\Delta N_{ot} = \frac{\Delta V_{ot}\, C_{ox}}{q} \qquad (62)$$

whereby of course $\Delta V_{th}=\Delta V_{ot}+\Delta V_{Nit}$.

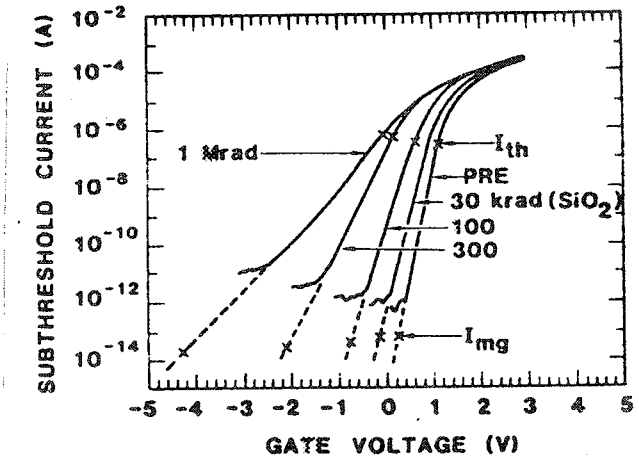

Fig. 94: Subthreshold current curves for a MOS transistor before irradiation and at four different levels of ^{60}Co radiation. Threshold and midgap currents are marked on each curve (after McWhorter and Winokur [204]).

The above method has since its introduction been widely used for the study of radiation effects in MOSFETs and can be extended towards lower temperature operation. However, it has been remarked that for irradiations at 77 K, the technique no longer holds [205-206], because of the degradation of the subthreshold slope due to so-called Local-Non-Uniformities (LNUs) in the created oxide-trapped charge. An example is given in Fig. 95, showing pre- and post-80 K irradiation subthreshold curves and a calculated fit according to the LNU model, whereby the σ stands for the standard deviation of the surface potential induced by the non-uniform distribution of the trapped holes at 80 K. In other words, at liquid nitrogen temperatures, the subthreshold curves become flatter, without the creation of interface traps. Fortunately, at these temperatures hardly no interface traps are created [161,205], so that in this case $\Delta V_{th}\approx\Delta V_{ot}$.

For temperatures below ≈100 K, the irradiation created holes are essentially immobilised in SiO_2 and remain in a so-called self-trapped state whereby they are bound by a polaron to the dielectric. Consequently, nearly all created charge will contribute to the initial flat-band shift and no short- or long-term annealing occurs as long as the temperature is not raised above 120 K or so. This implies that the prompt ΔV_{ot} achieves much larger values at 77 K than at room temperature, even for a 300 K hard oxide. In fact, as shown in Fig. 80 [162], little difference exists for "thick" oxides, whatever the processing is. This imposes special requirements for low temperature gate dielectric hardening. For an oxide thickness above 20 to 30 nm, eq. (51) quite accurately describes the dose dependence of ΔV_{ot} (Fig. 80). As seen in this figure, a saturation of the shift occurs in the high dose regime [162,207-208]. This behaviour can be described by the so-called "field-collapse" model depicted in Fig. 96, which takes into account the effect of a large density of radiation-induced free pairs in the oxide on the field profile [162]. From an originally uniform field (A), a sharp E_{OX} profile is obtained for larger doses, whereby the transport of electrons is slowed down near the positive electrode, so that efficient e-h recombination can take place and the buildup of positive charge is halted (saturated). Further refinement of this simple idea takes into account recombination of electrons with previously trapped holes and yield a good fit for thick oxides (e.g. 26 nm [209]).

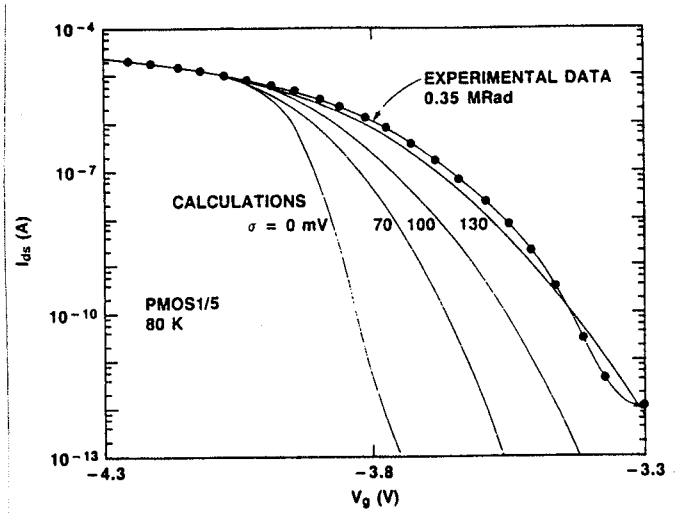

Fig. 95: Comparison of experimental pre- and post-80K-irradiation MOSFET data with calculations from a simple MOSFET LNU model (σ=0 is the pre-irradiation data). The best fit to the data is obtained for a σ=130 mV (after Saks and Ancona [205]).

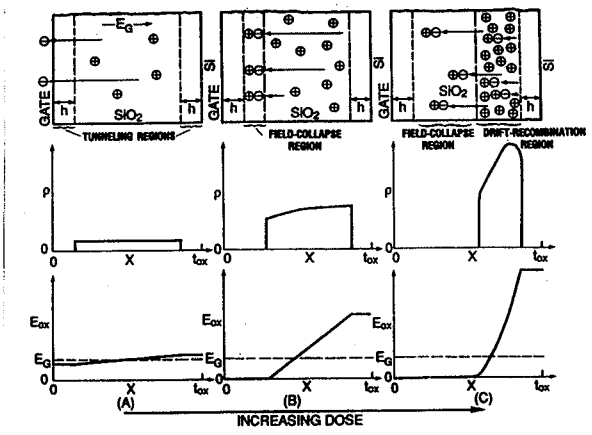

Fig. 96: Oxide charge (top), hole density ρ (middle) and electric field E_{OX} (bottom) for small (A), moderate (B) and large (C) radiation doses (after Klein et al. [208]).

For thin oxides on the other hand, the charge buildup and corresponding ΔV_{ot} at 80 K is much smaller than expected from eq. (51). This is observed in Fig. 97, showing the deviation from the t_{ox}^2 law for oxides below ≈20 nm [208]. Furthermore, the field polarity dependence is different for thin oxides compared with thick ones (Fig. 98) [205]. While for thick oxides the hole yield shows a minimum for fields below 1 MV/cm, because of geminate recombination, no dip is seen for the thin oxides. This behaviour can be reasonably accurately explained by considering tunneling recombination of the holes near the interfaces, as shown in Fig. 99. Assuming an initially uniform trapped hole distribution, the density profile which would result from such an effect is roughly proportional to $\exp[-t \exp(-x/x_0)/t_0]$, where x and t are the distance from the interface and elapsed time, respectively, and x_0 and t_0 are constants. The reduction of hole yield with thickness at 80 K implies that downscaling CMOS technologies results in an inherent hardening of the gate dielectric. Of course, there is still the degradation of the thick isolation oxides, which do not scale in the same way.

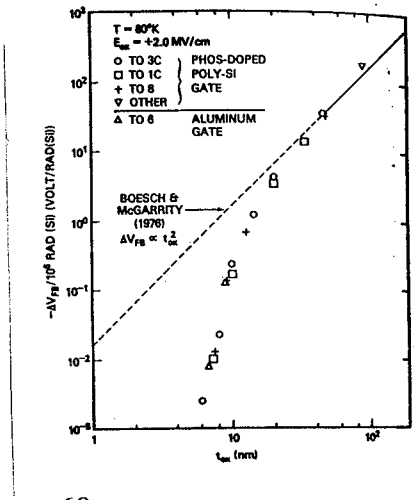

Fig. 97: ΔV_{FB} per MRad dose (^{60}Co) for MOS capacitors at 80 K as a function of oxide thickness. Also shown is the anticipated $\Delta V_{FB} \approx t_{ox}^2$ dependence (after Klein et al. [208]).

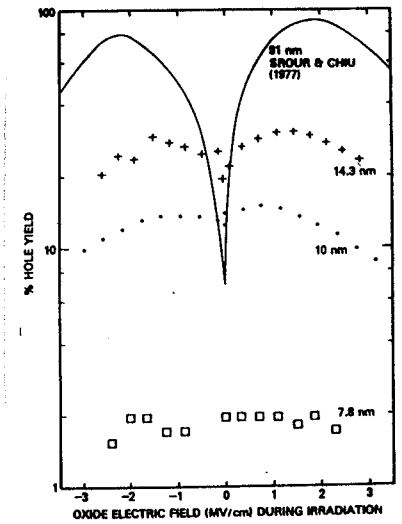

Fig. 98: % hole yield (defined as ΔV_{FB} shift actually observed by the shift which would have occurred for 100 % uniform trapping of the radiation-induced holes) as a function of oxide field for several samples with different oxide thickness (after Klein et al. [208]).

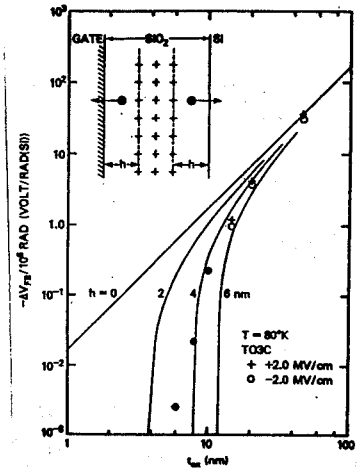

Fig. 99: Comparison between experimental ΔV_{FB} data and calculated ones. The calculated values are deduced from a tunneling model in which all trapped holes are assumed to be removed from the oxide at the interface within a distance h as depicted in the inset. The solid lines are the calculations from this model with h treated as a parameter. An excellent fit to the data is achieved with h=4 (after Klein et al. [208]).

As mentioned in §3.1, the hole transport in the oxide is strongly temperature and field dependent. At 77 K and for moderate (low) E_{OX}, the holes are approximately immobile so that they can stay very long times in the dielectric in a self-trapped state [165,209]. An example is given in Fig. 100 for both conventional oxide (OX) and reoxidized nitrided oxide (RNO). The latter dielectric has been shown to give a larger resistance to radiation than a standard oxide at room temperature [210]. However, for increasing fields (≥2 MeV/cm) the hole transport at 77 K is enhanced significantly, as in Fig. 101. This suggests that by operating MOS devices and circuits at moderate fields from 1 to 5 MV/cm could result in a larger cryogenic radiation tolerance. Further hardness improvement is achieved by using an RNO dielectric (Fig. 101) [163], which can be made even thinner.

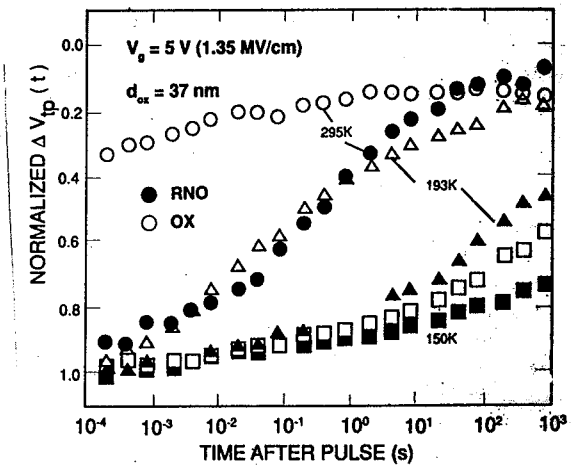

Fig. 100: Normalised $\Delta V_T(t)$ in RNO (closed symbols) and OX (open symbols) p-MOSFETs at 150, 193 and 295 K with E_{OX}=1.35 MV/cm (after Boesch Jr. and Dunn [163]).

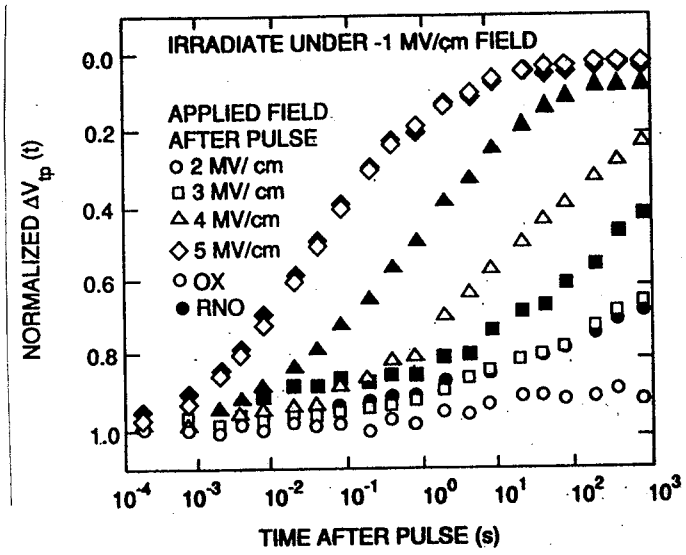

Fig. 101: Normalised $\Delta V_T(t)$ in RNO (closed symbols) and OX (open symbols) p-MOSFETs irradiated at 77 K with E_{OX}=-1 MV/cm. E_{OX} switched to values from 2 to 5 MV/cm at 6 μs after the LINAC pulse (after Boesch Jr. and Dunn [163]).

For temperatures above ≈120 K, the hole transport becomes thermally activated (eq. (52)). Generally, a distribution of levels is found in the range 0.3 eV - 0.5 eV, depending on the applied field [209]. This is in support of a transport model, whereby the holes are trapped and activated from a distribution of deep levels in the oxide upon their migration to the negative electrode [209]. Experimental values for the parameters defined in eq. (52) are given in Table V, showing a qualitative agreement for the transport in OX and RNO [163].

Table V: Transport parameters defined in eqs. (52) for OX and RNO, corresponding to a field E_{ins}=1.35 MV/cm (after Boesch Jr. and Dunn [163]).

Dielectric	b_{ins} [eV/(MV/cm)]	E^0_{ins} (eV)
OX	0.04	0.56
RNO	0.025	0.35

Radiation-induced interface trap generation is strongly reduced at 77 K [161,205,211-213]. Typical densities created at 77 K irradiations are in the range 10^{10} /cm^2 eV, as shown in Fig. 102 [205], which is only 10 % of what is typically generated at room temperature for the same total dose exposure. In fact, even for 4.2 K irradiations the creation of interface traps in thick field oxides has been observed [214]. The 'prompt' mechanism accounts for most of the radiation-induced N_{it} formation in field oxides. It is now believed that the responsible mechanism for the formation of these so-called 'prompt' interface states is limited by the hole transport [161,213], although the exact nature of the processes involved is unresolved so far.

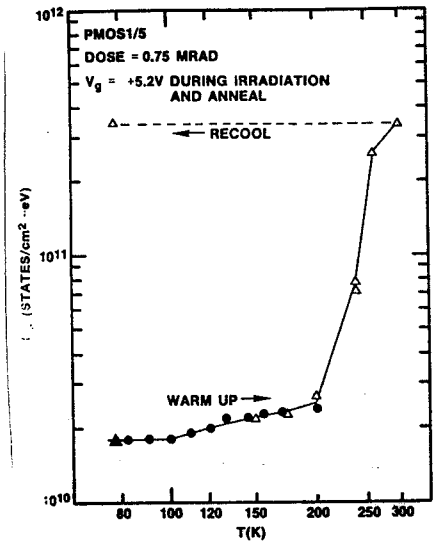

Fig. 102: Annealing experiment. A MOSFET is irradiated at 80 K, warmed up to 295 K, then re-cooled to 80 K. Interface states form during warming up, showing that the main D_{it} formation is frozen out at 80 K (after Saks and Ancona [205]).

When heating up a MOS device which has been irradiated at low temperatures, typically two annealing stages can be distinguished in Fig. 102. One situated in the range 120-150 K and the second one with an activation energy in the range 0.7 to 0.9 eV, which is quoted to correspond to the diffusion process of protons in the oxide [161]. The first annealing stage is thought to be associated with the diffusion of neutral H_2 and has for instance also been observed in 77 K HC degraded MOSFETs, yielding at most ≈10 % of the total radiation-induced interface traps N_{it}. Finally, in a number of studies, the low-temperature properties of radiation-induced oxide traps have been studied, in both gate [215-216] and buried oxides (SIMOX) [217-218].

It is clear that when ionising radiation impinges on a CMOS circuit a number of both transient and long-term degradation effects occur. Hole trapping in the gate dielectric results in a reduction of the flatband (and threshold) voltage for n-MOSFETs (an increase for p-MOSFETs), which changes the net operation voltage. However, as indicated in Fig, 103, not only the gate transistor is degraded but also the field and the encroachment transistor, which can generate parasitic subthreshold leakage [219] in n-MOSFETs, if the field threshold voltage reaches unacceptably low levels.

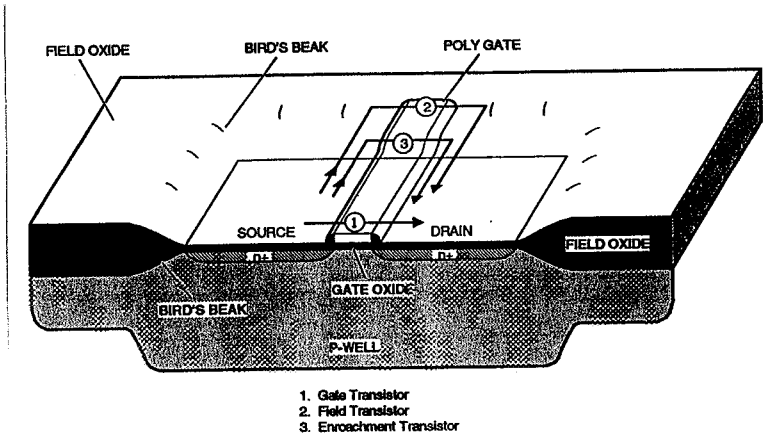

Fig. 103: NMOS cross section.

For p-channel devices, the threshold voltage becomes more negative. However, one particular problem related to p-MOSFETs in n-polysilicon gate CMOS at 77 K is the freeze-out occurring for the buried-channel type of devices, which are in principle more rad-hard than surface-channels [219-220]. At cryogenic temperatures, a subthreshold kink is observed typically in Fig. 104, which remains after total-dose exposure. This anomalous behaviour can be avoided by omitting the counterdoping of the channel, at the expense of a more negative V_T and a larger susceptibility to punch-through [219-220].

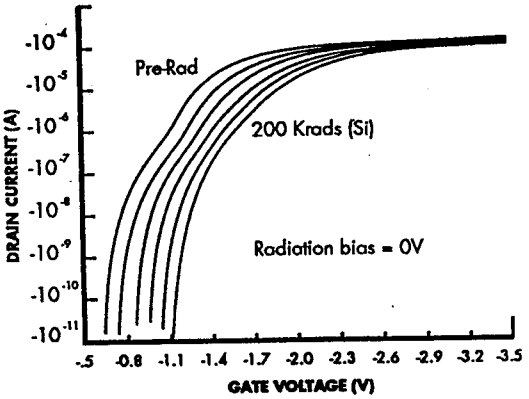

Fig. 104: Measured transfer characteristics at 77 K for a p-channel device with a counterdope implant and with various total doses and 0 V gate bias during irradiation (after Groves et al. [219]).

Ionising radiation not only causes a charging of the oxide, but results after some time in the increase of N_{it}. This can give rise to a number of deleterious effects: a straightforward reduction of the subthreshold slope and a concomitant change in V_T [221]. For a large increase of N_{it} so-called rebound can occur, whereby the final threshold voltage for n-channel devices becomes higher than the initial pre-rad value, which is not likely to occur below 200 K. Simultaneously, the mobility and transconductance is reduced [206,219-222], as evidenced by Fig. 105 for 300 K and 77 K. In general, the mobility reduction is due to coulombic scattering by the created oxide-trapped charge ΔN_{ot} and by the radiation-induced interface charge ΔN_{it} according to the general formula [206]:

$$\frac{\mu}{\mu_0} = \frac{1}{1+\alpha_{it}\Delta N_{it}+\alpha_{ot}\Delta N_{ot}} \qquad (63)$$

with α_{it} and α_{ot} the respective scattering parameters, in the range 10^{-12} cm^2.

In case of submicron LDD-type p-MOSFETs, a strong reduction of the transconductance is observed after 77 K [220], or 10 K [223] irradiations. An example is given in Fig. 106. The basic reason for this behaviour is the charging of the spacer oxides on top of the LDD region, which depletes the surface and hence increases the series resistance associated with the LDD. As in Fig. 106 [220], this can be successfully counteracted by leaving out the lowly doped implant and in fact use the same dose as for the highly doped drain regions [220-221]. More fundamental studies of the low-temperature radiation response of MOSFETs in order to determine the exact degradation mechanism have also been reported [224-225].

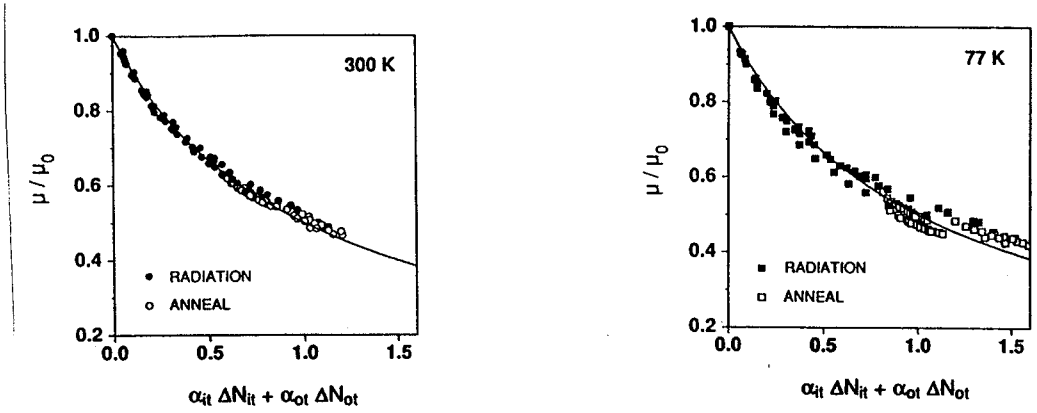

Fig. 105: Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) in p-channel power MOSFETs as a function of the linear combination $\alpha_{it}\Delta N_{it}+\alpha_{ot}\Delta N_{ot}$: (a) at room temperature, and (b) at 77 K (after Zupac et al. [206]).

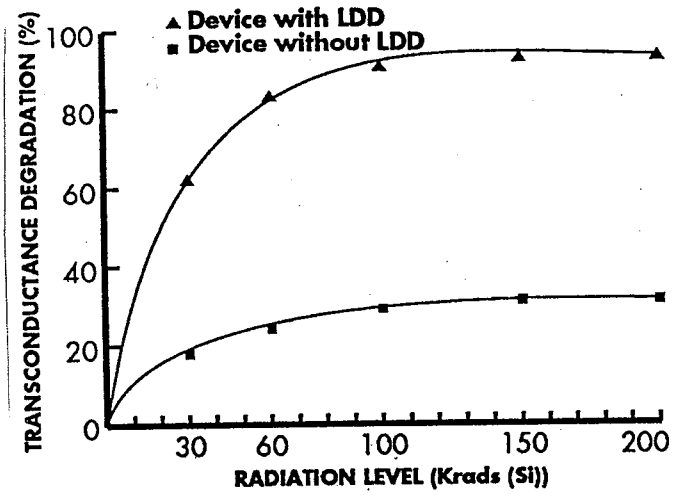

Fig. 106: Improvement in transconductance performance over radiation at 77 K obtained by removing LDD region from p-channel device (after Pantelakis et al. [220]).

In CCDs, ionising damage will first of all result in a shift of the operation voltages and performance [169]. Most gate dielectrics in commercial CCDs are thick (≈100 nm) and radiation-soft, resulting in a typical flatband shift in the range 0.1V/krad(Si) (300 K), but may be considerably higher for cryogenic operation. Performance degradation (particularly in the operation point of the output amplifier) will become noticeable for total doses above 10 krad(Si). Present-day CCDs may withstand doses up to 100 krad(Si), although considerable progress is being made in hardening up to the Mrad(Si) range [169]. The creation of interface traps results in an increase of surface-generated dark current, which in turn affects the signal and transfer noise and hence the Full Width at Half Maximum (resolution) [169]. Typical values are in the range of 1-10 nA/cm^2/krad(Si) at 20 °C. Low temperature operation removes this problem, because of the thermally activated nature of the leakage current, if irradiated at room temperature. This applies the more for low-temperature exposure because of the suppression of N_{it}

formation for cryogenic irradiation. The same is achieved if instead of a surface-channel, a buried-channel architecture is used, or the surface is inverted during the operation (MPP devices) [169]. However, as will be seen in the next section, the dark current of space-born CCDs will be limited by displacement damage.

Finally, the degradation of the current gain of advanced bipolar transistors exposed to a 5 to 30 keV electron beam at 80 K has been shown to recover much slower than at room temperature [226]. More recently, interest has turned to the response of SiGe HBTs to ionising and high-energy particle irradiation, both on the room temperature operation [227] and on the 77 K operation [228-229]. From Fig. 107, an excellent total dose response of the current gain at 77 K is derived [228]. The same applies for room temperature neutron exposure in Fig. 108 [229]. From these initial studies, it is concluded that SiGe HBTs show excellent radiation tolerance down to 77 K.

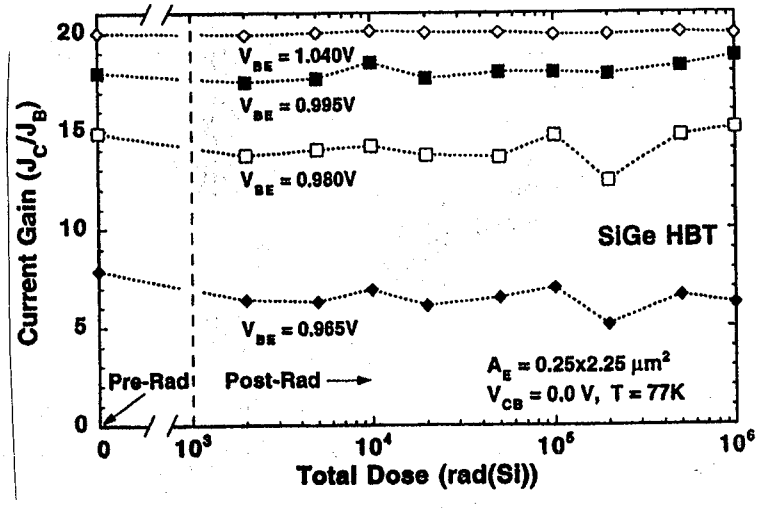

Fig. 107: Current gain of a SiGe HBT as a function of total radiation dose at constant base-to-emitter voltage V_{BE} at 77 K (after Babcock et al. [228]).

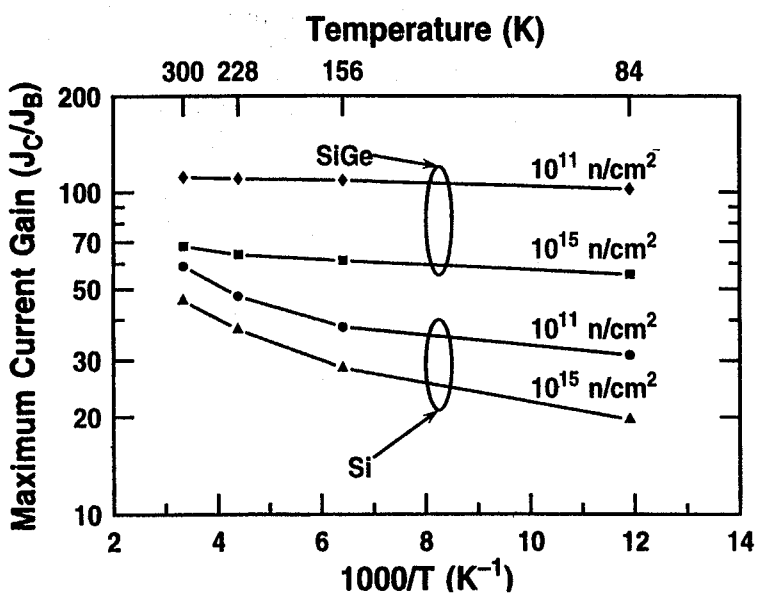

Fig. 108: Maximum current gain as a function of reciprocal temperature for SiGe and Si transistors, at different neutron doses (after Roldan et al. [229]).

In a number of studies, transient ionization damage in CMOS devices and circuits has been studied as a function of temperature [230-232]. Initial results indicate that the soft error cross sections for heavy ions reduce with temperature, although the behaviour strongly varies from application to application [231]. The problem has also been tackled in more recent simulation efforts [167,233]. According to the work by Iwata and Ohzone [167], the single-event latchup threshold initially goes up upon cooling, reaches a maximum around 120 K and then sharply reduces below (Fig. 109), which is in contrast to the steady-state latchup behaviour at low temperature, described in chapter 2. Other calculations for practical cryogenic CMOS circuits indicate, however, that SEL should be no real problem [233]. For instance, the use of a guard-ring structure for the n-MOSFETs should clearly improve the immunity to single events.

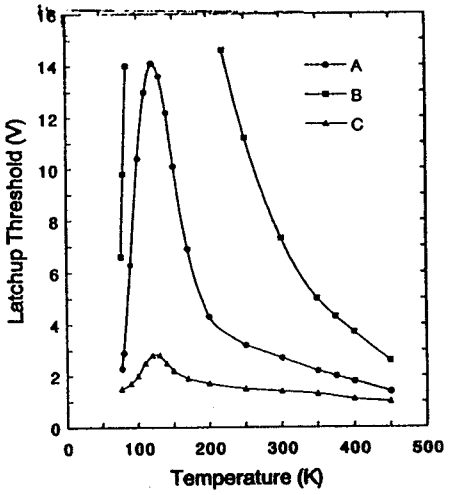

Fig. 109: The latchup threshold as a function of temperature for the A, the B and the C incident types (after Iwata and Ohzone[167]). The incidences A,B and C are depicted in Fig. 82.

Proton-induced transient effects are also a concern for space-born CCDs [169]: a MeV proton transient will roughly create 2000 electrons, which should be compared to a typical signal charge of $5x10^5$ electrons.

In the above, a number of problem fields for radiation exposed circuits have been defined. In order to increase the resistance against ionization damage, hardening efforts are undertaken, which either involve a modification (optimisation) of the technology, the design and architecture, or the operation conditions (temperature, shielding, clocking and readout speed,...). Also, measures can be taken at the device and at the system level in order to reach a satisfactory lifetime in the expected radiation environment.

The choice of substrate can already provide considerable hardness improvements: epitaxial substrates give considerable SEL (SEU) robustness compared with standard substrates. The same is true for SOI/SOS based technologies [15,223]. For MOS technologies, the hardening of the gate dielectric is of key importance, although the problem lies different for cryogenic applications. As mentioned above, the use of RNO can alleviate part of the problem [163], especially if combined with moderate fields at 77 K. In fact, there is an inherent total dose hardening associated with downscaling CMOS technologies, from the strongly reduced t_{ox} dependence of the hole yield mentioned above (eq. 51). This is even more so, if the classical LOCOS isolation is replaced by more advanced isolation schemes like trenches for example. However, an often used alternative is a p^+ guard ring surrounding an n-MOS structure, depicted in Fig. 110, which is at the expense of integration density (minimum device size increases) [219-221]. The same applies for the omission of the LDD or channel implant for cryogenic p-

MOSFETs [220-221]. A final remark is that in general, it has been found that hardening a cryo-technology is generally detrimental to cryogenic HC reliability [221].

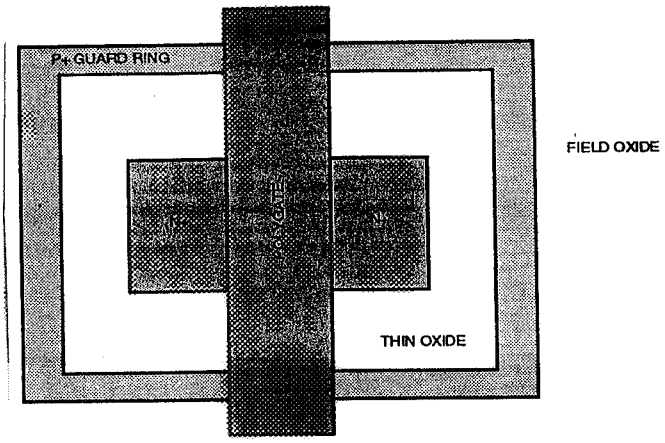

Fig. 110: An n-channel transistor with a guard ring. Note that the width of the transistor is defined by the N^+ S/D pattern and not by the thin oxide region (after Groves et al. [219]).

3.3. Displacement Damage in Cryogenic Si Electronics.

As discussed above, the degradation of solid-state components by displacement damage is a complex function of the original vacancy-interstitial pairs created. The latter can be modeled quite accurately by Monte-Carlo or analytical procedures [170]. The ultimate goal of these modeling efforts is to be able to simulate the expected damage in a given radiation and shielding environment, which would replace timely and expensive radiation testing. For Si bipolar devices, it has been demonstrated successfully that the electrical damage can be predicted quite accurately by the NIEL concept [234-235]. This is shown in Fig. 111 for bipolar junction transistors. The same concept can be applied to other "bulk" type devices like CCDs [236], or Si diodes (Fig. 112). The general idea behind the NIEL concept is to limit the number of radiation experiments by irradiating at one (or a few) particle energy for a number of fluences. In case of protons, 10 MeV is the energy of preference, as the depth range is around 700 μm so that homogeneous displacement damage is created in a large part of a Si device, while there is a significant amount of ionization damage as well (Fig. 83). For electrons and neutrons 1 MeV is the energy of choice.

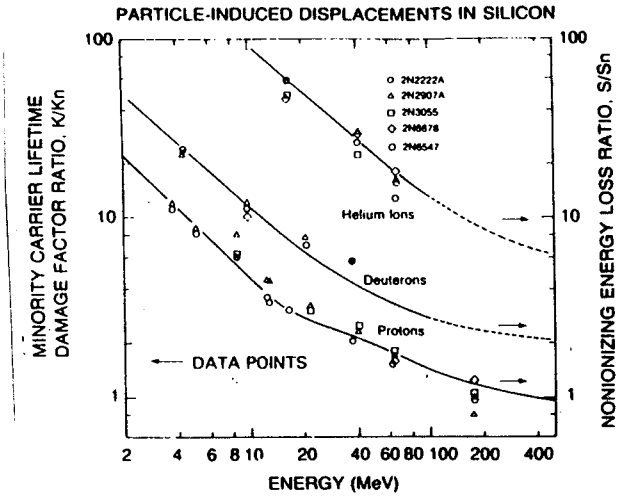

Fig. 111: Damage factors for bipolar transistors for protons, deuterons and helium ions, normalised to 1 MeV equivalent (Si) neutron damage factors as a function of energy. The solid lines (right hand ordinate) are calculations of the corresponding ratios of the nonionising energy loss (after Dale and Marshall [235]).

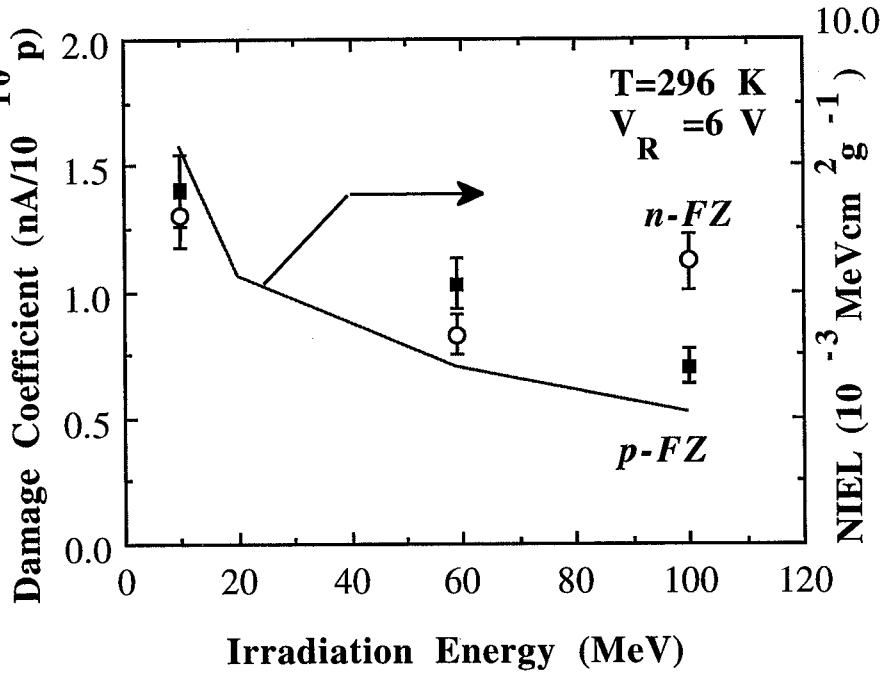

Fig. 112: Leakage current damage coefficient in function of the proton energy, for FZ Si p-n junction diodes at 296 K and a reverse bias of 6 V.

At the selected energy, the damage coefficient (also called factor or constant) of a single electrical parameter P_{IV} is measured as a function of the particle fluence (in case of Fig. 111 it is the static current gain; for Fig. 112 it is the bulk leakage current density J_A) and derived from the formula:

$$K_{10} = \frac{\partial P_{IV}}{\partial \Phi(10\ MeV)} \approx \frac{\Delta P_{IV}}{\Phi} \qquad (64)$$

In many cases, the parameter at stake degrades linearly with fluence, so that K_{10} is a constant factor. For example, a value of $\approx 10^{-19}$ A per 10 MeV proton is found in Fig. 112, for the increase in reverse current density of $2x10^{14}$ cm^{-3} doped FZ Si p-n junction diodes [200]. The average degradation at another particle energy then follows from the NIEL, i.e. it is given by:

$$\Phi(E_p)\ xK_{Ep} = \Phi(E_p)\ K_{10} \frac{NIEL(E_p)}{NIEL(10MeV)} \qquad (65)$$

If the particle distribution of the radiation environment is known, one can integrate eq. (65) over the differential spectrum $d\Phi/dE$, to derive the total device degradation. In principle, by using calibration curves like in Figs 93, or 111, one can translate the calculated results to other high-energy particles as well [234-235].

Two remarks have to be made: first, taking into account the many factors which are of importance for determining the final stable radiation damage, one has to perform at least a limited radiation testing for every type of device. As an example, one can mention that the leakage current damage coefficient in a Si junction diode is a sensitive function of the starting material and subsequent diode processing, resulting in a variation of K_A between 0.5 and 2 $x10^{-19}$ A per 10 MeV proton [200]. A similar type of variation has been found for CCDs fabricated on different substrates [236]. Second, in some cases, the NIEL concept is no longer valid [183]. This may be particularly true for high-fluence (neutron) irradiations, where the electrical damage evolves no longer proportional to the fluence. The same applies for low-energy irradiations where the damage peak falls into or close to the active device region, so that the damage shows a marked profile with distance. Another possibility may be that the electrical parameter at stake is rather connected to the ionization damage, which seems to be the case for the low-frequency noise of irradiated diodes [237].

With respect to low temperature radiation displacement damage, little studies have been reported so far. One reason may be that standard bipolar transistors show a poor cryogenic performance anyhow and are thus not popular for such applications. In case of silicon diodes, one should take into account that the SRH leakage current strongly reduces with temperature, which implies a hardening effect by cooling. Recently, the 77-K-radiation behaviour of power diodes has been studied in view of the Large-Hadron-Collider at CERN [238]. The major concern there is the increase in resistivity (series resistance) due to the irradiation. A similar concern exists for high-resistivity silicon radiation detector diodes [183], although little studies have been devoted specifically to cryogenic operation.

One particular class of devices which can be very susceptible to displacement damage are solid-state imagers [169,235,239], with CCDs as the best known example [169]. The possible interactions when a high-energetic particle impinges on a CCD are depicted in Fig. 113 [169]. Although ionization and transient damage can be important [169,239], ultimately the device performance for state-of-the-art CCDs will be limited by the creation of bulk traps and GR centres. One should also keep in mind that, since imagers are analog devices, the degradation will proceed gradually with time, which stands in contrast to pure digital circuits like memories, which show abrupt failures. For a given expected operation time and radiation environment, one can calculate the total dose to which the CCD will be exposed. In order to estimate the performance degradation, one can not rely on simulations based on NIEL or TRIM only [169,2391], but as pointed out above, for each type (and even batch) of devices some limited testing needs to be performed.

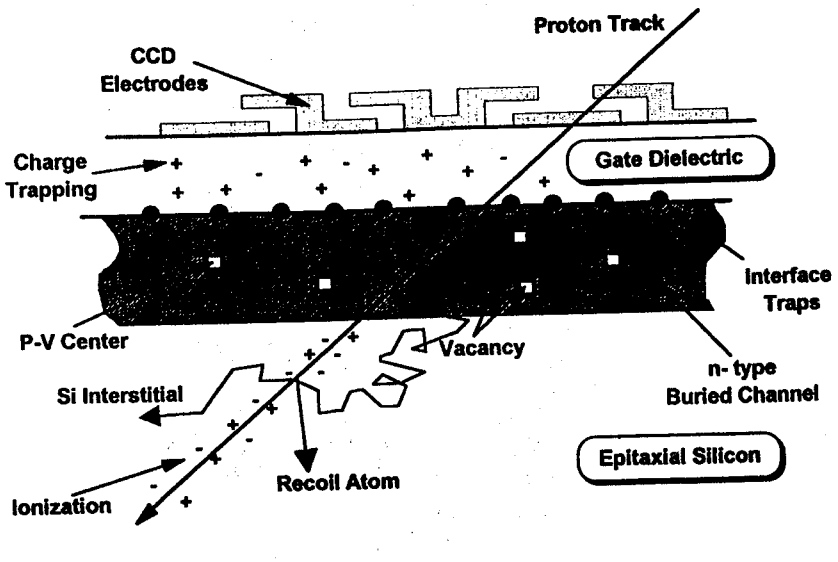

Fig. 113: Schematic diagram of the processes taking place when a proton passes through a CCD. These are charge trapping in the gate and interface trap generation (ionization damage), ionization in the silicon (transient damage) and displacement damage in the silicon, which produces vacancy/interstitial pairs and stable defects such as the E centre. Note that since the gate dielectric is usually composed of an oxide and a nitride layer, both holes and electrons can be trapped (after Hopkinson, Dale and Marshall [167]).

The creation of defect centres in the n-type buried-channel of a (BC) CCD (which is generally created by P-implantation and has a typical doping density in the range $\geq 10^{16}$ cm^{-3}) first of all gives rise to carrier trapping and release (generation), which results in a decrease of the Charge Transfer Efficiency (CTE) or an increase in the Charge Transfer Inefficiency (CTI=1-CTE). In turn, this will contribute to the transfer noise, which results in a loss of energy resolution or increase in FWHM in case of X-ray spectroscopy, for example. This is illustrated in Fig. 114 for a proton irradiated scientific CCD, which not only shows a broadening of the Fe^{55} peaks but a shift of the average position, which corresponds to the average number of created and collected electrons by a photon with an energy of 5.9 and 6.4 keV [240]. Note that the X-rays themselves have too low energy to create any displacement damage. The increase in FWHM for a CCD exposed to protons at -90 ^{o}C as a function of the fluence is shown in Fig. 115 [241].

Both the electron trapping and the emission are a strong function of a number of parameters. The emission time is for instance thermally activated, while the capture time is reversely proportional to the density of free carriers, i.e. to the signal size. Furthermore, the effect of a trap in a certain pixel will strongly depend on the transfer (clocking) rate of the signal from pixel to pixel, towards the output amplifier. This implies that the actual CTI for a MeV proton exposed CCD relies heavily on the operating temperature and speed, as illustrated in Fig. 116 [242]. It is shown that the CTI shows a pronounced increase around 210 to 220 K, which shifts to higher T for a higher transfer rate. At the point where the CTI is half its maximum value, half of the trapped electrons have been emitted in the time t_0, from which the activation energy of the radiation-induced trap level can be derived [241].

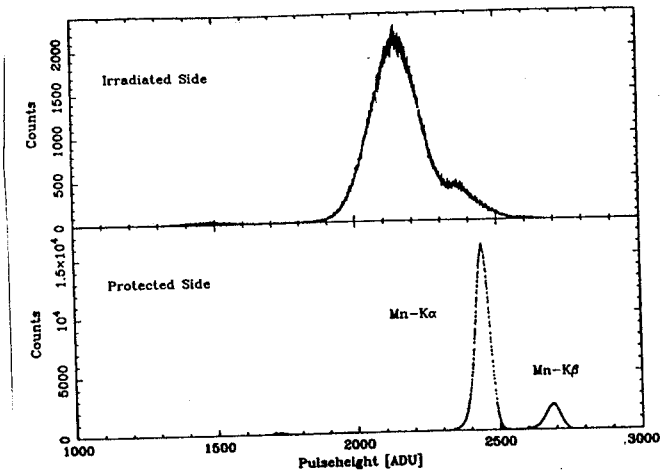

Fig. 114: Fe^{55} spectra obtained from the irradiated and control (protected) sides of an irradiated CCD. The prominent feature is the Mn-Kα peak centered at about 1620 electrons (2450 ADU) on the protected side. The CTI degradation on the damaged side shifts the central peak of the Mn-Kα feature downward. The loss of spectral resolution on the damaged side is apparent (after Gendreau et al. [240]).

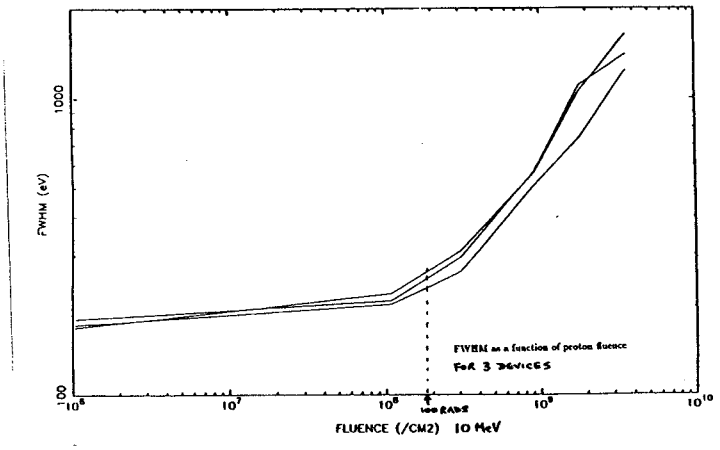

Fig. 115: FWHM as a function of proton fluence (after Abbey et al. [241]).

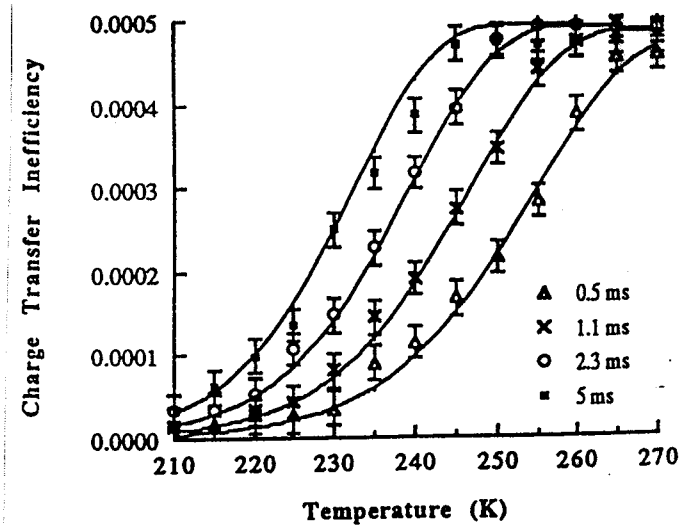

Fig. 116: The shift in peak as the time between the signal bursts is altered. The signal size is 10^4 electrons and the device received ±30 krad(Si) (after Robbins et al. [242]).

When measuring the CTI as a function of temperature, a number of such steps are encountered in Fig. 117, corresponding to the proton-induced radiation levels [167,239,241-249]. At the same time, it is clear that specific temperature windows exist, where the CTI is hardly affected by the irradiation. Lowering the operation temperature to such a valley is indeed a very efficient way of hardening [167,236,239,250]. From CTI "spectroscopy" of proton irradiated CCDs it has been observed that the dominant defect level is the E-centre (200 - 300 K range) and the A centre at the lower temperature end in Fig. 117. Typical introduction rates are ≈30 /cm for both the E- and A-centre for 10 MeV protons [236], in the P-doped buried channel of the CCD. In fact, annealing studies reveal that the CTI peak above 200 K consists for 85 % out of E-centres, which anneal above 150 °C and for ≈15% divacancies, annealing at higher temperatures [236]. This suggests that a periodic in-flight high-temperature anneal is a possible way to reduce the impact of radiation damage [167,236,241,251]. The expected improvements of different hardening efforts for modern CCDs are shown in Fig. 118 [244,249]. The fact that for CCDs the E-centre is the dominant radiation defect compared with the V-V (which is the dominant lifetime detractor in normally doped n- and p-type Si) stems from the fact that in the buried-channel, the P-doping concentration is much larger than in standard Si substrates, so that the probability for capture of a created vacancy is much larger. Also comparing an introduction rate in the buried channel in the range of 30 /cm with the values of Table II shows an at least 10 times bigger value for the E-centre in CCDs.

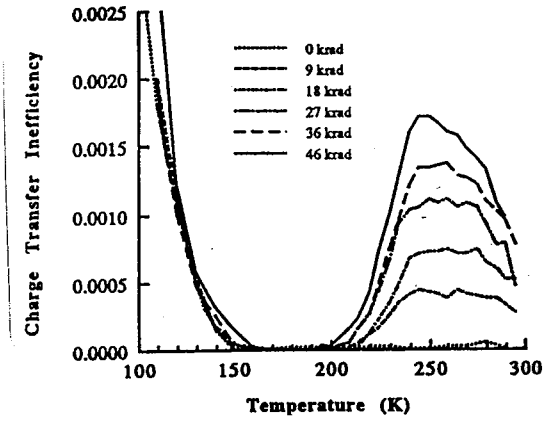

Fig. 117: The change in transfer inefficiency with dose (after Robbins et al. [242]).

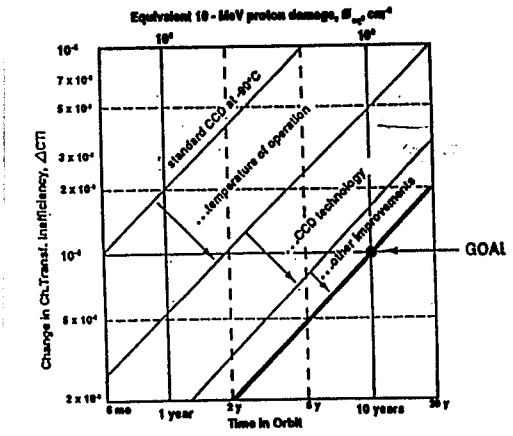

Fig. 118: CTI change vs. fluence in X-ray astronomy CCD imagers. The improvements expected from various radiation hardening techniques, starting with the performance of a standard EEV CCD02 design (after Holland et al. [244]).

As outlined above, in order to predict the radiation response and hardness of a specific CCD one first of all needs to perform a few radiation tests at e.g. a reference energy of 10 MeV for protons, in function of the fluence. A typical result for the CTI is reported in Fig. 119 [236], showing a linear response of CTI versus fluence; the corresponding damage factor for the CTI is in the range $K_{CTI}=2x10^{-13}$ cm^2 [167,236,241]. Hereby should one also take into account the effect of the signal size on CTI illustrated by Fig. 120 [235,245], whereby for larger signals (hit rates), a better CTI is typically found. This stems from the fact that for large signal sizes a larger fraction of the traps remains filled with electrons and does not contribute when the next charge packet is being transferred (trap saturation). Finally, the expected damage can be modeled by integrating over the particle spectrum the individual contributions of eq. (65), resulting in [167,235-236]:

$$\text{mission damage} = \int_0^{\infty} K_{CTI} \frac{NIEL(E)}{NIEL(10MeV)} \frac{d\Phi(E)}{dE} \cdot dE \qquad (66)$$

with $d\Phi(E)/dE$ the differential proton fluence (=flux times mission duration).

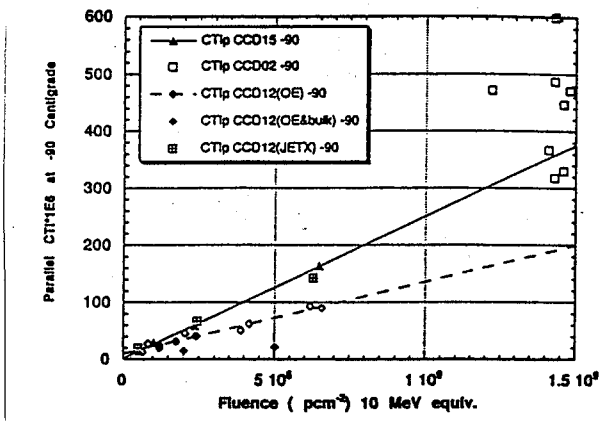

Fig. 119: Parallel CTI in a proton-irradiated diode versus equivalent 10-MeV proton fluence at -90 °C (after Holmes-Siedle, Holland and Watts [236]).

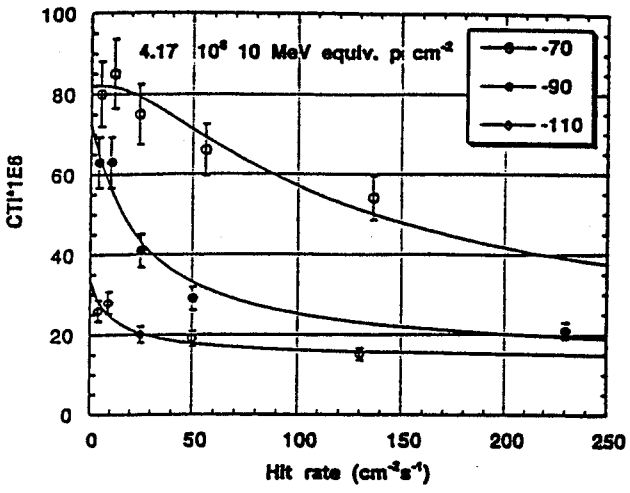

Fig. 120: Parallel CTI in a proton-irradiated CCD as a function of Fe^{55} X-ray photon hit rate (after Holmes-Siedle, Holland and Watts [236]).

A second major effect associated with the creation of displacement damage in CCDs is the increase in dark current, which is another source of signal noise and loss in FWHM. As shown in Fig. 121, the average dark current level increases proportionally with fluence [167,235-236,250-252]. K_A values in the range 2.8×10^{-11} $nA/cm^2/proton/cm^2$ can be found in the literature [167].

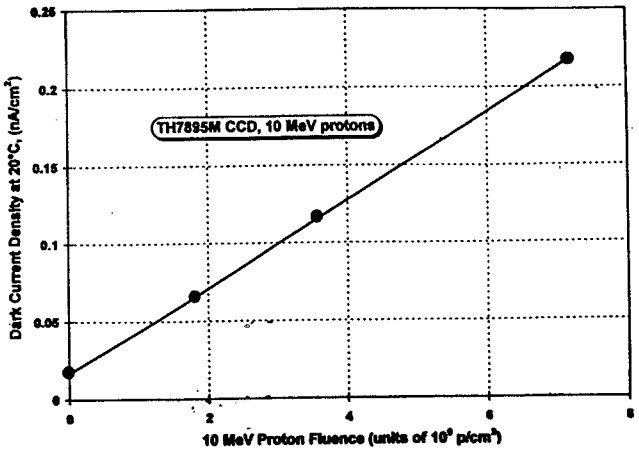

Fig. 121: Mean dark-current density versus fluence of 10-MeV protons for MPP CCD (after Hopkinson, Dale and Marshall [167]).

Of more importance is the fact that the dark current distribution broadens considerably after proton exposure, which is due to the occurrence of bright pixels (dark current spikes). An example is given in Fig. 122 [236], which shows that these anomalous pixels can not be described by the standard NIEL concept. It should be emphasised here that NIEL estimates the average displacement damage, but does not take into account statistical fluctuations related to damage extremes. These pixels are characterised by an enhanced generation rate, corresponding to a lower activation energy (Fig. 123). From Fig. 123, one can also deduce that by lowering the operation temperature sufficiently, the impact of dark current spikes can be reduced or even eliminated. The lowering of the activation energy from an average value of $\approx$0.6 eV to values in the range 0.4 - 0.5 eV has been ascribed to electric field lowering of the emission barrier by the Poole-Frenkel effect [250-252]. This could occur for a radiation trap which is sitting in the high-field region in between two pixels. Additionally, it has been observed that some of the bright pixels show an unstable behaviour of the current with time, whereby the current switches between two levels, i.e. showing so-called Random Telegraph Signal behaviour [253].

A final potential problem area in imagers and IR focal plane arrays can be the read-out electronics (i.e. noise increase in the read-out amplifier, the storage capacitor,...). However, from a viewpoint of displacement damage, little effect is to be expected for typical doses during space missions [239]. Finally, for IR detection, Si read-out electronics operating at cryogenic temperatures is generally combined with some detector material (silicide Schottky barrier, blocked-impurity-band silicon,...). The radiation response of Si:As doped IR detectors at 10 K has been studied recently [254], showing considerable degradation. More details can be found in dedicated reviews [239].

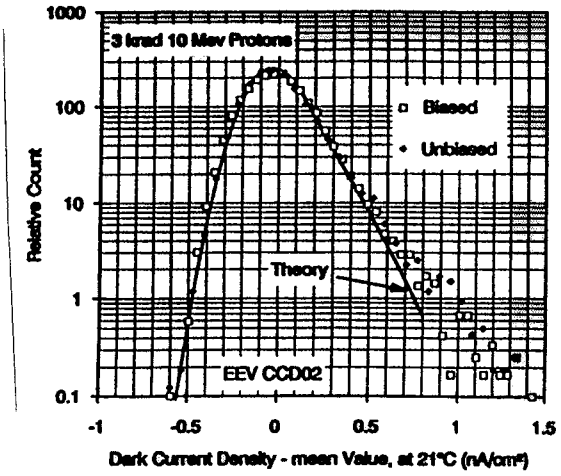

Fig. 122: Histogram of dark current density values for each pixel of two n-buried channel CCDs (mean dark current value has been subtracted). One CCD was biased during irradiation, the other not. Also shown is a theoretical fit (after Hopkinson [239]).

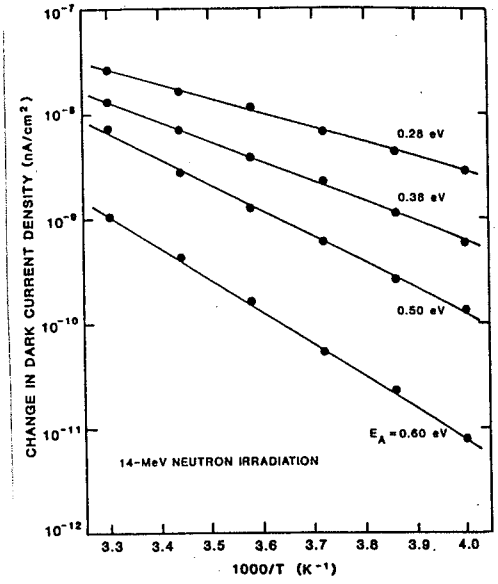

Fig. 123: Change in dark current density versus reciprocal temperature for four cells in a 14-MeV neutron-irradiated CCD (after Srour and Hartman [250]).

Chapter 4

GENERAL CONCLUSIONS

The aim of this chapter is to draw some general conclusions from the extensive literature study in chapters 2 and 3 with respect to the low temperature operation of silicon electronics and more in particular regarding the radiation response. From this, some guidelines for the radiation test plan, given in chapter 5, can be drawn. For the latter it is essential to focus on a number of pertinent questions.

A first key issue is whether or not it is relevant to perform the irradiations at cryogenic temperatures. The answer to this question is different in the case that displacement damage is at stake or the total dose response. One can roughly state that the stable displacement damage created is larger for room temperature irradiations compared with cryogenic irradiations. This follows from the larger introduction rates of the most prominent radiation defects. Of course, the stable defects created at low temperatures can be quite different than the room temperature ones. Anyhow, a marked difference is to be expected for irradiations well above 100 K and below (77 K and 4.2 K), where the vacancy is believed to be immobile and thus creates a number of stable defects in the bandgap. As a conclusion from all this, one can say that the room temperature displacement damage studies can be considered as a kind of worst case situation and therefore are on the safe side.

Total dose effects on the other hand, follow a completely different behaviour. Operation at 77 K prevents the trapped holes first of all to move towards the negative interface and secondly to escape (tunnel), to recombine, to annihilate or to be transformed into interface traps. As a consequence, the degradation of the gate oxide (and field oxides) should be clearly more pronounced at low temperatures. In addition to that, very little information is available with respect to 4.2 K behaviour - of interest for the FIRST mission for example. A related aspect is the effect of single-events on low temperature CMOS devices and circuits. The available studies indicate that the susceptibility towards latchup (or the cross section) increases significantly below $\approx$100 K, which is of concern for cryogenic space electronics. Certainly more data (down to 4.2 K) would be welcome to have an idea about the SE response of CMOS.

A second important item is whether one should harden the technology for cryogenic operation or not and this in view of the recent COTS (custom-off-the-shelf) strategy. There is indeed more and more a tendency to abandon considerable technology hardening efforts and to replace expensive hardened space components by standard commercially available devices. Along with this line goes a strategy for risk management, built-in sufficient redundancy etc.. From a radiation effects viewpoint, the downscaling of technologies in some aspects bears an inherent hardening by the use of thinner gate oxides, different more radiation tolerant isolation schemes and so one, which improves the total-dose response. Of concern, however, become the single-events. In fact, even for non-space, or non-military applications, the DRAM community is concerned about the effect of the natural radiation environment on present-day and future generations of memories.

The sense of this new philosophy may be questioned for cryogenic applications. In many cases, the technology needs to be optimised anyhow for specific cryogenic operation, in order to meet the requirements and to reduce/eliminate some specific low temperature anomalies, like kink and transient effects. Since no standard (off-the-shelve) technology is used, it becomes worthwhile to reconsider the use of hardening techniques in addition to cryogenic hardening. This goes of course at the expense of integration density and an increased processing complexity and risk (lower yield?). The first point, however, is not really an issue for most of the envisaged cryogenic space applications.

Taking into account the dominance of CMOS for cryogenic applications, one should particularly focus on the ionization damage (i.e. total dose and SE).

It is also worthwhile mentioning that bipolar technologies show an inherent better radiation tolerance compared with CMOS. This means that SiGe-based technologies may be attractive alternatives in the "near" future. It probably explains the fast growing interest in radiation studies of these materials and devices. However, little information is available on the radiation response at cryogenic temperatures. In addition, bulk displacement damage may be of concern for the SiGe layers, which seem to be (more) susceptible than silicon. Some radiation aspects of more advanced silicon based technologies will be studied in the second phase of this Work Order.

With respect to the radiation damage response of cryogenic circuits probably the same remark can be made as with respect to hot-carrier degradation. The degradation of a device in many cases gives an overestimation of the observed circuit operation. This may be related to the fact that for many circuits, the operation voltages switch continuously (ac mode of operation), whereby the "damage" experienced during the positive cycle for example, is partially counteracted during the negative cycle. The studies of the individual components are particularly important from a fundamental viewpoint, in order to get a better understanding of the degradation mechanisms involved. Such studies can also be of interest from a technological (hardening) viewpoint, since one can better estimate the effect of a certain technological change. On the other hand, it is strongly felt that it is very risky to extrapolate results obtained at a transistor level to a complete integrated circuit. In other words, it is hard to predict the radiation response based on device simulators. This is the more true for cryogenic operation, where even the low-temperature static device parameters can not be accurately predicted aforehand. In addition, there is insufficient data base to even start thinking of building technology specific cryogenic radiation simulators.

The following general guidelines for defining a radiation test plan should be taken into account:

1/ **Total dose testing** should preferably be done at the operation temperature of interest. This brings along some heavy practical roadblocks as there are not so many radiation facilities available to allow low temperature γ-irradiation **under operation bias** and **in-situ testing**. Alternatively, one can think of irradiating the devices at room temperature (or maybe at low temperature, if no local testing is possible) and to store the device at low temperature (liquid nitrogen?) in between irradiation and cryogenic testing, to prevent considerable annealing. Within the first phase of the present Work Order, the possibilities to perform cryogenic irradiations will be explored. Although technical aspects are the main concern, economical issues will also have to be taken into account.

2/ For displacement damage evaluation, one can consider to perform the irradiations at room temperature, followed later by a cryogenic testing. In-between, one could store the irradiated parts at LNT. An important remark with respect of high energy ion irradiation is that if devices are mounted in a metal cryostat, there can be a serious constraint related to radiation protection. Parts of the cryostat may become activated. Additionally, the metal shielding of the cryostat requires rather high energies for the bombarding particles. These may not be the most relevant energies for the envisaged missions.

3/ It is important to irradiate both circuits and individual devices of the same technology in parallel and under realistic bias conditions. A sufficient amount of circuits should be irradiated at the same time to allow some statistical variation. The irradiation of the circuits are to be considered as go/no go tests and should be for sufficiently high doses, in agreement with the total dose expected during the mission. A detailed evaluation at a component level is essential to gain some fundamental insight into the degradation mechanisms and to evaluate possible hardening measures.

Chapter 5

PROPOSED IRRADIATION PLAN FOR PHASE 1

During the irradiation rounds of phase 1 of this Work Order it is the intention :

* to study the radiation performance of cryogenic circuits, such as envisaged to be used for the FIRST mission;

* to investigate the necessity to perform cryogenic irradiations;

* to analyse in detail the technical difficulties associated with cryogenic irradiations;

* if possible, to have some low temperature irradiations executed.

As the investigations toward the practical feasibility to perform cryogenic irradiations is a part of the present study, this initial irradiation plan will not take into account any cryogenic irradiations. However, the irradiation plan will be modified in case that low temperature irradiation facilities would become available during the execution of the Work Order.

The cryogenic electronics that will be studied are the circuits fabricated by IMEC, and of which the design and fabrication are forming an activity within another Work Order. Whenever possible, IMEC will investigate the possibility to test the radiation hardness of other cryogenic circuits, fabricated by ESA suppliers. If the devices are delivered free of charge, IMEC is willing to perform the radiations free of charge and to inform the supplier on the outcome of the results. Whenever requested, the data concerning the radiation performance can be kept confidential.

IMEC has already developed a first prototype of some FIRST circuits. Therefore, the most promising design will be evaluated from an irradiation hardness viewpoint. Optimised prototypes are presently under fabrication and will in a later stage also be studied form a radiation hardness viewpoint. In order to obtain an insight into the radiation performance of the circuits, it is essential to irradiate in parallel some test structures processed in the same technology. All the IMEC circuits and devices that will be studied within the frame of the present Work Order will be processed in a 0.7 μm CMOS technology.

For the moment it is envisaged to performed the following set of irradiation rounds at Louvain-La-Neuve :

* Irradiation round 1 (proton irradiations)

  - 2x3 FIRST circuits under bias
  - additional test devices (e.g. MOSFETs and field transistors) under bias
  - protons
    * 60 MeV
    *dose : 1×10^{10} cm^{-2} and 1×10^{10} cm^{-2}

In view of the maintenance of the facilities, the irradiations can be performed around Feb-March 1998.

* Irradiation round 2 (γ-irradiations)

- 3 FIRST circuits under bias
- additional test devices (e.g. MOSFETs and field transistors) under bias
- total dose testing according to the FIRST specification
    * γ-irradiations
    * 100 krad

This irradiation round is scheduled for the beginning of 1998.

* Irradiation round 3 (protons)

- similar as irradiation round 1, but on new protoypes

Most likely around the May-June time frame

* Irradiation round 4 (γ-irradiations)

- similar as irradiation round 2, but on new protoypes
- possibly more than one design will be evaluated

This irradiation round should also be scheduled before the 1998 summer holidays.

In view of the general conclusions outlined in chapter 4, it would be highly desirable if the total dose irradiations could also be performed at cryogenic temperatures. In the coming period, the available possibilities will be investigated.

For all irradiation round the devices will be pre- and post-rad tested at cryogenic temperatures. The possibility to transport and store the devices at low temperatures will be investigated.

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