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Work Order 1938/96/NL/LB :

Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials

Radiation Testing of Cryogenic Devices and Circuits

Deliverable D2

C. Claeys and E. Simoen

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Abstract

This report constitutes the Deliverable D2 of Work Order 1938/96/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials". It gives a critical analysis of the extensive amount of pre- and post-irradiation test data on devices and circuits operating at cryogenic temperatures. The circuits are the first prototypes for the FIRST mission and have been processed in an 0.7 μm CMOS technology. Both high energy proton and γ-irradiations have been studied, in agreement with the irradiation test plan outlined in Deliverable D1. Attention is also given to the on-going activities related to the possible irrradiations at cryogenic temperatures. The most important conclusions coming out of the experimental study are summarized and recommendations are given for future activities.

Introduction **ESA_QCA00168T_C**

This reports constitutes Deliverable D2, associated with RFQ/3-8938/97/NL/NB on “Study of Radiation Effects in Cryogenic electronics and Advanced Semiconductor Materials “ – Activity 1 related to Radiation Effects in Cryogenic Electronics. This 18 months activity started with a literature study on the radiation effects in cryogenic electronics, the result of which is summarized in depth in Deliverable D1.

Based on the review, it was decided to have some cryogenic circuits, specially designed as prototypes for the FIRST mission, irradiated with both gamma’s and protons. Along with these circuits, selected test structures were also irradiated. The outcome of a first irradiation round would form the input for the experimental conditions for the execution of a possible second irradiation round. All these irradiations have been performed at room temperature. As the literature study pointed out that, in case of total dose effects, the device performance more severely degrades if the irradiations are done at low temperatures, another task was devoted to investigate the possibility for cryogenic irradiations. This Deliverable gives a detailed overview of all the different experimenal activities that have been performed within the frame of Activity 1.

The report is organized as follows. The first section is related to the pre-irradiation testing of the devices and circuits studied, i.e. processed in the technology anticipated to be used for the circuits of the FIRST mission. Attention is given to both dedicated test structures and cryogenic circuits. As the prototypes are still in the development phase, the impact of several technological parameters on the cryogenic device performance has been studied. Special attention is given to the impact of i) the presence of a lowly doped drain (LDD) region, ii) the use of a threshold voltage adjustment ion implantation, and iii) the use of a p-well region. This section also gives information on the FIRST protoypes that have been studied.

The post-irradiation performance results are given in section 2. Whereas the cryogenic circuits are more giving a go/no go criterion, the analysis of the test structures allows to obtain insight into the device degradation mechanisms. Therefore both test structures and FIRST prototype circuits have been irradiated by high energy protons and gamma’s, respectively. These two different types of irradiations should give information on both the displacement damage and the total dose effects.

The third section is discussing the actions and the status of the work going on at IMEC in order to create the possibility to perform cryogenic irradiations.

The most important conclusions of the work are summarized in section IV, together with some recommendations for future activities.

I. PRE-IRRADIATION CRYOGENIC CHARACTERIZATION OF THE DEVICES AND CIRCUITS

In this sections of the report the pre-irradiation characteristics at 4.2 K of the FIRGA transistors, which were processed at Alcatel-Microelectronics (Aμe) (run E740632A) are described. This is part of the global pre-irradiation characterization of the devices and circuits which have been irradiated within the framework of the present ESA contract (1938/96/NL/LB). In a first paragraph the experimental (processing) matrix will be described as well as the measurement procedures. In addition, information is given on the studied cryogenic circuits. The second paragraph gives an overview of the obtained current-voltage (I-V) characteristics in linear operation and in saturation. In the third paragraph, a summary is given of the main static parameters: the threshold voltage V_T, the (maximum) transconductance g_m and the subthreshold swing S. Next, the reproducibility/stability of the 4.2 K measurements is briefly touched on. Finally, the main trends observed during the present study are briefly summarized.

I.1. Experimental Device and Circuit Aspects

I.1.1 Experimental Processing Matrix and Test Procedures

Test structures have been mounted from 8 processing splits of AμE run E740632A, which was processed in a modified 0.7 μm CMOS technology. The technological splits are described in Table I.1 Wafer 1 represents the AμE standard 0.7 μm technology, with a p-well. The different processing splits are related to the presence of a p-well (wafers 1,6,9,11) or not (wafers 13,16,19,22); the application of Lowly Doped Drains (LDD) (wafers 1,9, 13,19) or not (wafers 6,11,16,22) and the implementation of a threshold voltage adjustment ion implantation (wafers 1,6,13,16) or not (wafers 9,11,19,22). A LDD approach for the transistor engineering is mainly used for suppressing possible hot carrier effects during device operation and relies on a control/shift of the maximum electrical field near the drain region. A possible negative effect is an increase of the source/drain series resistance, especially for cryogenic device operation [1]. The processing conditions of wafer 6 are closest to the standard AμE 0.7 μm technology used for foundry services. It is expected that these processing parameters can have a strong impact on the performance at 4.2 K, i.e. on the V_T, the g_m and kink and hysteresis effects. Based on the pre-irradiation characteristics a selection has been made of the processing splits (i.e. transistors and circuits) which are further studied in detail during the high-energy protons and ^{60}Co γ-irradiations. The post-irradiation results are described in section II.

From each wafer corresponding with a particular processing split, 10 test chips were mounted in 24 pins dual-in-line packages (DIL). The layout of the test chips is given in Fig. I.1, while the bonding pad configuration can be found in Fig. I.2. There are per package in total 3 n-channel and 4 p-channel MOSFETs available for testing. The dimensions and acronyms of the different test structures used are summarized in Table I.2 The cascode transistor (CASC) consists of a dual-gate structure, whereby two MOSFETs of the same length L are placed in series. Both gates can be connected separately, which can be beneficially used to suppress kink effects at 4.2 K. For the present measurements, the two gate contacts are connected together, so that the

transistor in first order behaves as a double length n-MOSFET (20 μm). The circular transistor (CIRC) is a closed geometry device with an inner source surrounded by the drain. The inner perimeter is 100 μm and the length 5 μm. The isolated p-MOSFET (ISO) transistor has an isolated source and gate contact, while the other three p-MOSFETs are part of the same array. The latter implies a common drain and common gate structure, respectively.

Table I.1. Description of the processing splits used for the fabrication of the transistors to be pre-irradiation tested at 4.2.

Wafer	**p-well**	**V_T adjust**	**LDD**
1	+	+	+
6	+	+	
9	+		+
11	+		
13		+	+
16		+	
19			+
22			

Table I.2. Dimensions of the available transistors.
*only p-MOSFETs.

Transistor	**Acronym**	**Area WxL (μm^2)**
Isolated	ISO*	10x5
Single	SING	10x5
Circular	CIRC	100x5
Cascode	CASC	20x5

The electrical testing is performed in a liquid helium tank, using a dedicated in-house designed measurement probe as described in detail in Ref. 2. Before starting with the liquid helium temperature (LHT) testing, a short room temperature characterization of the devices has been done on 3 out of the 5 arrays in order to check the bonding yield. A good agreement between the extracted parameters at room temperature (RT) and the electrical test data provided by AμE has been found. The full details of the original electrical test data can be found in reference 3.

The I-V characteristics of the devices have been measured using an HP4145 Parameter Analyzer. In linear operation, a drain bias V_{DS} of +25 mV (n-channel) or -25 mV (p-channel) was applied, while the gate voltage V_{GS} was varied from 0 V to + 5 V or -5 V, respectively. The threshold voltage was derived using the linear extrapolation technique. This means in practice that the tangent was drawn to the point of maximum transconductance. The intercept with the gate voltage axis gives $V_{Textrap}$. The threshold voltage is then obtained by subtracting (or adding in case of p-MOSFETs) $V_{DS}/2$=12.5 mV. A zero substrate bias was applied, whereby for the n-MOSFETs the substrate contact was connected to the p-well contact.

The subthreshold slope S is derived from a log I_D versus V_{GS} plot, whereby a value for the initial slope is obtained (initial part of the curve). It is known from past experiments that S at 4.2 K is not a constant but shows a variation with V_{GS} (or the drain current I_D) [4]. This is thought to be related to an increase of the density of interface traps, due to a shift of the Fermi level closer to one of the band edges for a lowering of the device operating temperature.

Next, the device characteristics in saturation have been obtained for gate voltages of 1 to 5 V in absolute value (1 V step). Both the drain (I_D) and the substrate current (I_B) have been measured up to a drain bias of 5 V. This should clearly reveal the presence of a possible kink effect at 4.2 K. By comparing the device characteristics for a V_{DS} sweep from low to high, with those for a high to low sweep, the occurrence of possible transient and hysteresis effects can be revealed. More details on the physical origin of these effects have been given in ref. [1].

In most cases, four complete transistor arrays per split have been measured at 4.2 K. However, not all of the devices tested worked properly at LHT, so they were not included for further irradiation tests. The sometimes non-functioning of the devices is due to the handling procedures.

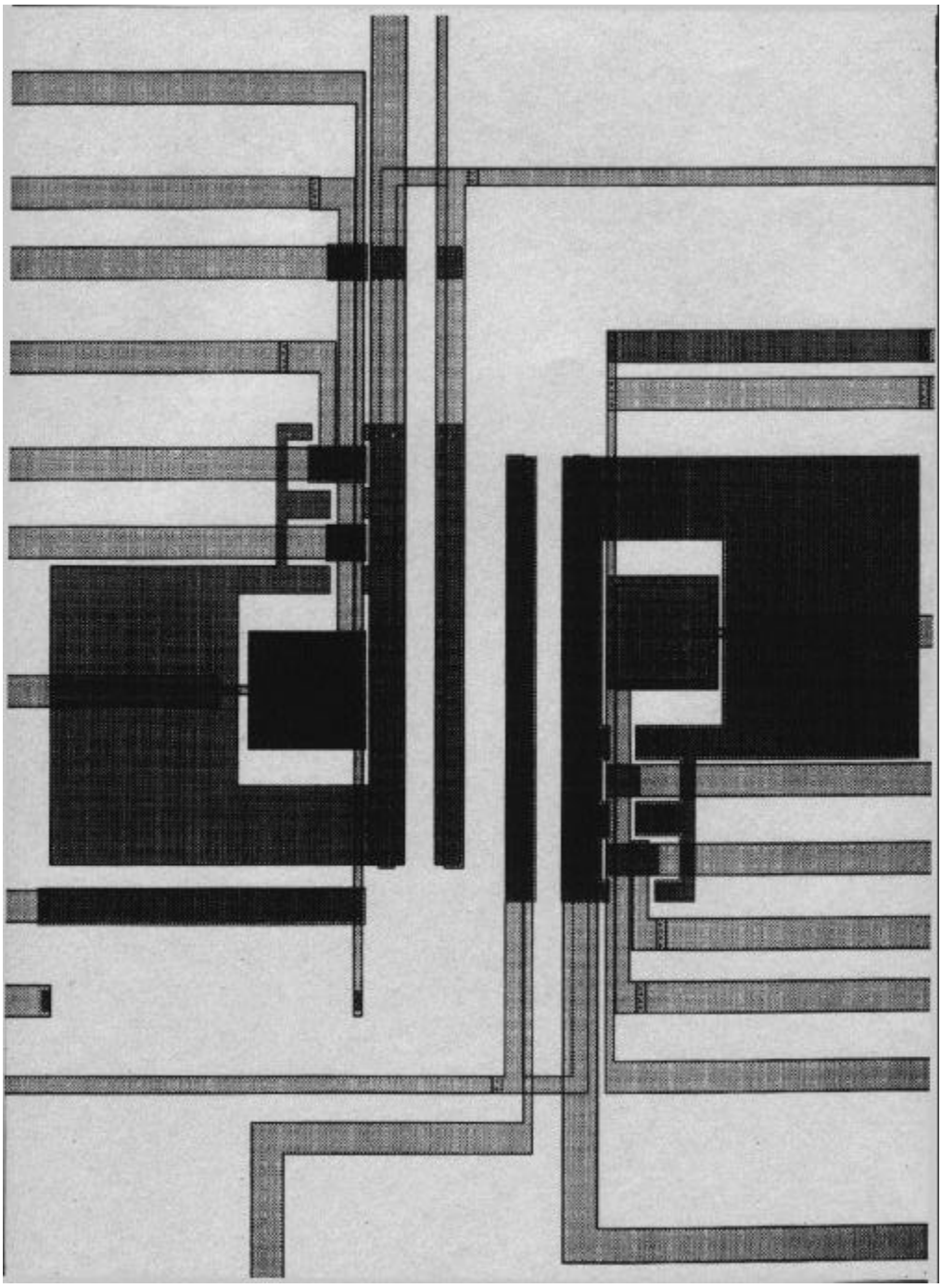


Fig. I.1. Layout of the test chip.

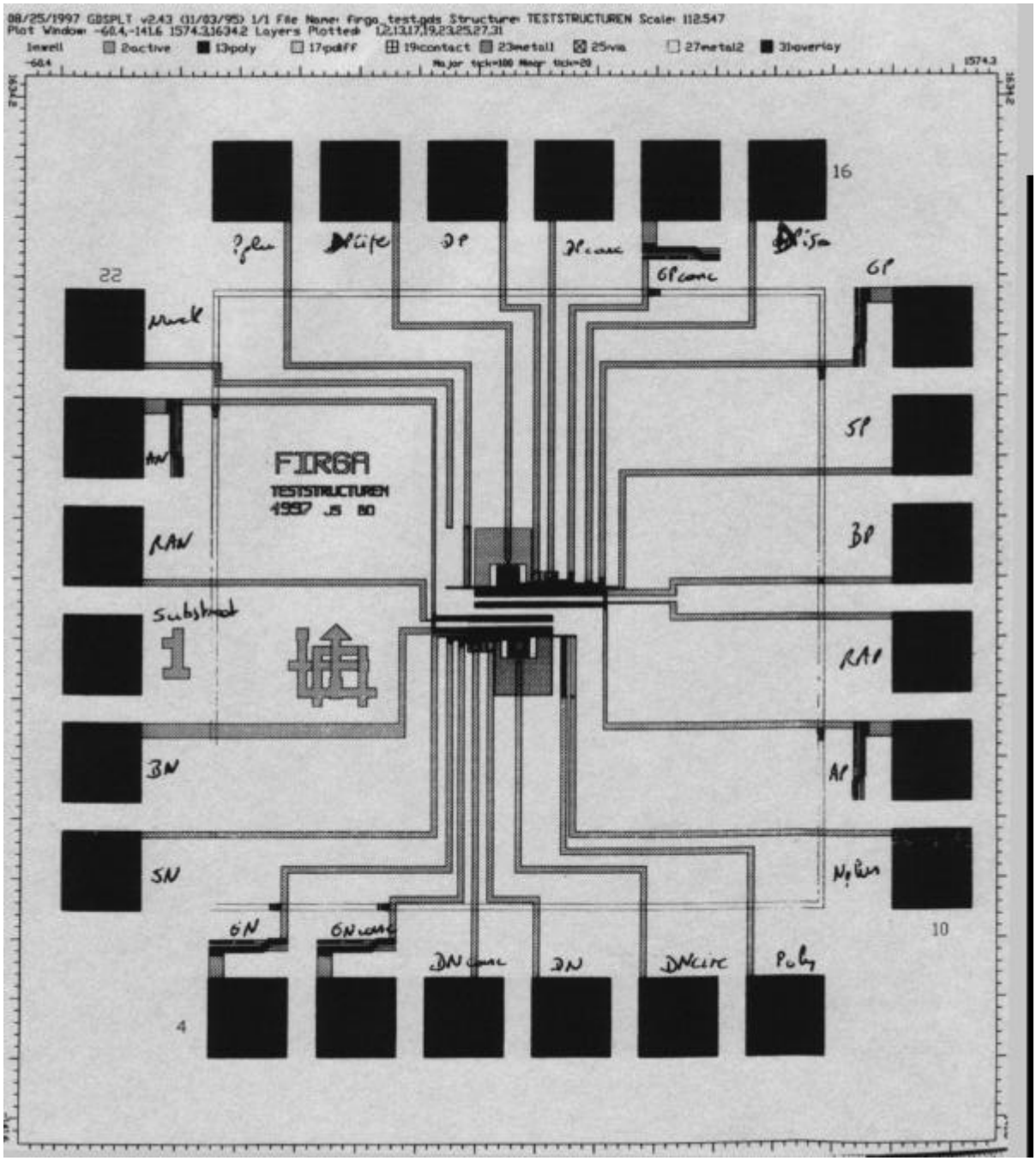


Fig. I.2. Bonding pad configuration

I.1.2. FIRGA cryogenic circuits

At IMEC the design of cryogenic readout electronics is focussing on the prototypes for the FIRST mission. FIRST, which stands for Far-infrared and Submillimeter Space Telescope is the successor of IRAS (1983) and the satellite is scheduled to be launched in 2005. The scientific objectives are:

- Far IR till mm wave mapping of the sky (80 µm to 1 mm wavelength)
- The submillimeter gap (300-1000 µm) is yet unexplored
- Spectroscopy of the insterstellar medium
- Cosmology and early evolution of galaxies
- Search for protostars
- Primitive matter in the solar system

The spectral range is divided in three bands covering the total wavelength range:

80 µm to 250 µm : 16 * 16 pixels stressed Ge:Ga photodetectors : FIRSA
250 µm to 700 µm : Bolometer detectors
700 µm to 1300 µm : Heterodyne receivers

The operational constraints for the readout electronics are:

• Operating Temperature	1.8K
• very low power dissipation	100 µW / 16 detector channels
• very low bias voltage	20 mV ± 2mV ± 0.2mV
• Five decades of photocurrent	10 fA to 1nA

The original design is called the FIRSA, while the modified design is referred to as the FIRGA. The main differences between the two designs are related to the fact that the following modifications have been implemented [5]: i) removal of the design mistakes, ii) bias preservation by means of a DC voltage instead of MOS devices, iii) improvement of the noise performance by changing the W/L of the devices in the cascode amplifier, iv) addition of a zero bias circuit, v) increase of the integration capacitance, vi) implementing a n-well plug next to each nMOST, vi) solving the debiasing problem, and vii) adding some additional circuitry. The basic design concept of the SARP2 and SARP3 blocs are given in Figs I.3a and I.3b. SARP3 is reducing the debiasing by means of a 3 stage amplifier and places the feedback integration capacitance only over the first stage amplifier. Simulations have shown when the feedback integration capacitance is placed over the whole amplifier, in some case the circuit may be unstable. The basic building bloc of SARP2 and SARP3 is thus identical. However, the two extra stages with amplification 3, and feedback for bias preservation, reduces the total debiasing with a factor of 10. The full cryogenic circuit is a linear array of 16 single SARP amplifiers to read out 16 stressed Ge:Ga detectors.

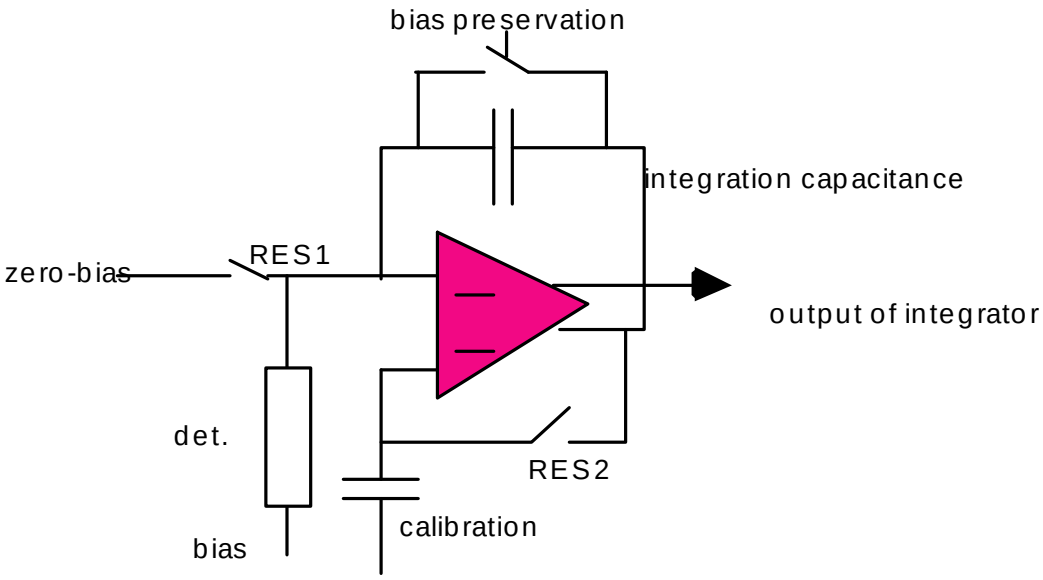


Fig. I.3a. Schematic representation of the SARP2.

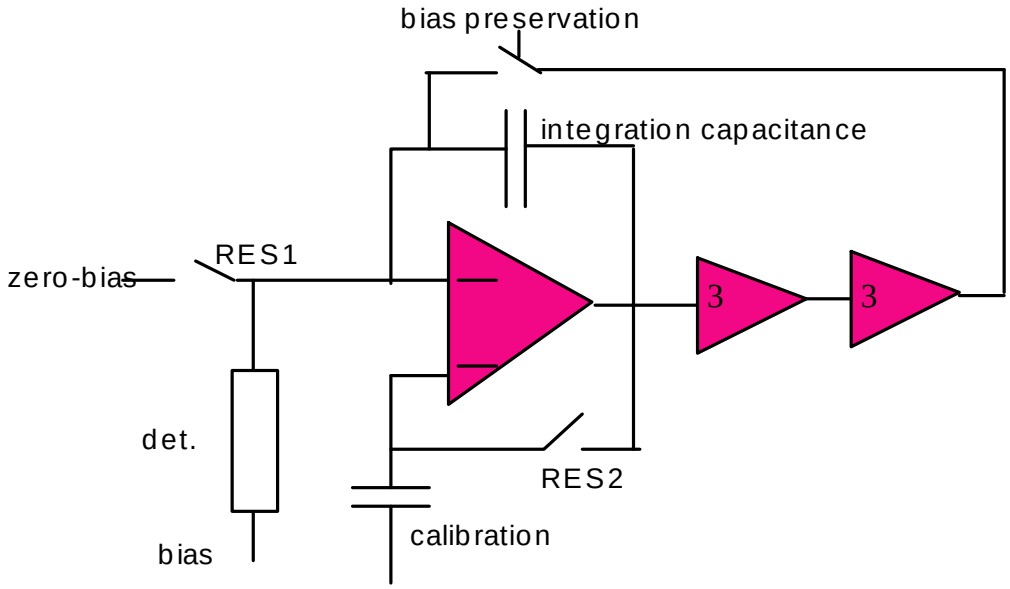
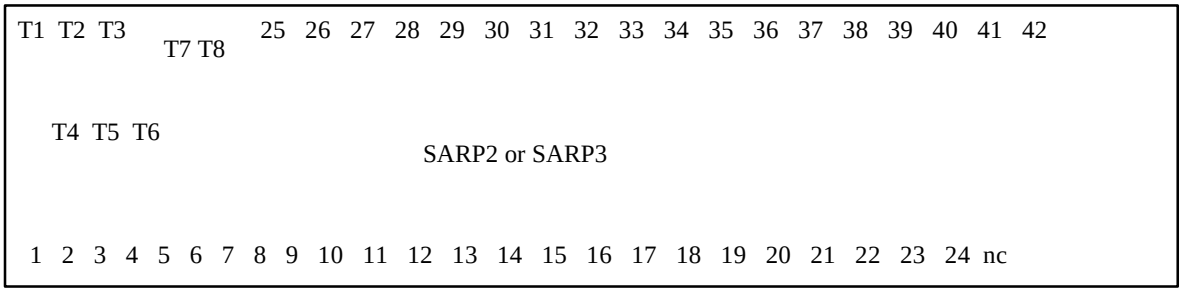


Fig. 1.3b.Schematic representation of the SARP3.

The pin configuration for the SARP2 and SARP3 circuits is given below



Pin	Name	Functionality
1	Vddd	Digital power supply (5V)
2	slow/fast	0 : slow , 5V : fast. Influences the slope of the digital signals
3	zero_bias	output signal of the zero bias circuit.
4	select	0 : standby mode , 5V : on-mode
5	clock	clock signal (10-20kHz) (see timing)
6	sync	Determines DR or NDR (see timing)
7	gnd	digital ground
8	well	well supply voltage (5V)
9	eos	end of scan output signal (see timing)
10	sub	substrate voltage (0V)
11	out	analog output signal from the transimpedance amplifiers
12	vddo	supply voltage for the output stage of the amplifiers (5V)
13	sel1	select signal for integration capacitance
14	sel2	select signal for integration capacitance
15	Zb	input zero bias signal for the amplifiers
16	rcmon	connected to 10 Mohms to vdda
17	gnd	analog ground
18	orv	via capacitance of few nF to vdda. input pmos-casc of the analog part
19	cascn_log	input nmos casc. of logic part. Normally connected with gcm2
20	cascp_log	input pmos casc. of logic part. Normally connected with orv
21	gcm2	via 5Gohms to vdda and capacitance to ground
22	vdda	supply voltage analog part (5V)
23	gcm1	1st nmos casc input of the analog part. Normally not used
24	bias-pres	bias preservation signal (2-5V)
25-42	det 1 - 18	detector inputs 1 to 18
T1-3	temp1-3	pads for temperature diodes
T4	inv_sample	testpad for testing signal inv_sample
T5	sample	testpad for testing signal sample
T6	precharge	testpad for testing signal precharge
T7	res1	testpad for testing signal res1
T8	res2	testpad for testing signal res2

Fig. I.4. Pin configuration and pin functionality for the SARP2 and SARP3 circuits.

I. 2. Pre-Irradiation Transistor Characteristics at 4.2 K

I.2.1. Linear characteristics

The linear characteristics obtained on the 10x5 and on the cascode n-MOSFETs of a wafer-1 array (standard AμE 0.7 μm processing) are summarized in Fig. I.5a. The corresponding transconductance $g_m=\partial I_D/\partial V_{GS}$ is represented in Fig. I.5b. A clear shift in the subthreshold region for the different type of structures is observed in Fig. I.5a, pointing to a large spread in V_T. The transconductance behaviour shows an unusual flat behavior for LHT operation [6]. Similar trends are observed for the corresponding p-MOSFETs, as illustrated in Figs I.5c and I.5d.

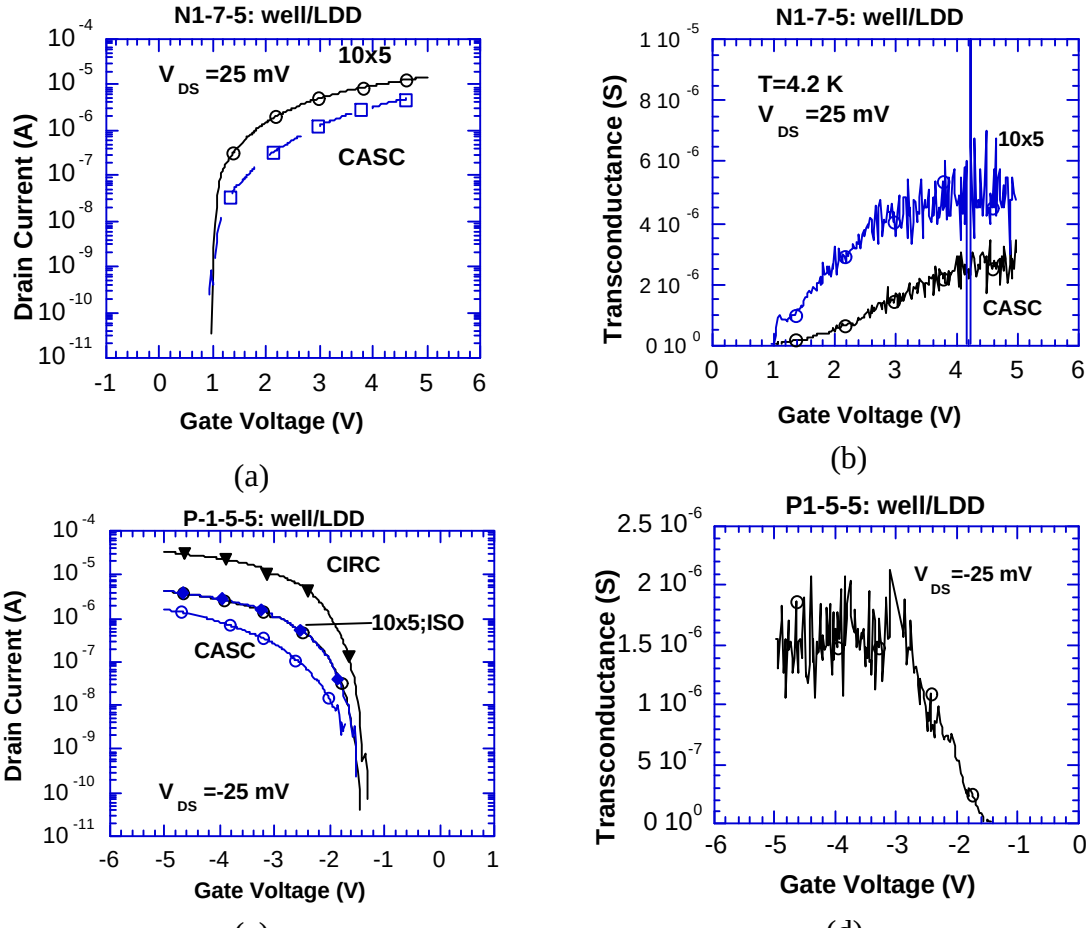


Fig. I.5. Linear characteristics of n- (a and b) and p-MOSFETs (c and d) for the standard process split (wafer 1), at 4.2 K.

A quite different picture is observed in Fig. I.6 for the Wafer 6 (i.e. No LDD implemented) devices at 4.2 K. Maybe the most pronounced difference is the transconductance behavior, which shows the expected peak-shape curve, for both the n- (Fig. I.6b) and the p-MOSFETs (Fig. I.6d). This peak-shaped behavior is explained by considering the two dominant mobility scattering mechanisms at liquid helium temperature: on the one hand Coulomb scattering at ionized dopant impurities and on the other scattering due to oxide charges at low V_{GS} and surface roughness scattering at high gate voltages [6]. Note also that the peak g_m is a factor 10 larger than in the case of

Fig. I.5b and I.5d. The curves are also better grouped together, suggesting a low spread in V_T (see section I.3). Furthermore, the onset of the curves comes at lower V_{GS}, implying a lower V_T. As the only difference between split 1 and 6 is the presence/absence of the LDD it can be concluded that the reduction of the maximum transconductance and the higher V_T are due to the presence of a LDD. It has been demonstrated in the past that in case of an LDD device, the measured transconductance can be written as [7]:

$$\frac{1}{g_{mmeas}} = \frac{1}{g_{mi}} + R_{ds} \qquad (1)$$

with g_{mi} the intrinsic (channel) transconductance and R_{ds} the series resistance, mainly determined by the LDD regions. Assuming a negligible R_{ds} in case of a non-LDD device of wafer 6, a value of $R_{ds} \cong 200\ k\Omega$ is estimated for the n-channel devices of wafer 1. This rather high value points to the occurrence of significant carrier freeze-out in the LDD regions [7-9]. Furthermore, from previous studies it is expected that the transconductance of LDD n-MOSFETs will increase significantly after low-temperature irradiation, while the opposite is true for the p-MOSFETs. This is related to the ionizing radiation induced positive charge build-up in the spacer oxides above the LDDs [7-8].

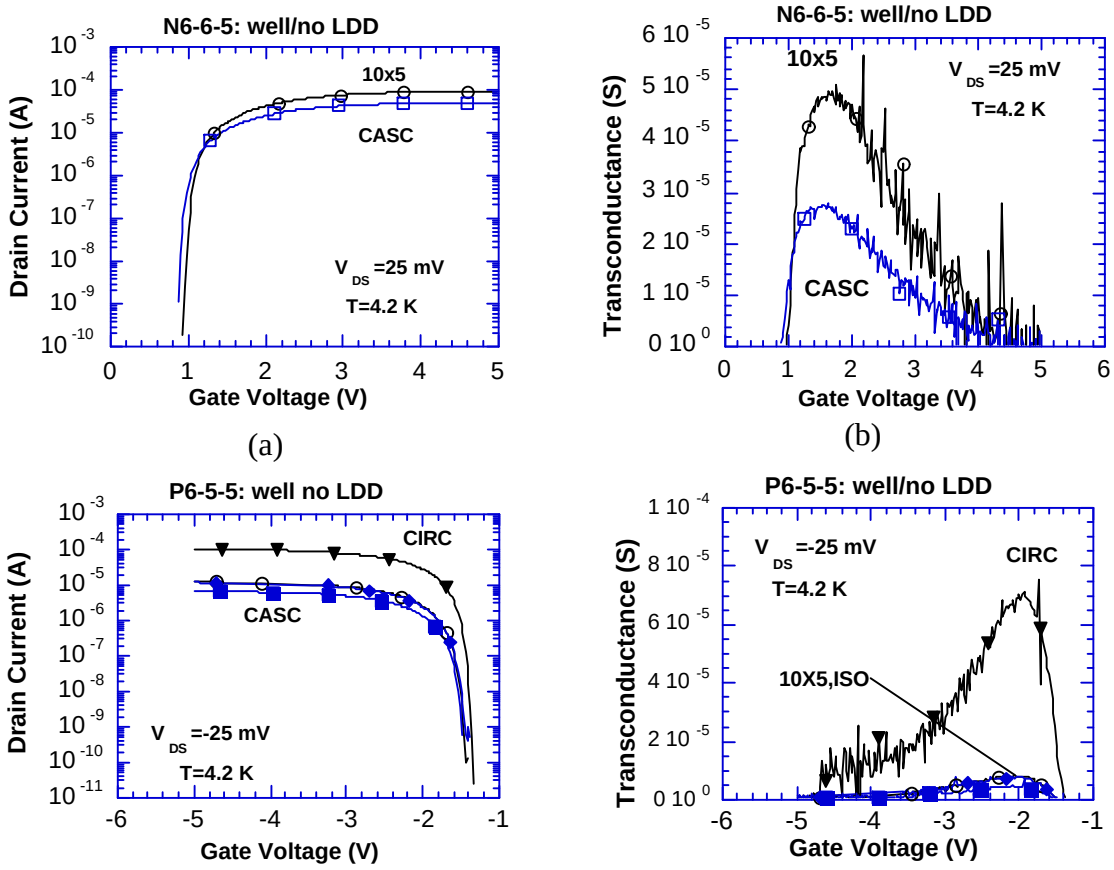
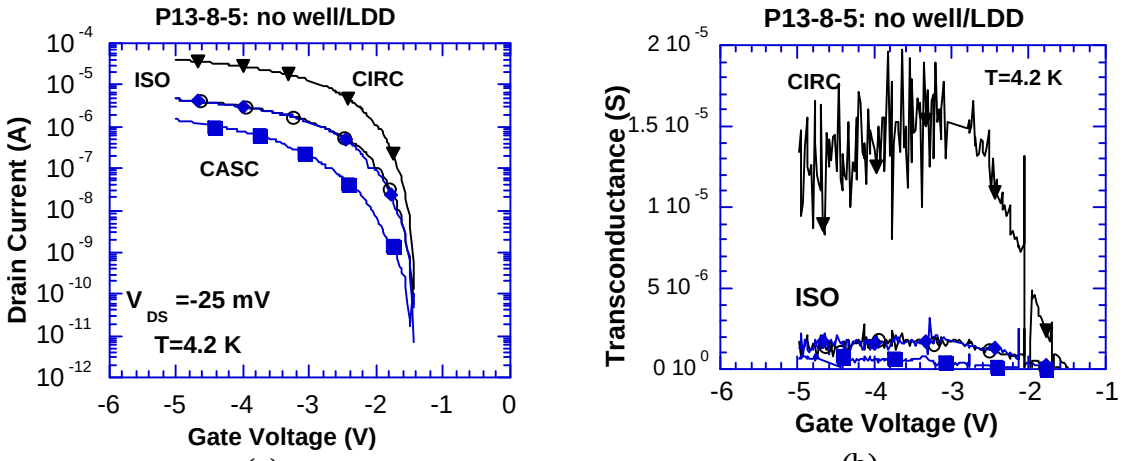


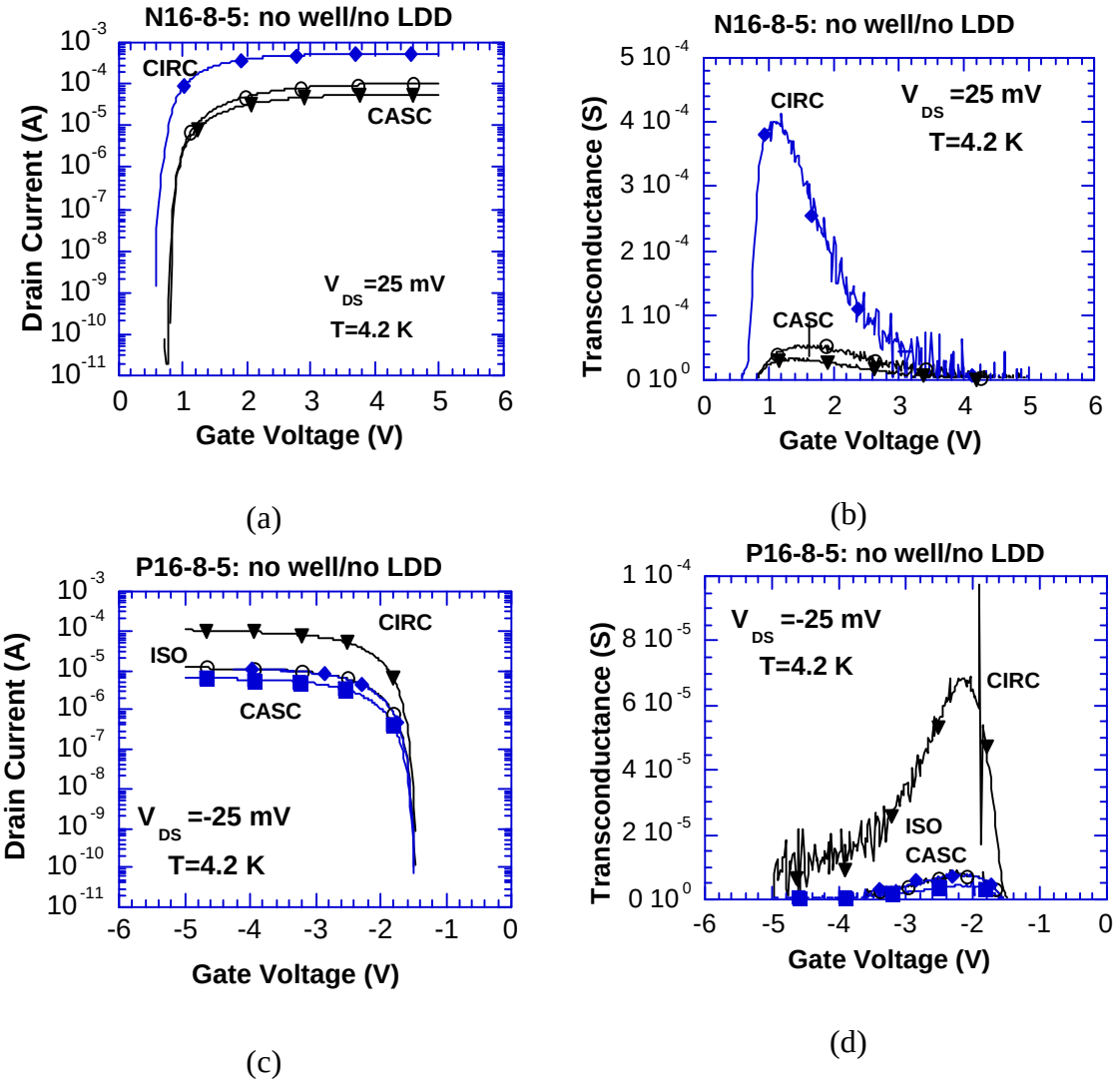
Fig. I.6. Input characteristics of the wafer 6 (i.e. no LDD) n- (a and b) and p-MOSFETs (c and d).

Qualitatively the same picture is observed for the no p-well devices of wafer 13, (Figs I.7) and 16 (Fig I.8; no LDD).



(a) (b)

Fig. I.7. Input characteristics of the wafer 13 (no well/LDD) p-MOSFETs at 4.2 K.



(a) (b)

(c) (d)

Fig. I.8. Input characteristics of the wafer 16 (no well/no LDD) n-(a and b) and p-MOSFETs (c and d) at 4.2 K.

I.2.2. Saturation.

The electrical output characteristics at 4.2 K of the standard and the wafer 6 splits are summarized in Fig. I.9, for a 10 µmx5 µm n-channel (a and c) and p-channel MOSFET (b and d). No clear kink or hysteresis effects are discerned. This implies that the role of the LDD in this case - for reducing the generation of the multiplication current - is not very pronounced. Taking account of the favorable static characteristics (see also section I.3), a clear preference goes to split 6, which also deviates only slightly with respect to the standard processing condition.

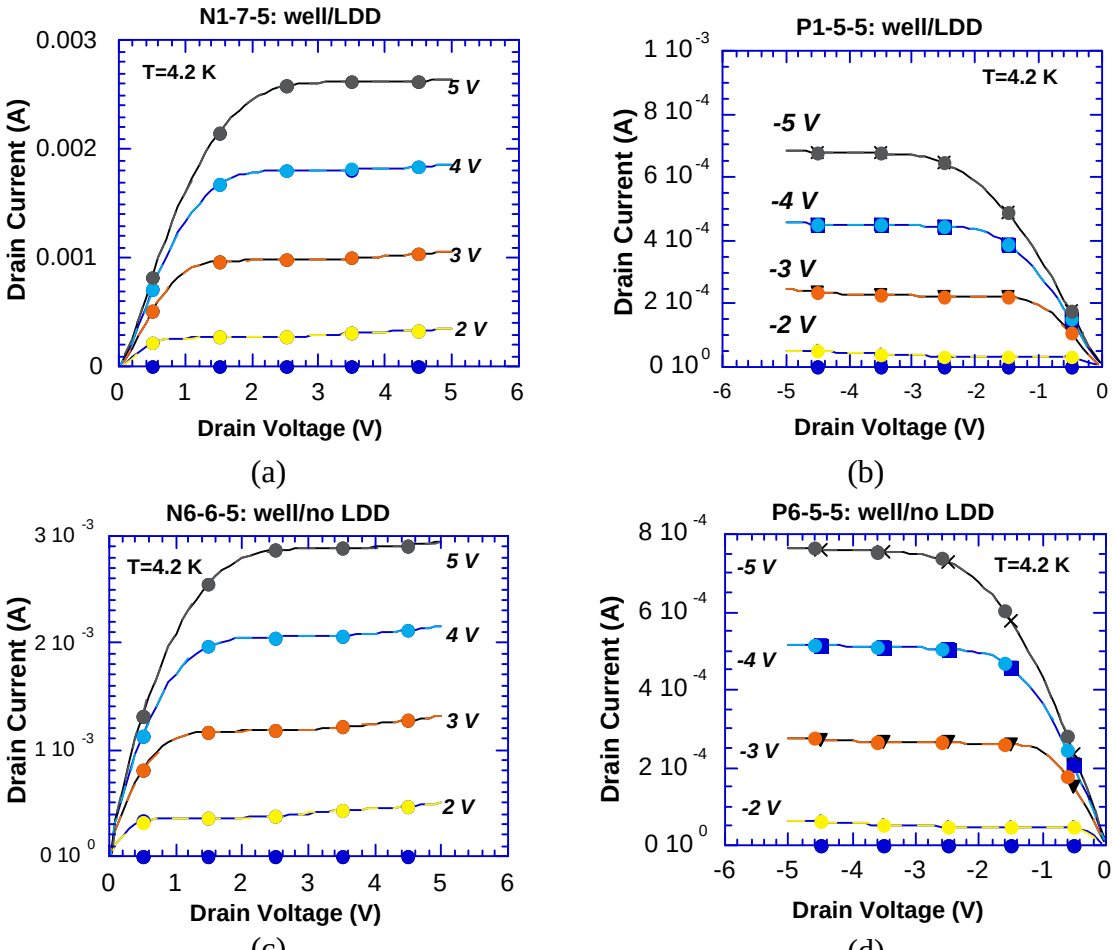


Fig. I.9. Output characteristics at 4.2 K of a 10 µmx5 µm n- (a and c) and p-MOSFET (b and d) of splits 1 and 6, corresponding to a p-well and LDD (a and b)/no LDD (c and d), respectively.

However, for some process splits, kink and hysteresis phenomena are observed for the n-MOSFETs, as illustrated by Fig. I.10. Comparing for example Fig. I.10a with I.10b, it is clear that for no LDD and no threshold adjustment implantation, a clear kink develops. The absence of the adjustment implant gives rise to a lower threshold voltage for the n-MOSFETs and hence a larger saturation current (see e.g. Fig. I.9). The presence of an LDD is here critical for the suppression of the kink effect (a and b). The reason why wafer 11 is more susceptible to the kink effect could be a combination of

two factors: omitting the extra adjustment implantation lowers the density of ionized scattering centers at 4.2 K. This means that due to this reduced probability for a Coulomb scattering the electrons on the average can gain more energy in the field. In other words, they have a higher chance to undergo an impact ionization event. This can be suppressed by lowering the maximum electrical field near the drain by the implementation of a LDD region. Support for this idea is also delivered by the observation that the transconductance (mobility) is highest for wafer 11 (see part I.3). Further insight can be gained by studying more in detail the behavior of the substrate current.

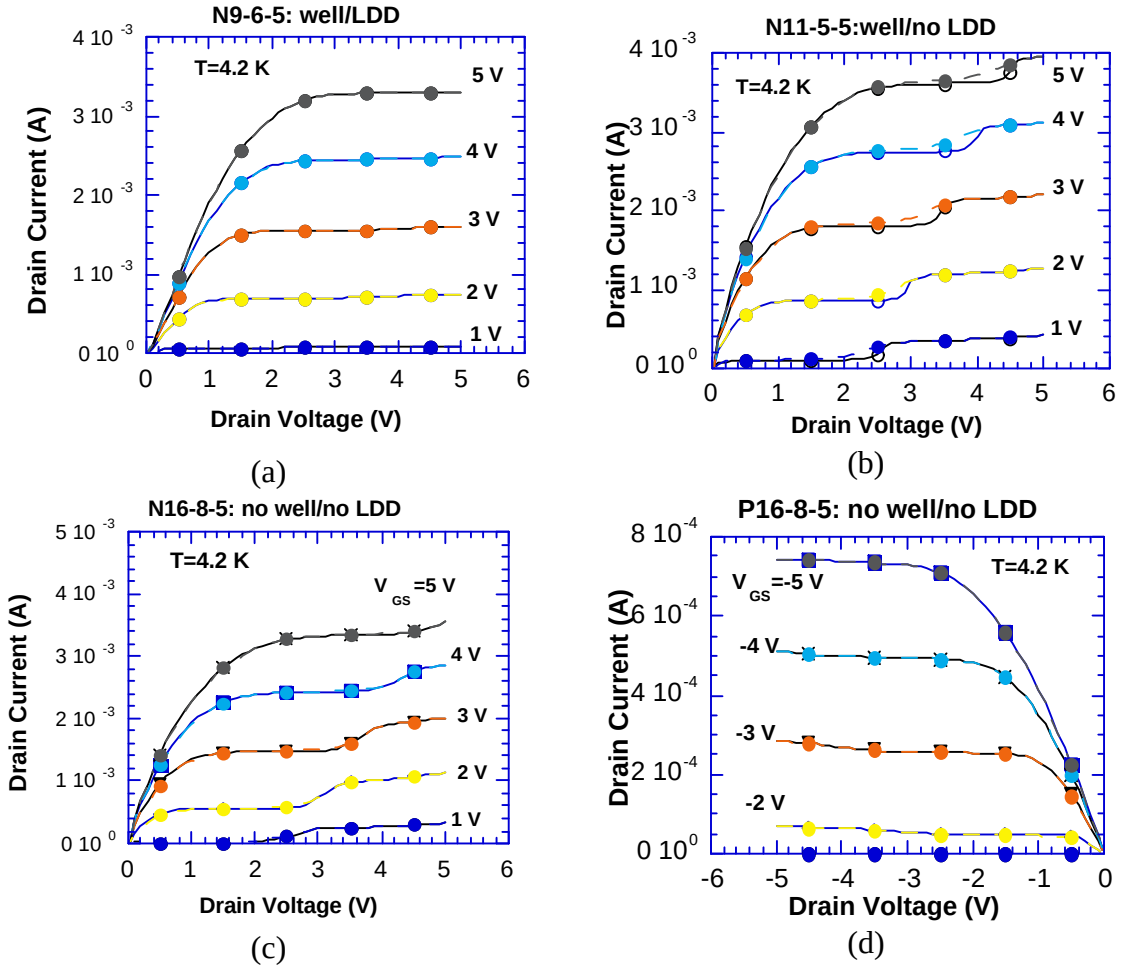


Fig. I.10. Output characteristics at 4.2 K for a 10 µmx5 µm n-MOSFET of split 9 (a); 11 (b) and 16 (c) and a p-MOSFET of split 16 (d).

The tendency for kink and hysteresis formation is enforced in the absence of a p-well, as evidenced by Fig. I.10c. This is not a surprise as it is known that the resistance of the path towards the substrate contact plays a crucial role in the kink generation [10-11]. The lower p-doping of the substrate leads to a higher series resistance at 4.2 K. This in turn creates a higher potential drop when a small substrate current is flowing. As a consequence, a larger increase in the substrate potential is induced and, hence, the threshold voltage is lowered more. The role of the LDD is again understood by a reduction of the primary cause, namely the multiplication occurring near the drain. The splits 19 and 22 yield depletion mode MOSFETs at 4.2 K and are therfore not further considered here.

Summarizing the electrical measurements so far, for obtaining a kink-free output characteristics, the optimal choice is a p-well, a V_T adjust and no LDD (split 6).

I.3. Static Device Parameters at 4.2 K

As already indicated previously, the processing conditions have a marked impact on the key static parameters. Most of the results obtained at 4.2 K are schematically summarized in Fig. I.11 (threshold voltage) and Fig. I.12 (maximum transconductance). The subthreshold slope can be found in Table I.3, which gives all results obtained so far.

Table I.3. Static parameters of all transistors characterized before irradiation at 4.2 K.

#1-5-5	N10x5	1.87	11.4	28.3
	NCIRC	1.48	41.4	22.6
	NCASC	2.43	3.0	11.5
	PISO	-2.17	1.7	45.2
	P10x5	-2.26	2.0	?
	PCIRC	-1.88	12.5	51.3
	PCASC	-2.90	0.8	?
#1-7-5	N10x5	1.95	5.2	21.0
	NCIRC	1.65	41	19.8
	NCASC	2.7	2.85	62.8
	PISO	-2.3	1.6	40.4
	P10x5	-2.08	1.5	32.8
	PCIRC	-2.00	15.0	26
	PCASC	-3.26	0.74	18.5
#6-5-5	N10x5	1.02	46.6	22.4
	NCIRC	0.93	351	17.5
	NCASC	1.03	29	49.1
	PISO	-1.56	8.1	30.3
	P10x5	-1.56	7.7	42.8
	PCIRC	-1.48	71	14.8
	PCASC	-1.67	4.6	24.4
#6-6-5	N10x5	1.02	49.0	17.9
	NCIRC	0.91	349	15.9
	NCASC	0.94	27.5	18.8
	PISO	-1.50	7.6	28.9
	P10x5	-1.58	7.7	18.1
	PCIRC	-1.55	66	21.6
	PCASC	-1.62	4.3	56.5

Table I.3. Static parameters of all transistors characterized before irradiation at 4.2 K.

Array	**Transistor**	**V_T (V)**	**g_{mmax} (μS)**	**S (mV/dec)**
#9-5-5	N10x5	--	--	--
	NCIRC	--	--	--
	NCASC	--	--	--
	PISO	-2.12	1.7	30.0
	P10x5	-2.25	1.8	30.7
	PCIRC	-2.03	13.3	49.6
	PCASC	-2.16	0.3	77.5
#9-6-5	N10x5	1.59	5.8	17.5
	NCIRC	1.25	42.4	16.1
	NCASC	2.44	3.5	16.4
	PISO	-2.40	1.9	54.9
	P10x5	-2.19	1.8	41.9
	PCIRC	-2.17	13.9	20.1
	PCASC	-2.56	0.7	24.1
#11-5-5	N10x5	0.640	66.6	18
	NCIRC	0.562	476	21.3
	NCASC	0.660	41.3	19.1
	PISO	-2.04	5.9	36.6
	P10x5	-2.04	5.8	36.8
	PCIRC	-2.01	50.2	35.2
	PCASC	-2.08	3.4	49.1
#11-6-5	N10x5	--	--	--
	NCIRC	--	--	--
	NCASC	--	--	--
	PISO	--	--	--
	P10x5	--	--	--
	PCIRC	--	--	--
	PCASC	--	--	--

Table I.3. Static parameters of all transistors characterized before irradiation at 4.2 K.

Array	**Transistor**	**V_T (V)**	**g_{mmax} (μS)**	**S (mV/dec)**
#13-8-5	N10x5	--	--	--
	NCIRC	--	--	--
	NCASC	--	--	--
	PISO	-2.51	2.4	53.2
	P10x5	-2.18	2.0	18.6
	PCIRC	-2.07	17.1	17.1
	PCASC	-2.73	0.6	72.8
#16-8-5	N10x5	0.89	52.5	15.9
	NCIRC	0.67	400	19.9
	NCASC	0.84	32.1	13.9
	PISO	-1.60	7.9	15.9
	P10x5	-1.61	7.8	17.7
	PCIRC	-1.62	68.9	31
	PCASC	-1.62	4.3	30.6
#19-5-5	N10x5	0.82	6.1	17.7
	NCIRC	0.69	43.2	14.8
	NCASC	1.85	7.9	14.6
	PISO	-2.25	1.9	47.7
	P10x5	?	?	?
	PCIRC	-2.15	15.4	23.3
	PCASC	-2.77	0.8	49.5
#6-6-5	N10x5	1.09	5.6	18.7
	NCIRC	0.85	46.6	16.7
	NCASC	2.0	3.3	16.8
	PISO	-2.30	1.9	53.2
	P10x5	-2.16	1.5	79.9
	PCIRC	-2.21	15.0	39.1
	PCASC	-2.66	0.6	15.1

Summarizing the results for the n-MOSFETs: reasonable values of V_T (=1 V) are obtained at 4.2 K for the non-LDD devices. At the same time, the device-to-device spread is lower for the non-LDD condition. Most likely this is associated with the rather low bias voltage used (25 mV) which may cause more variation in series resistance (by e.g. the variation at wafer level of the spacer width). Leaving out the V_T adjustment implant yields the lowest thresholds for the n-MOSFETs at 4.2 K but rather large values for the p-MOSFETs as seen in Fig. I.9b. In summary, the most symmetric V_T behavior at 4.2 K is observed for process split 6, which at the same time yields reasonably low values (=1.5 V in absolute value) and a good sample-to-sample reproducibility.

A similar conclusion is reached with respect to the maximum transconductance: roughly a decade higher g_{mmax} is found for the non-LDD splits, both for n- and p-channel devices. This corresponds to the presence (absence) of the transconductance peak in linear operation, noted in Figs I.2 and I.3. As remarked before, omission of the V_T adjust has a beneficial impact on the mobility and g_m (Fig.I. 10).

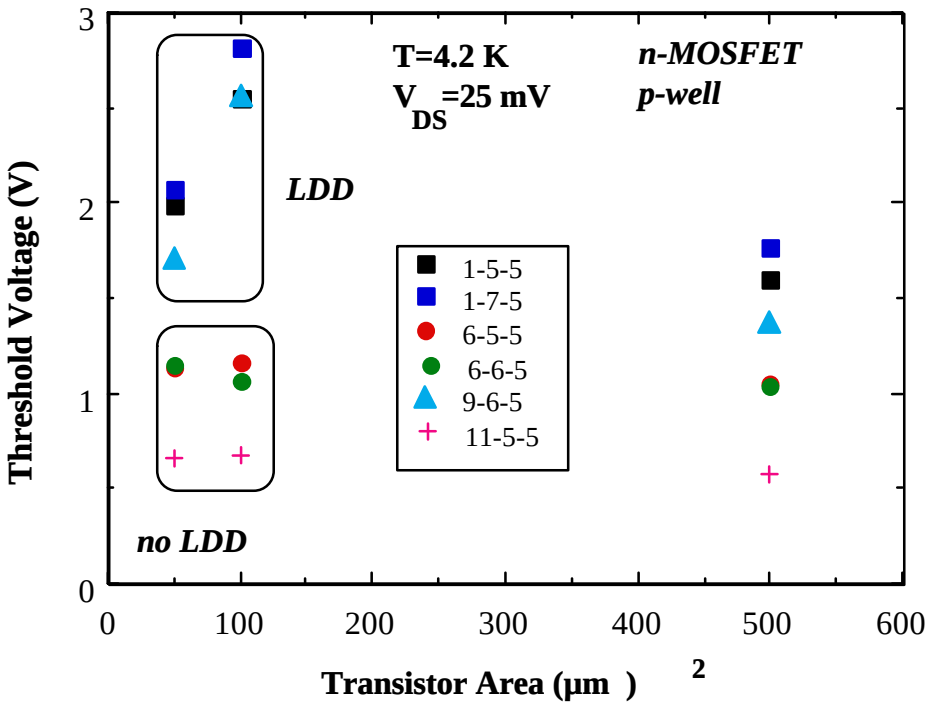


Fig. I.11a. Threshold voltage as a function of device area and processing split for the n-MOSFETs processed in a p-well.

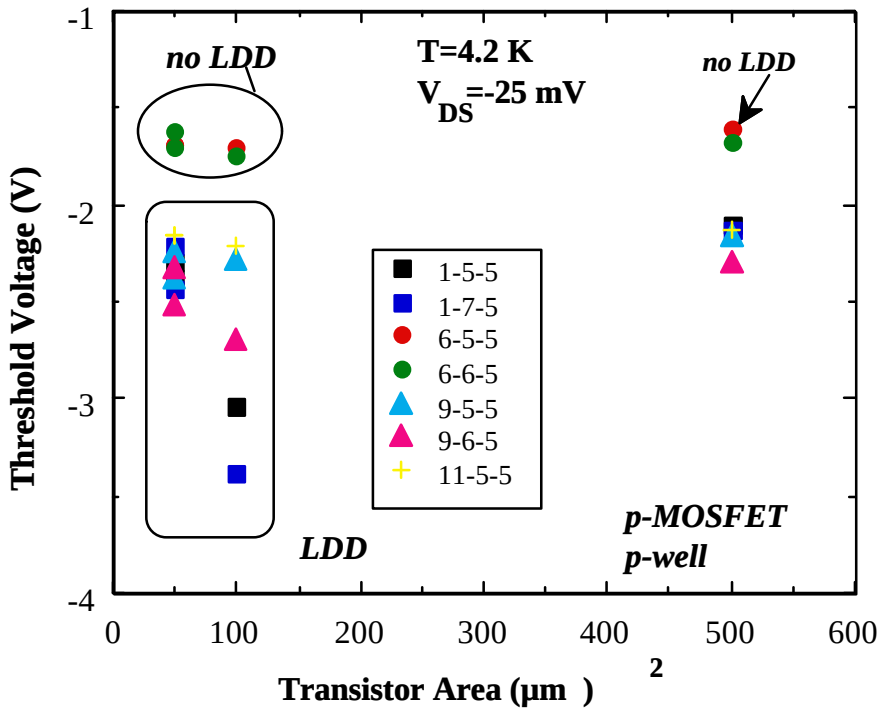


Fig. I.11b. Threshold voltage as a function of device area and processing split for the p-MOSFETs (p-well).

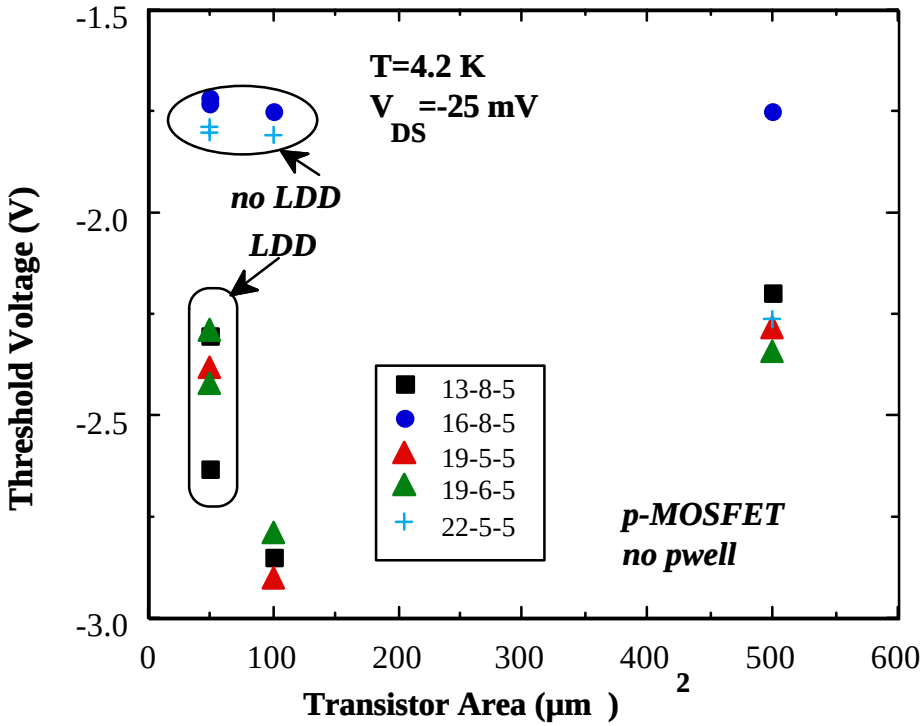


Fig. I.11c. Threshold voltage as a function of device area and processing split for the p-MOSFETs (no p-well).

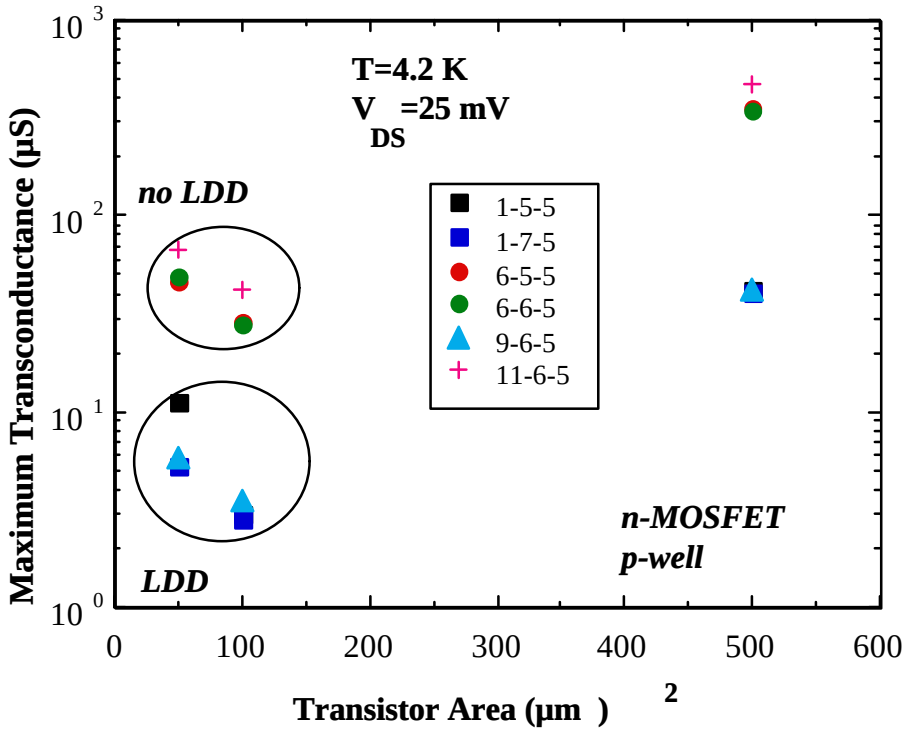


Fig. I.12a. Transconductance as a function of device area and processing split for the n-MOSFETs processed in a p-well.

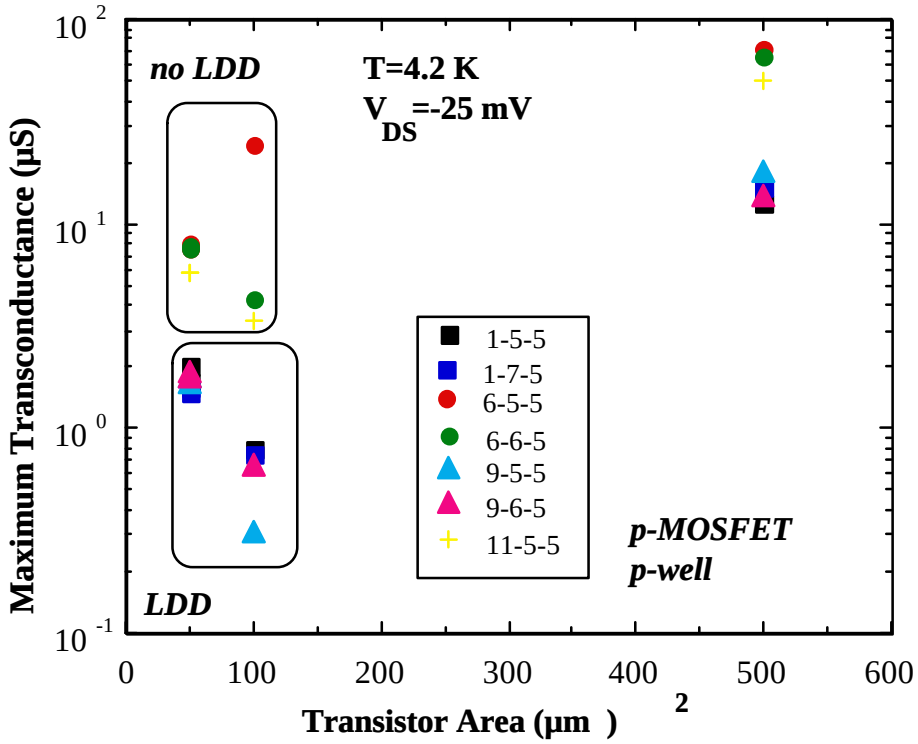


Fig. I.12b. Transconductance as a function of device area and processing split for the p-MOSFETs (p-well).

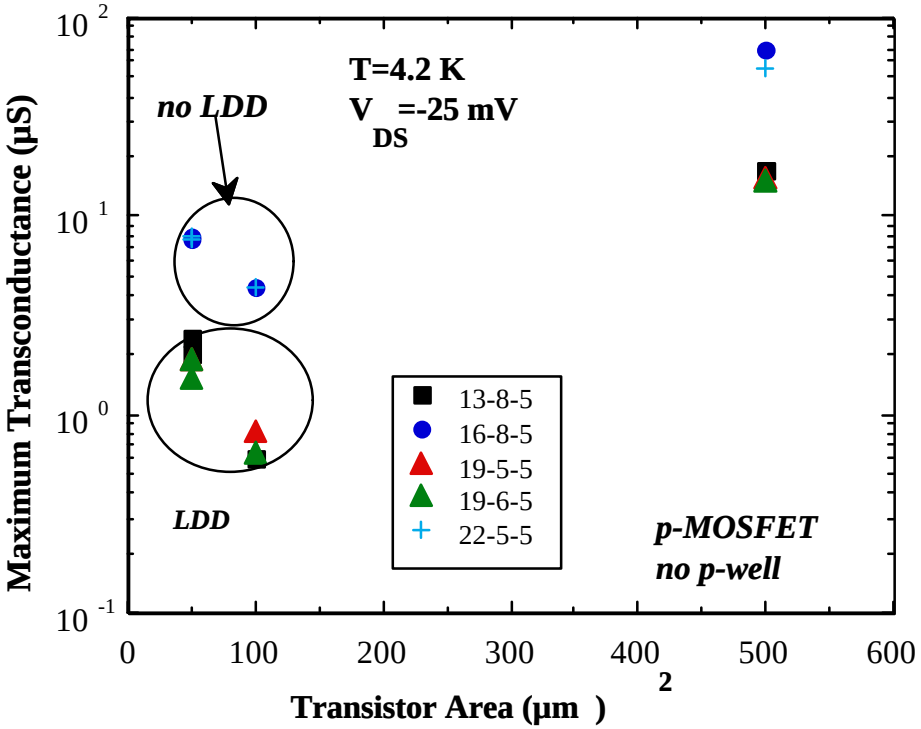


Fig. I.12c. Transconductance as a function of device area and processing split for the p-MOSFETs (no p-well).

Note finally that whether there is a p-well or not has no impact on the parameters of the p-MOSFETs, which indeed follows from the data shown in Figs I.11a and I.11b and in Figs I.12a and I.12b (or Table I.3).

I.4. Reproducibility

One particular concern for cryogenic testing and parameter extraction is the occurrence of transient and hysteresis phenomena [1,12]. This can give rise to problems for the accurate determination of the threshold voltage for example [1]. Therefore, it is essential to check the reproducibility of the measurements on the same device. In most cases, only marginal shifts of the input and output curves have been noted on most of the devices studied. The biggest differences occurred in the subthreshold regime. In some cases, marked transients or shifts were observed, pointing for example to a bad (or floating) substrate contact. Such measurement results were generally omitted in the analysis or at least considered with great care.

A final point which could give a problem is the fact that the sample-to-sample and array-to-array spread of the device characteristics becomes also more pronounced at 4.2 K. An example of the array to array differences is shown for the input curves of two 10 x5 µm p-MOSFETs in Fig. I.13 and I.14. A clear difference in the transconductance is found in this case. The differences within one array are generally less pronounced. This indicates that one should compare as much as possible the pre- and the post-irradiation characteristics of the same device and not rely too much on the expected similarity with other devices from different arrays.

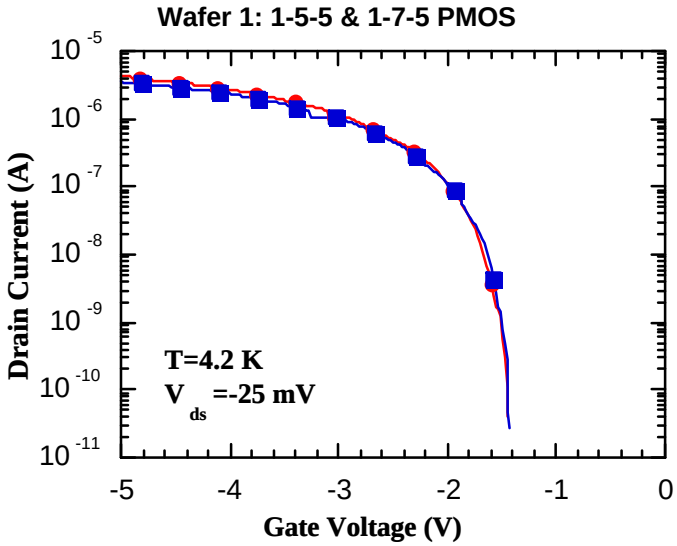


Fig. I.13. Input curves of two 10x5 µm p-MOSFETs at 4.2 K and -25 mV, corresponding to different arrays.

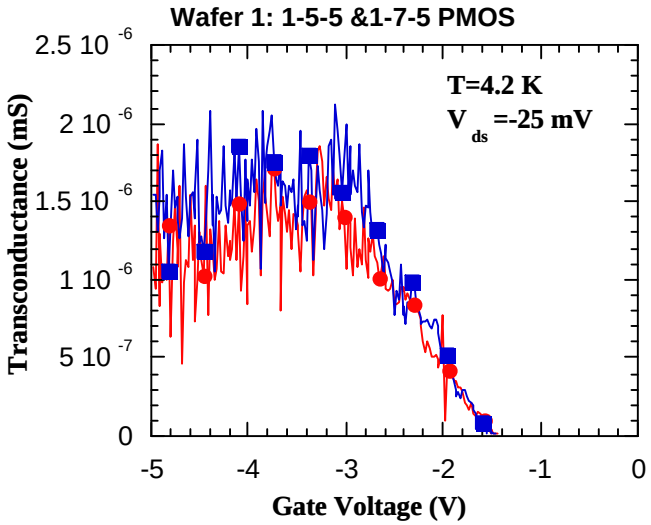


Fig. I.14. Transconductance of two 10x5 µm p-MOSFETs at 4.2 K and -25 mV, corresponding to different arrays.

I.5. Conclusions

From the pre-irradiation MOSFET characterization at 4.2 K can be concluded that at a device level, process split 6 is outperforming the other device types. It is also closest to the standard 0.7 µm AµE processing, so it requires only a small process modification. The presence of an LDD tends to degrade the static parameters but has in some cases a positive impact on the reduction of the kink, especially if no p-well is fabricated. It is therefore decided to focus the irradiation studies on splits 1, 6, 9, 11 and 13.

II. POST-IRRADIATION DEVICE/CIRCUIT CHARACTERIZATION-

During the irradiation round, both proton and γ-irradiations were performed on test structures of the selected splits, discussed more in detail in section I. The irradiations and the post-irradiation characterization at 4.2 K took place in the period May-June 1998, as indicated in Tables II.1 and II.5. At the same time, FIRGA circuits from the same splits were irradiated up to $3x10^{10}$ cm^{-2} 60 MeV protons and up to 50 krad γ's. Irradiations, performed at room temperature and under DC bias, were done by using the irradiation facilities at Louvain-la-Neuve. The activity related to cryogenic irradiations is addressed in section III.

The electrical testing of the devices and circuits at 4.2 K was performed shortly after the exposures and under the same experimental conditions as used for the pre-irradiation characterization. This minimizes possible post-irradiation room temperature annealing effects. In the case of γ-irradiation also room temperature testing has been performed. It has to be remarked that room temperature testing is only meaningful for the test structures and not for the circuits, as the latter are only functioning properly at cryogenic temperatures, i.e. the operating range for which they are designed. The only experimental change was that the drain bias during the input I_D-V_{GS} measurements was reduced from -25 mV down to -100 mV for the p-MOSFETs, for the post γ-irradiation measurements. This change in bias voltage was needed to reduce the spread in the results, which is much more pronounced after than before irradiation.

It should finally be remarked that the irradiated test structures were kept at room temperature after the irradiation and in-between the testing rounds.

Table II.1. 60 MeV proton irradiation matrix. A bias of +5 V (n-MOSFET) and 0 V (p-MOSFET) was applied during the room temperature irradiations, which took place on May 18, 1998. The used fluence was approximately $5x10^8$ p/cm^2s.

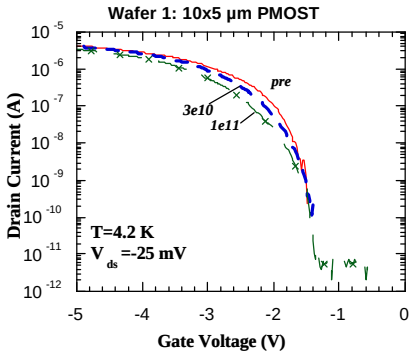
H^+ fluence (cm^{-2})	**Sample**
$3x10^{10}$	1-9-5 11-5-5 6-5-5 15-5-6 9-6-5 16-8-5
$1x10^{11}$	1-5-5 11-6-5 6-6-5 13-8-5 9-5-5 16-6-5

II.1. Proton Irradiation Effects.

A short overview of the cryogenic testing performed after the proton irradiation is given in Table II.2. A general remark is that there apparently were some measurement problems on the n-channel devices, while this was generally not the case for the p-channels. Although not confirmed, this may be related to contact problems. This became clear after a second measurement of some of the test structures in order to look for possible room temperature annealing effects. As can be read from Table II.2, acceptable results were obtained for some of the n-MOSFETs in the second measurements. Some of the proton irradiated test chips could not be measured at all, as indicated in Table II.2, explaining some of the 'missing' data in the following.

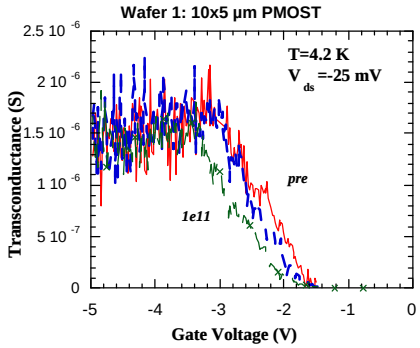
II.1.1. Impact on the linear characteristics.

A clear contrast was observed between the proton radiation response at 4.2 K of p-MOSFETs from wafer 1 and wafer 6. In the first case, a systematic reduction of the drain current (Fig. II.1.a) and of the transconductance (Fig. II.1.b) was found. For wafer 6, on the other hand, a slight increase was observed after a fluence of $3x10^{10}$ 60 MeV protons, while the device rebounds to the original current after the 10^{11} cm^{-2} irradiation.



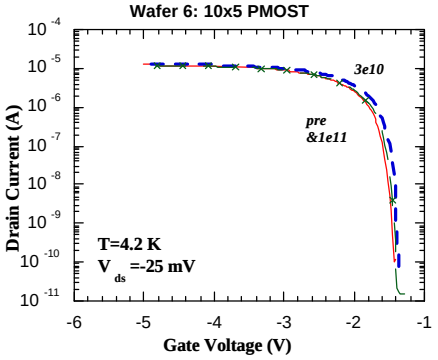
(a)

Fig. II.1.a. Input characteristics of a split 1 10 µmx5 µm proton irradiated p-MOSFET at 4.2 K, before and after 2 60 MeV proton fluences.



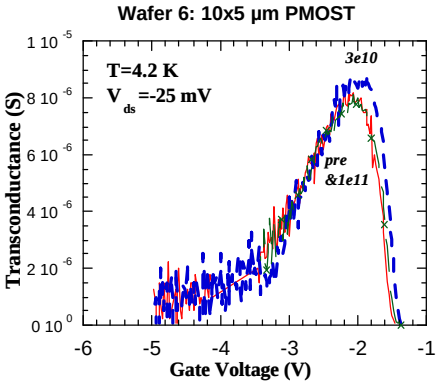
(b)

Fig. II.1.b. Linear transconductance for the same device as in Fig. II.1.a.



(a)

Fig. II.2.a. Input characteristics of a split 6 10 µmx5 µm proton irradiated p-MOSFET at 4.2 K, before and after 2 60 MeV proton fluences.



(b)

Fig. II.2.b. Linear transconductance for the same device as on Fig. II.2.a .

Since according to Table I.1 the only difference is the presence of the LDD, comparison of Figs II.1 and II.2 suggests that the different radiation response is related to the LDD/spacer regions. This is further confirmed by the results of Fig. II.3 (split 9 - LDD) and II.4 (split 11 - no LDD), showing the same trend.

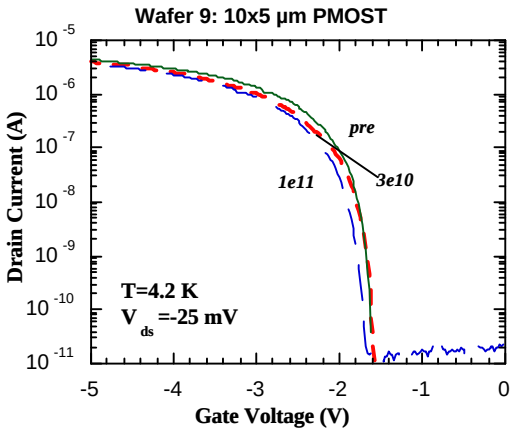


Fig. II.3. Input characteristics of a 10 µmx 5 µm p-MOSFET of split 9, after a $3x10^{10}$ cm^{-2} 60 MeV proton irradiation.

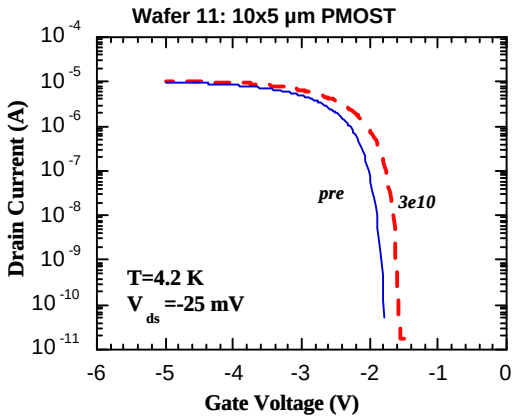


Fig. II.4. Input characteristics of a 10 µmx 5 µm p-MOSFET of split 11, after a $3x10^{10}$ cm^{-2} 60 MeV proton irradiation.

The behavior of the LDD p-MOSFETs can be reasonably well and qualitatively understood if one considers the creation of positive charge in the spacer oxide. This causes a reduction of the near surface hole density in the LDDs and hence an increase of the series resistance after irradiation. Similar results have been obtained before at 4.2 K [6-7]. The improvement for the non-LDD devices suggests the creation of negative charges in the gate oxide, or the creation of positive charges in the substrate or at the interface induced by the resulting displacement damage. The former mechanism seems rather unlikely, as the created electrons remain mobile in the oxide down to LHT, so that mainly hole trapping prevails. Even if the trapped charge is converted to interface traps due to room temperature annealing (not occurring at 4.2 K !!), it is expected that the corresponding charge is also positive. The reason is the donor like nature of the interface traps close to the valence band edge, which is of interest for p-MOSFETs. This introduces a positive charge contribution. Additional positive charge could come from the formation of radiation induced displacement damage, with a (deep) donor character (such as e.g. A-centers). Deactivation of the shallow donors in the n-well would lead, on the other hand, to the opposite effect. Measurements of the body factor and of the MOSFET capacitance at cryogenic temperatures could yield further information on this matter.

One should also take into consideration the degradation of the field oxide. For the applied technology a polysilicon buffered LOCOS (PBL) isolation scheme is used. This could lead to edge leakage in a parallel parasitic MOS along the bird's beak, evidenced by a subthreshold kink or step [11]. However, given the positive sign of the oxide trapped charge, this is not likely to occur in p-channel devices. For the irradiated n-MOSFETs such a behavior was occasionally found (see part II.2). A further clue for field-oxide effects can be derived by comparing edgeless (circular or closed-geometry) with rectangular devices. Input curves for splits 1,6,9 and 11 p-MOSFETs are represented in Figs II.5 to II.8. Comparing with the curves of the 10x5 µm devices of Figs. II.1 to II.4, the following is concluded. Except maybe for wafer 6, the same

qualitative shifts are observed for both transistor geometries. This indicates that the proton irradiation induced changes are intrinsic, i.e. related to the channel region (gate oxide/interface/substrate). The result of the #6 p-MOSFET of Fig. II.6 suggest that the rebound behavior noticed in Fig. II.2.a. may be related to the edge region in this case. This is, however, not confirmed by the other non-LDD p-MOSFETs of wafer 11. This issue needs to be confirmed in a second experiment.

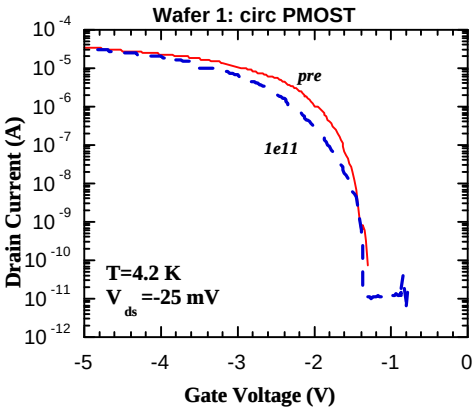


Fig. II.5. Input characteristics of a circular p-MOST of split 1, after a $1x10^{11}$ cm^{-2} 60 MeV proton irradiation.

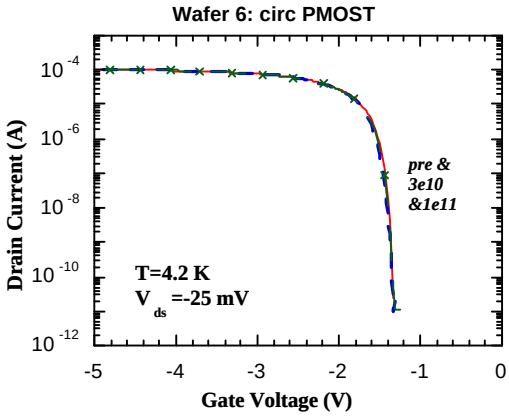


Fig. II.6. Input characteristics of a circular p-MOST of split 6, after a 3x and $10x10^{10}$ cm^{-2} 60 MeV proton irradiation.

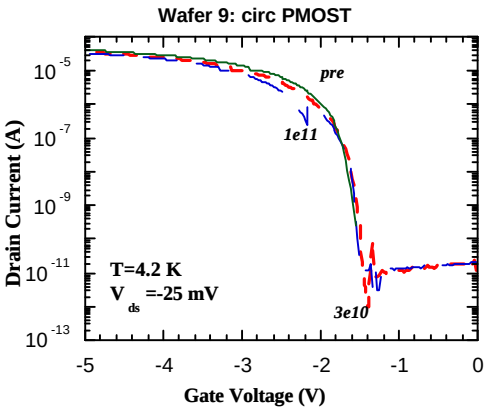


Fig. II.7. Input characteristics of a circular p-MOST of split 9, after a $3x10^{10}$ cm^{-2} 60 MeV proton irradiation.

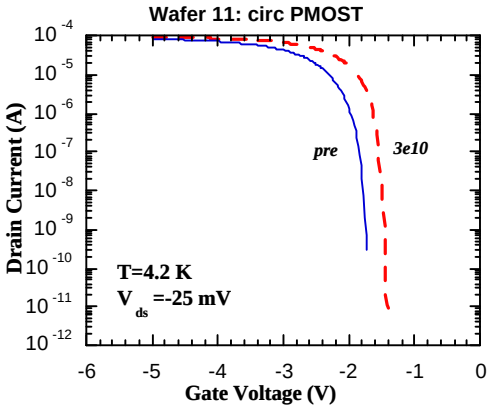
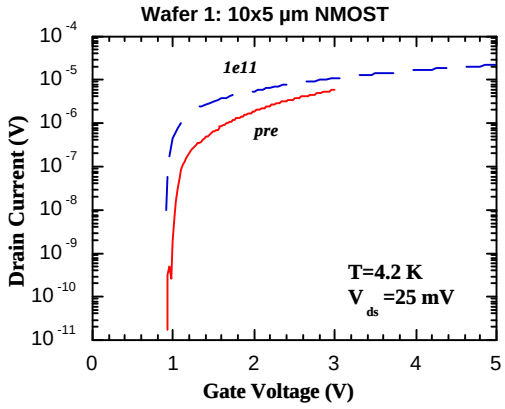


Fig. II.8. Input characteristics of a circular p-MOST of split 11, after a $3x10^{10}$ cm^{-2} 60 MeV proton irradiation.

As mentioned before, only a limited post-irradiation characterization of the n-MOSFETs could be performed. Furthermore, the useful measurements took place about one and a half week after the irradiation, so that significant room temperature annealing could take place. However, as will be demonstrated, little difference has been found for the initial and the following post-irradiation measurements for the p-MOSFETs.

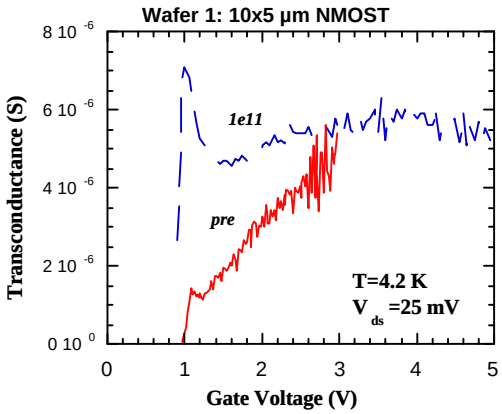
As can be seen from Figs II.9 and II.10, the same type of degradation is observed for the 10 µmx5 µm n-MOSFETs of splits 1 and 6, namely: a significant increase of the maximum transconductance, whereby a kind of peak-shaped behavior is now found for the LDD devices as well. In fact, looking at Fig. II.9, one can discern already before irradiation a small peak at the same position, which becomes more pronounced after the irradiation. At the same time, the threshold voltage reduces after the exposure, in line with the expected positive charging of the gate oxide.

. For the LDD devices, the positive charging of the spacer oxide will lead to an accumulation of the n^+ region and hence to a reduction of the series resistance [11]. Note finally that the observation of Fig. II.9.b is not believed to be a measurement artifact: also the n-MOSFETs of split 9 (LDD) show the same behavior after 60 MeV proton irradiation. Confirmation is expected from an additional irradiation round.



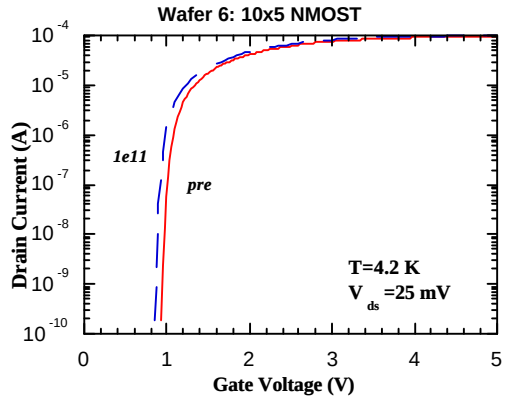
(a)

Fig. II.9.a. Input characteristics of a 10 µmx5 µm n-MOSFET of split 1, after a 10^{11} cm^{-2} 60 MeV proton irradiation.



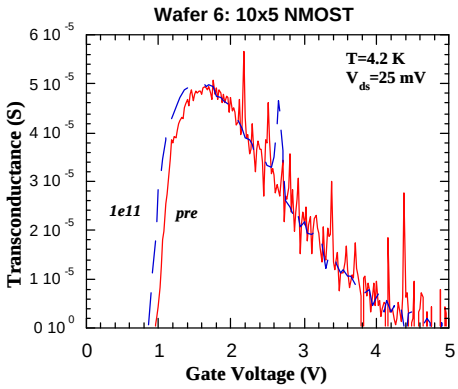
(b)

Fig. II.9.b. Transconductance of a 10 µmx5 µm n-MOSFET of split 1, after a 10^{11} cm^{-2} 60 MeV proton irradiation.



(a)

Fig. II.10.a. Input characteristics of a 10 µmx5 µm n-MOSFET of split 6, after a 10^{11} cm^{-2} 60 MeV proton irradiation.



(b)

Fig. II.10.b. Transconductance of a 10 µmx5 µm n-MOSFET of split 6, after a 10^{11} cm^{-2} 60 MeV proton irradiation.

II.1.2. Saturation.

The proton irradiations on wafer 1 p-MOSFETs provoke little changes in the output I_D-V_{DS} characteristics as is shown in Fig. II.11. There is maybe a slight tendency for reduction of the drain current. Noticeable changes are found for wafer 6 p-MOSFETs in the linear regime, showing an increase of the drive current (Fig. II.12). The same applies for the 'kink' region. The wafer 9 p-MOSFETs show a clearer tendency for reduction of the drain current with fluence (Fig. II.13), which is equally observed for the split 11 p-MOSFETs. This indicates that the standard and the wafer 6 split show a favorable degradation behaviour at 4.2 K after proton irradiation.

The proton irradiated n-MOSFETs show a slight (split 1; Fig. II.15) to a marginal increase (split 6; Fig II.16) of the drain current in saturation, for the largest proton fluence studied.

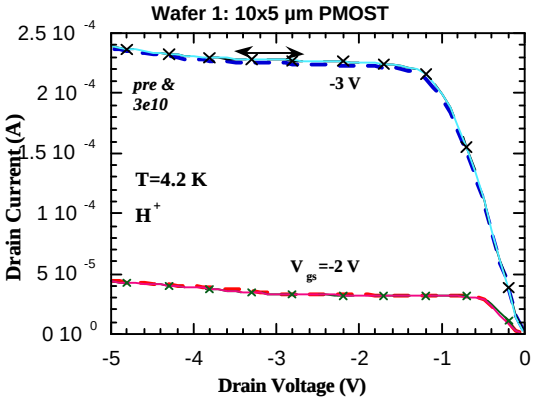


Fig. II.11. Output characteristics of a 10 µmx5 µm p-MOSFET of split 1, after a 3x and a $10x10^{10}$ cm^{-2} 60 MeV proton irradiation. Full lines are pre-rad. The dashed lines correspond to post rad 3e10, low-high and high-low sweep (crosses).

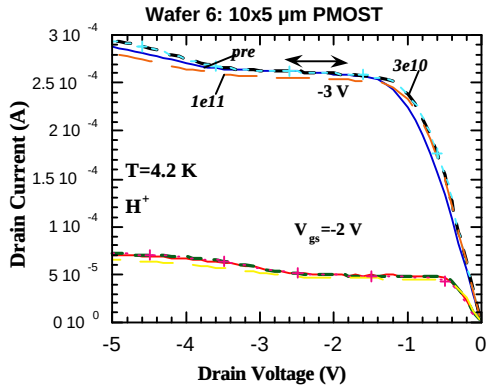


Fig. II.12. Output characteristics of a 10 µmx5 µm p-MOSFET of split 6, after a 3x and a $1x10^{11}$ cm^{-2} 60 MeV proton irradiation.

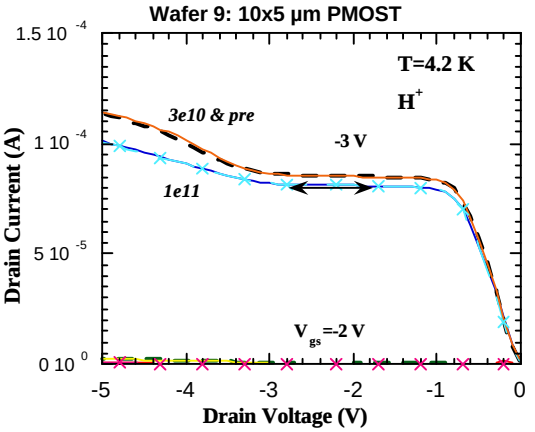


Fig. II.13. Output characteristics of a 10 µmx5 µm p-MOSFET of split 9, after a 3x and a $10x10^{10}$ cm^{-2} 60 MeV proton irradiation.

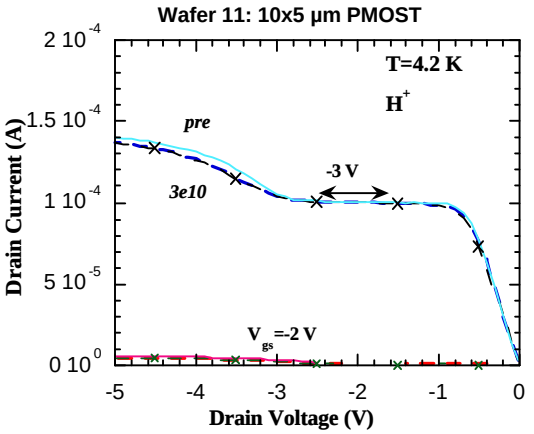


Fig. II.14. Input characteristics of a 10 µmx5 µm p-MOSFET of split 11, after a $3x10^{10}$ cm^{-2} 60 MeV proton irradiation.

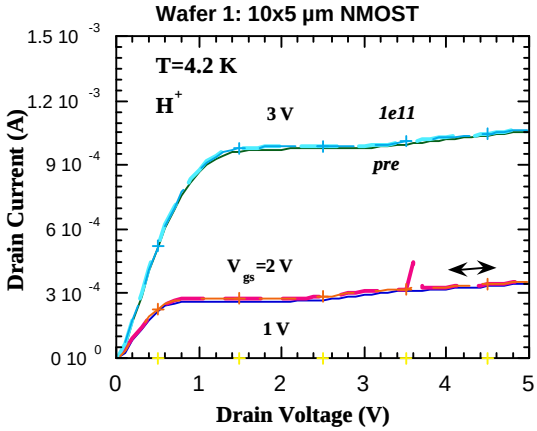


Fig. II.15. Output characteristics of a 10 µmx5 µm n-MOSFET of split 1, after a $1x10^{11}$ cm^{-2} 60 MeV proton irradiation.

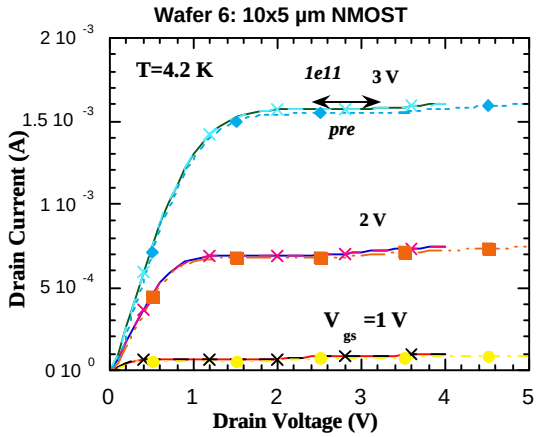


Fig. II.16. Input characteristics of a 10 µmx5 µm n-MOSFET of split 6, after a $1x10^{11}$ cm^{-2} 60 MeV proton irradiation.

Table II.2. Measurement diary of the proton irradiated samples.

Date	Sample	Remarks
19/05/98	1-9-5	n-MOSFETs give "strange" results (too high V_T)
	6-5-5	idem
	11-5-5	idem
	1-5-5	idem
	6-5-5	idem
26/05/98	13-5-6	n-MOSFET ?
	16-8-5	no substrate contact (zero I_B) n-MOSFETs
	9-5-5	ok
	13-8-5	n-MOSFETs?
28/05/98	16-6-5	gate leakage
	1-9-5	RT anneal effect ? problem I_G p-MOSFET n-MOSFET?
	6-5-5	n-MOSFET no stable characteristics
	1-5-5	n-MOSFET ok problem p-MOSFET
	6-6-5	n-MOSFET ok p-MOSFET ?

II.1.3. Device parameters after proton irradiation

The measured V_Ts and maximum transconductances are summarized in Figs II.17 and II.18, for the 60 MeV proton irradiated p-MOSFETs.

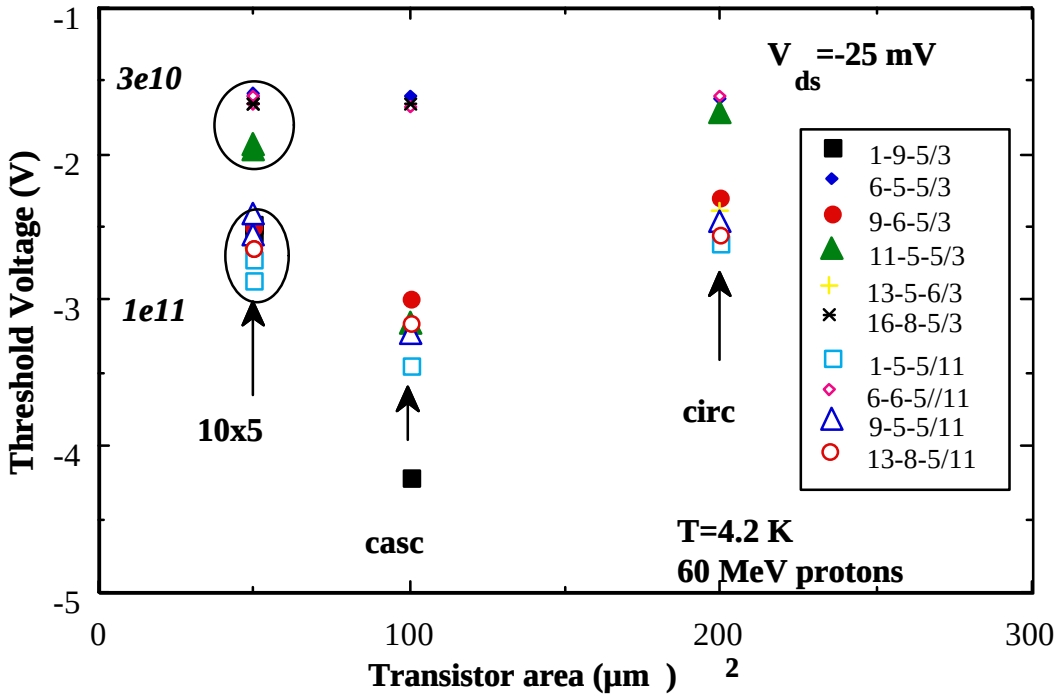


Fig. II.17. Threshold voltage at -25 mV and 4.2 K of the proton irradiated p-MOSFETs.

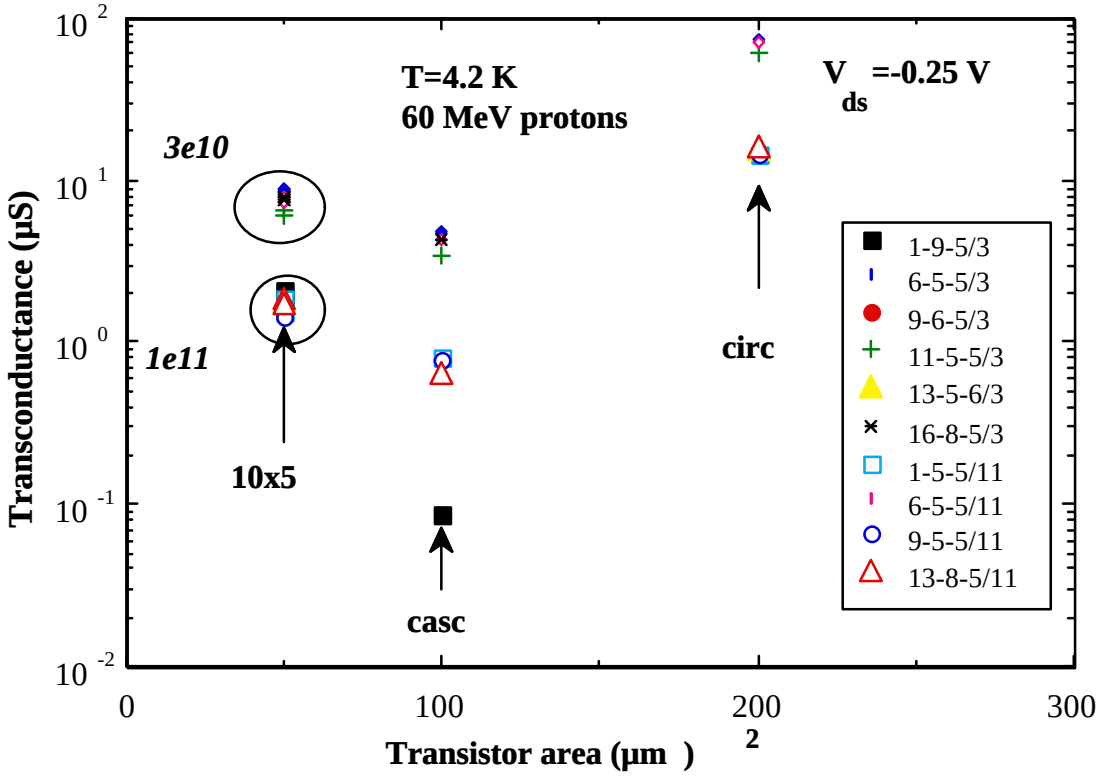


Fig. II.18. Transconductance at -25 mV and 4.2 K of the proton irradiated p-MOSFETs.

As a rule, the threshold voltage shifts to more negative values for increasing fluence, while the maximum transconductance reduces with Φ. Detailed measurement data are represented in Tables II.3 (n-) and II.4 (p-MOSFETs). As can be seen, the induced changes for the split 1 devices is much more pronounced than for the non-LDD devices (Tables II.3 and II.4). This is related to the drastic change in shape of the characteristic to be noted in Figs II.9 and II.10. It should also be remarked here that for the LDD devices a V_{DS}=±25 mV is probably too small to accurately determine the device parameters, using the classical extrapolation method. Measurements at much higher V_{DS} (±1 V) generally reveal a lower threshold and a 'normal' transconductance peak. Similar observations hold for the p-MOSFETs in Table II.4.

Note in Table II.4 for the non-LDD p-MOSFET of wafer 6, the ‘rebound’ behavior in the threshold voltage, showing first an increase, followed by a reduction for larger fluences. In general, the device degradation is in the range of a few % up to 10 % typically. Furthermore, there is no clear scaling with the proton fluence, indicating the complex nature of the induced damage. Another observation is that in some cases, the circular transistors show the opposite shift in V_T compared with the 10 µmx5 µm devices (see for example the #6 p-MOSFETs in Table II.4).

A final remark is that the data in Tables II.3 and II.4 have been derived from the pre- and post-irradiation measurements of the *same* transistors. However, the pre-irradiation results in the figures II.1-II.18 correspond to one pre-irradiation result only. As shown in the first part, there are some sample-to-sample and array-to-array differences already before irradiation, which have been taken as much as possible into account. A further source of measurement instabilities and data spread is the occurrence of freeze-out transient effects at LHT [11], which will be discussed further.

Table II.3. Changes in the threshold voltage and in the maximum transconductance of n-MOSFETs at 4.2 K, induced by a 10^{11} cm^{-2} 60 MeV proton irradiation. The parameters have been extracted in linear operation for a V_{DS}=25 mV.

Device	ΔV_T (V)	%	Δg_{mmax} (µS)	%
N1-5-5 10x5	-0.82	41.2	4.15	36.6
N1-5-5 circ	-0.71	44.4	57.9	140
N6-6-5 10x5	-0.1	8.7	1.3	2.7
N6-6-5 circ	0.07	6.7	24	6.9

Table II.4. Changes in the threshold voltage and in the maximum transconductance of p-MOSFETs at 4.2 K, induced by a 60 MeV proton irradiation. The parameters have been extracted in linear operation for a V_{DS}=25 mV. For the different devices, the used irradiation fluence is indicated between brackets.

Device	ΔV_T (V)	%	Δg_{mmax} (μS)	%
P1-9-5 10x5 ($3x10^{10}$ cm^{-2})	-0.22	9.6	0.39	22.9
P1-9-5 circ ($3x10^{10}$ cm^{-2})				
P1-5-5 10x5 ($1x10^{11}$ cm^{-2})	-0.58	25.3	0.17	10
P1-5-5 circ ($1x10^{11}$ cm^{-2})	-0.61	30.5	2.0	16
P6-5-5 10x5 ($3x10^{10}$ cm^{-2})	+0.11	6.5	0.59	7.3
P6-5-5 circ ($3x10^{10}$ cm^{-2})	-0.03	1.9	2.2	3.1
P6-6-5 10x5 ($1x10^{11}$ cm^{-2})	-0.04	2.5	0.4	5.3
P6-6-5 circ ($1x10^{11}$ cm^{-2})	+0.06	3.6	4.5	6.8
P9-6-5 10x5 ($3x10^{10}$ cm^{-2})	+0.03	1.2	-0.23	12.1
P9-6-5 circ ($3x10^{10}$ cm^{-2})	0.00	0.0	0.9	6.5
P9-5-5 10x5 ($1x10^{11}$ cm^{-2})	-0.32	14.3	-0.05	3
P9-5-5 circ ($1x10^{11}$ cm^{-2})	-0.32	14.9	1.4	10.5
P11-5-5 10x5 ($3x10^{10}$ cm^{-2})	+0.23	10.6	0.74	12.6
P11-5-5 circ ($3x10^{10}$ cm^{-2})	+0.41	19.2	9.9	19.7

II.1.4. RT annealing effect.

One of the drawbacks of the room temperature irradiation is the occurrence of damage annealing or conversion. In order to have some idea, a number of samples have been measured a second time (Table II.2). According to the results of Figs II.19 till II.21 little additional changes occurred in-between the first and the second measurements. It is concluded from this that the main annealing will take place the first few hours after the irradiation. It also shows the reproducibility of the measurements. It is well-known from the past that LHT characteristics may suffer from transient effects [11,12]. These are apparently less important for most of the devices measured. This was also verified by repeating the same measurement a second time immediately after the first measurement (same cooling round). In most cases, negligible changes were observed. This indicates that the differences reported above are (most likely) induced by the proton irradiation.

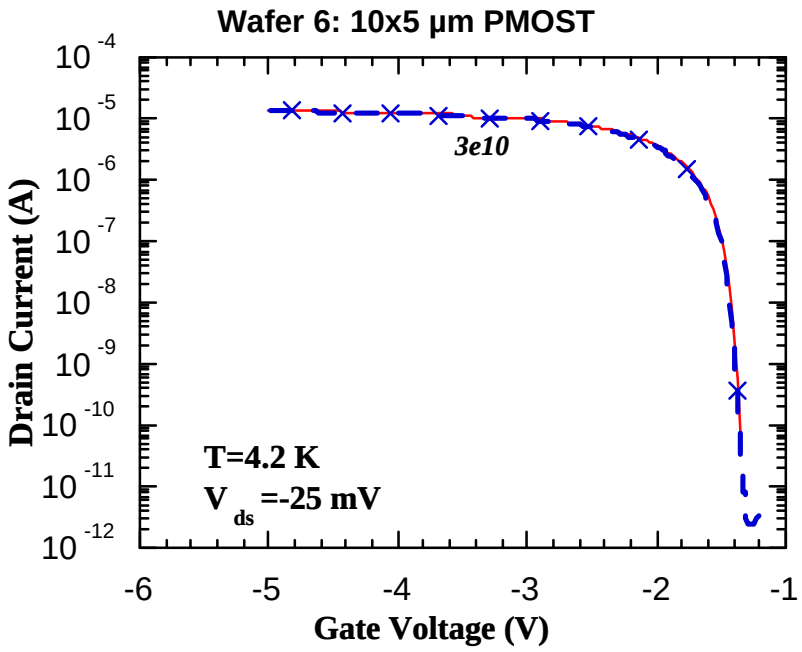


Fig. II.19. Input characteristics of a 10 µmx5 µm p-MOSFET after $3x10^{10}$ cm^{-2} 60 MeV protons. Two measurements have been performed with one and a half week in-between (see Table II.2).

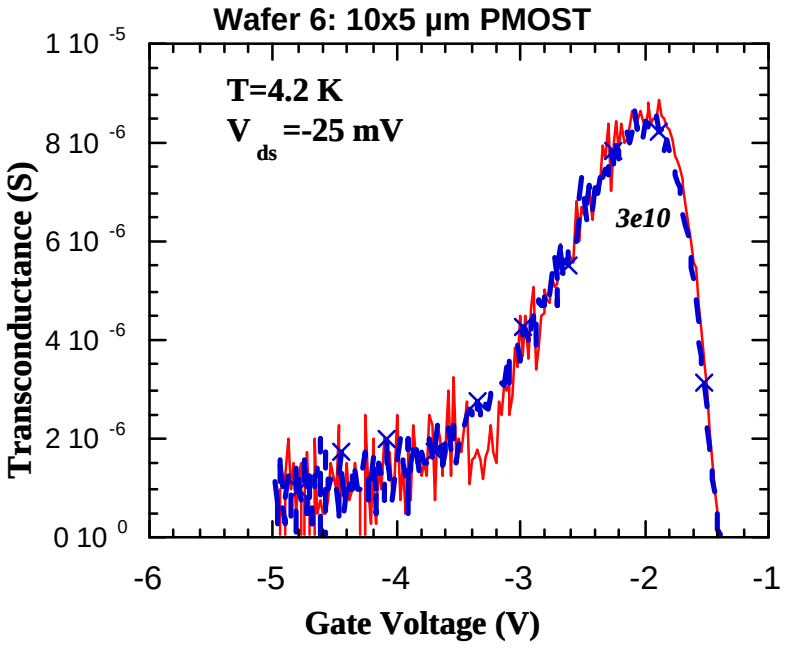


Fig. II.20. Transconductance of a 10 µmx5 µm p-MOSFET after $3x10^{10}$ cm^{-2} 60 MeV protons. Two measurements have been performed with one and a half week in-between (see Table II.2).

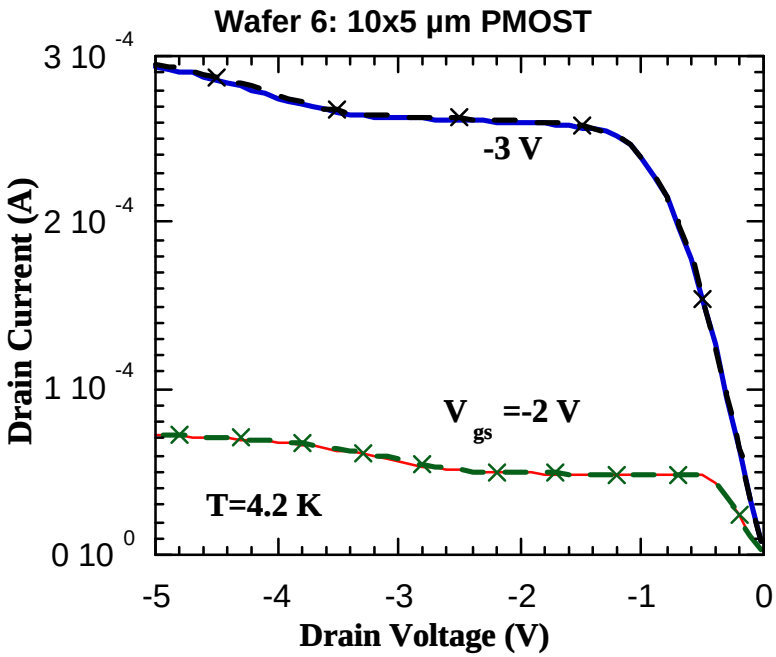


Fig. II.21. Output characteristics of a 10 µmx5 µm p-MOSFET after $3x10^{10}$ cm^{-2} 60 MeV protons. Two measurements have been performed with one and a half week in-between (see Table II.2).

II.1.5. Conclusions

In summary, it can be stated that the induced changes after room temperature proton irradiation are in the range of a few percent up to 10 % typically, for the fluence range studied. There is an impact of the technology, whereby the presence of an LDD has the strongest impact, particularly for the p-channel devices. Non-LDD p-MOSFETs can show a rebound behavior, i.e., at moderate fluences, the drain current increases, followed by a reduction for further exposure. As this effect has been seen on both wafers 6 and 11 and for a number of devices on each wafer, it is believed to be a real effect. The exact mechanisms underlying this phenomenon have to be further explored. LDD p-MOSFETs show the classical increase of the reduction of the threshold voltage and reduction of the drain current, which becomes more pronounced for higher fluences. The opposite is found for the n-channel devices.

In order to get more insight, further proton irradiations at higher fluences may be performed (10^{12} cm^{-2}) and compared with an 10^{11} cm^{-2} reference. This should confirm some of the observed trends and extend the damage range. Finally, LHT irradiations could be useful but are not feasible within the time and budget frame of the project. This is further discussed in section III. It should be recalled here that especially from a viewpoint of displacement damage, room temperature should be a worst case compared with proton exposures at 4.2 K [11].

II.2. Gamma Irradiation Effects

Table II.5 describes the experimental matrix for the γ-irradiations. The testing sequence is given in Tables II.6a and b.

Table II.5. Co γ-irradiation matrix. A bias of +5 V (n-MOSFET) and 0 V (p-MOSFET) was applied during the room temperature irradiations, which took place June 8 and 9, 1998. The dose rate was approximately 5 krad/hour, with the samples placed at a distance of 65 cm. The irradiations took, respectively, 9.5 and 19 h.

Co γ dose (cm^{-2})	**Sample**
50 krad(SiO_2)	1-7-7 11-8-6 6-5-6 13-6-6 9-5-6 16-5-6
100 krad(SiO_2)	1-8-7 11-9-6 6-6-6 13-9-6 9-6-6 16-7-6

II.2.1. Impact on the linear characteristics

The impact on the linear input characteristics of the 10x5 μm n-MOSFETs for the different splits is given in Figs II.22 to II.26. The split 13 could not be measured after irradiation, most likely because of handling reasons. The corresponding transconductance is represented in Figs. II. 27 to II. 31.

On the whole, in most cases, a reduction of the threshold voltage is observed and an increase of the maximum transconductance after γ-exposure. For the LDD splits 1 and 9, a pronounced change in the shape of the characteristic is observed (Figs II.22 and II.24), whereby the rather flat transconductance before is replaced by a peak-shaped curve (Figs II.27 and II.29). Interestingly, in Fig. II.22, a subthreshold kink is found for the LDD n-MOSFET, pointing towards conduction along the device edges. This feature is absent in the circular devices (Fig. II.32). On the other hand, the strong increase in g_{mmax} is also found for the circular LDD n-MOSFETs of Figs II.32 and II.34, indicating that it is an intrinsic change, related to the interface and channel region. For the LDD devices, the results strongly suggest a kind of saturation of the damage (Figs. II.22, II.24, II.32 and II.34). However, the maximum transconductance can show a further increase after the 100 krad exposure (Figs II.27 and II.36). Taking into account the positive charging of the oxide, one would expect on the one hand a reduction of the mobility, due to the increase of Coulombic scattering at 4.2 K. However, as noted before, the dominant degradation most likely takes place in the spacer oxides and related interface, which becomes more and more accumulated. Hence, scattering of electrons by charges in the oxide/interface will reduce, as will the series resistance.

The non-LDD n-MOSFETs show a less pronounced degradation after room temperature gamma's. While split 6 exhibits a more or less gradual change with total dose (Fig. II.23), marginal effects are seen for the wafer 11 n-MOSFETs (Figs II.25, II.30 and II.33). This is clearly the "hardest" split with respect to total-dose damage in the n-MOSFETs. Compared with wafer 9, it is striking that there is little change in the position of the curves (see e.g. Figs II.24, II.25, II.33 and II.34). The absence of the V_T adjust implant seems to have a positive effect on the radiation hardness with respect to total dose. To some extent the same is derived from the behavior of the transconductance in Figs II.28, II.30, II.31 and II.36 versus II.37 for the closed-geometry n-MOSFETs.

The impact of γ-irradiation on the p-channel devices is as usual opposite to the case for n-MOSFETs. This is summarized in Figs II.38 to II.43, for split 1 and 6. For the LDD case, the degradation increases with total dose and results in a reduction of the threshold voltage and a small reduction of the transconductance (Figs II.39 and II. 43). Overall, there is a large similarity with the case of the proton irradiations, discussed in section II.1. The same applies for the non-LDD split (Figs II.40-II.41), although there is no rebound behavior here. This could point to a specific degradation mechanism for low-dose protons in the p-channel devices. A possible intuitive interpretation could be that for low fluences, the displacement damage effects dominate, while for higher fluences, the oxide damage becomes more pronounced. It is estimated that the ionization damage equivalent to 60 MeV protons is roughly 5 ($3x10^{10}$ cm^{-2}) to 15 krad (10^{11} cm^{-2}). One should of course also take in mind the room temperature annealing effects, to be discussed later in more detail.

II.2.2. Saturation

The output characteristics in general show a slight increase of the drain current for lower V_{DS} after γ-irradiation (see Figs II.44 to II.48). In some cases, the increase is marginal (split 16; Fig. II.48). The most pronounced effect is for the LDD n-MOSFETs of Figs II.44 and II.46. Also indicated in most of the figures is a post-irradiation low-high (LH) and high-low (HL) curve. No clear hysteresis is found. However, in cases where there was a clear kink effect before irradiation, there is a strong reduction of the kink after (Figs II.47 and II.48). A similar observation was made for some types of hot-carrier degradation at 4.2 K [13-14]. The reduction of the kink effect points to a lower generated substrate current. This could be due to a lower maximum field near the junction or more likely, to a lower electron mean free path. The latter could be induced by the increased carrier scattering due to radiation induced charged centers. Analysis of the substrate current and of the multiplication factor will shine more light on the exact mechanism. That this kink reduction is not an artifact is further illustrated by Figs II.49 and II.50 for two circular n-MOSFETs of the same arrays as the 10x5 μm ones. The effect is thus observed for different technological splits and for more than one device per split.

The saturation current of the p-MOSFETs shows a marked reduction after γ-irradiation (Figs II.51 and II.52). The reduction is in fact more pronounced than after proton exposure (see Figs. II.11 and II.12). No particular hysteresis or kink effect is observed.

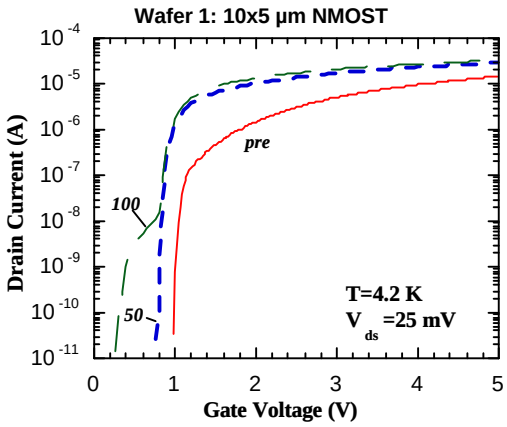


Fig. II.22. Input characteristics of a γ-irradiated #1 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

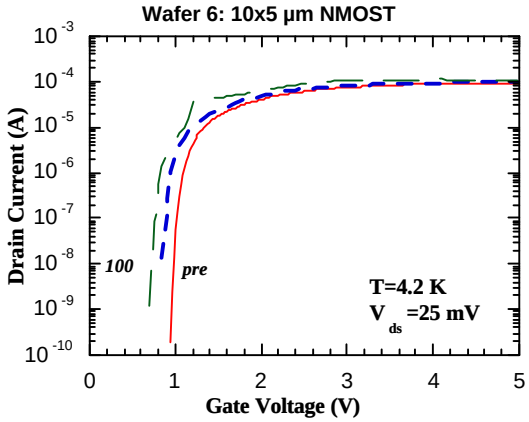


Fig. II.23. Input characteristics of a γ-irradiated #6 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

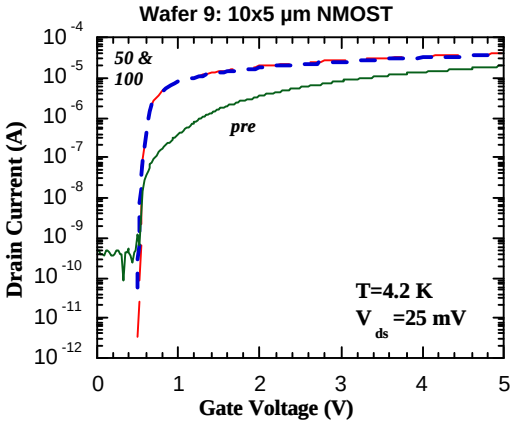


Fig. II.24. Input characteristics of a γ-irradiated #9 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

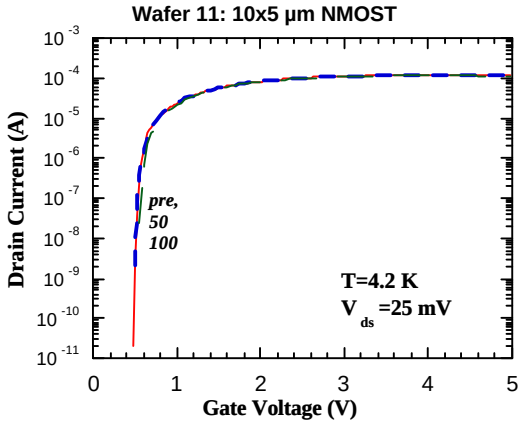


Fig. II.25. Input characteristics of a γ-irradiated #11 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

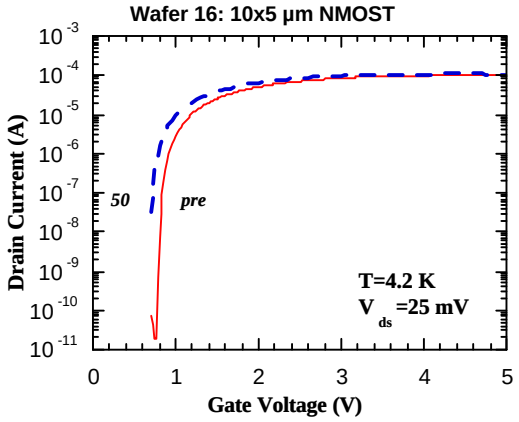


Fig. II.26. Input characteristics of a γ-irradiated #16 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 krad.

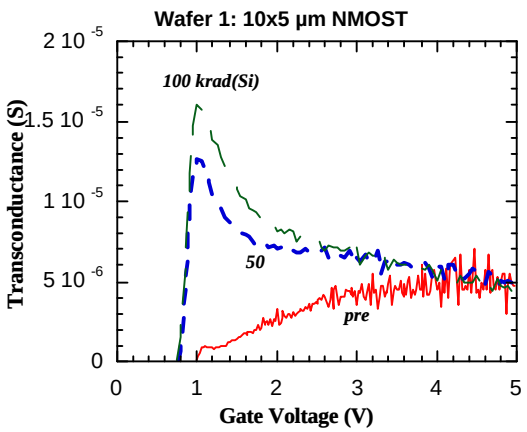


Fig. II.27. Transconductance of a γ-irradiated #1 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

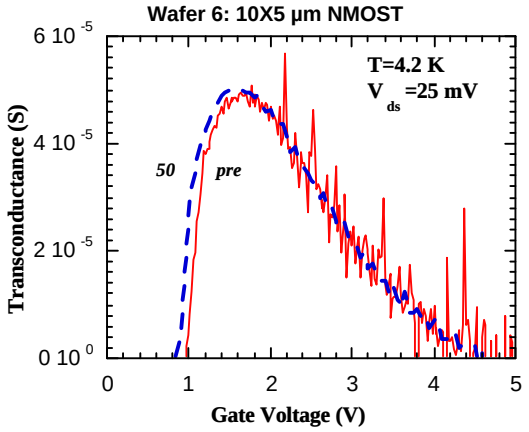


Fig. II.28. Transconductance of a γ-irradiated #6 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

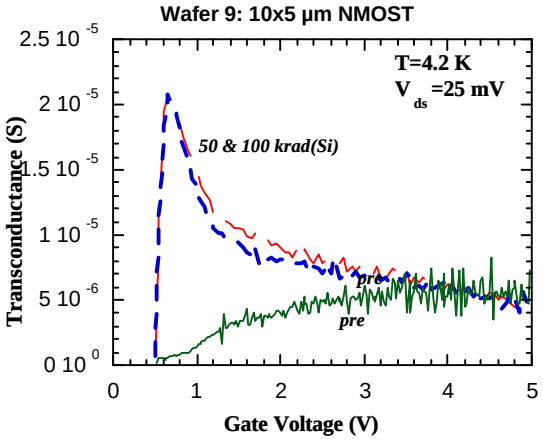


Fig. II.29. Transconductance of a γ-irradiated #9 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

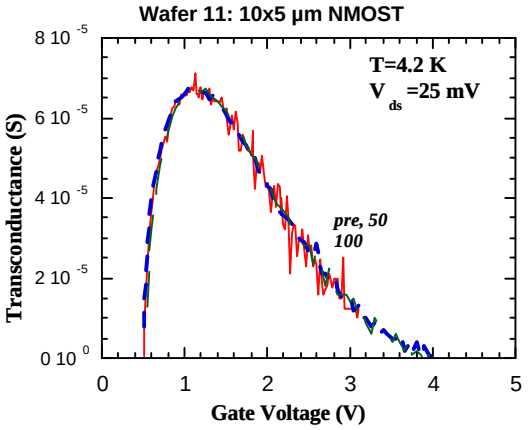


Fig. II.30. Transconductance of a γ-irradiated #11 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

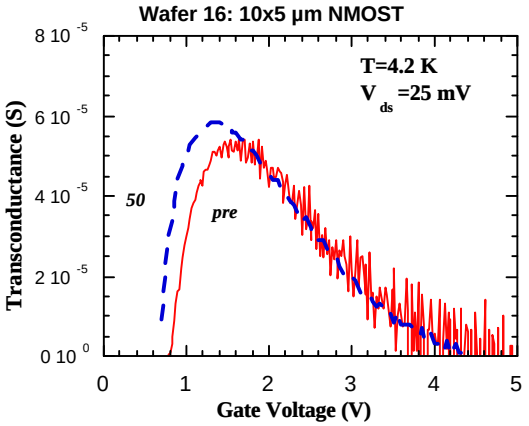


Fig. II.31. Transconductance of a γ-irradiated #16 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 krad.

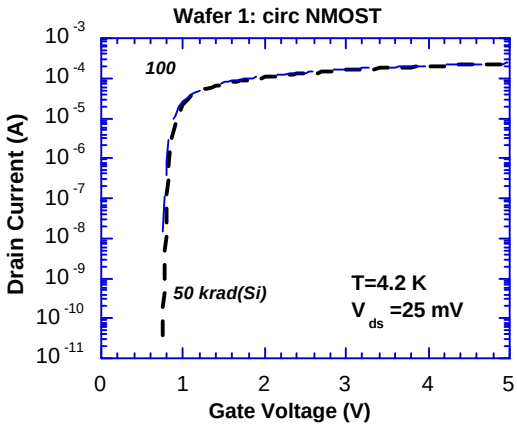


Fig. II.32. Input characteristics of a γ-irradiated #1 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

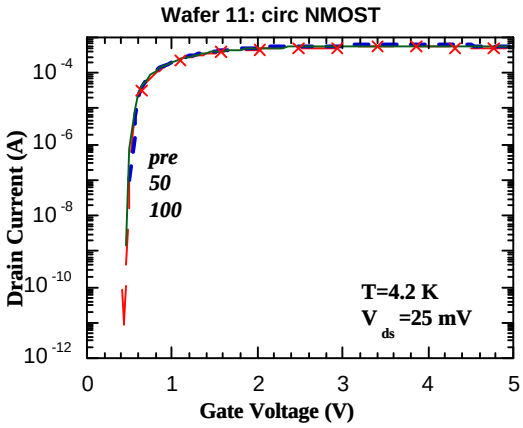


Fig. II.33. Input characteristics of a γ-irradiated #11 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

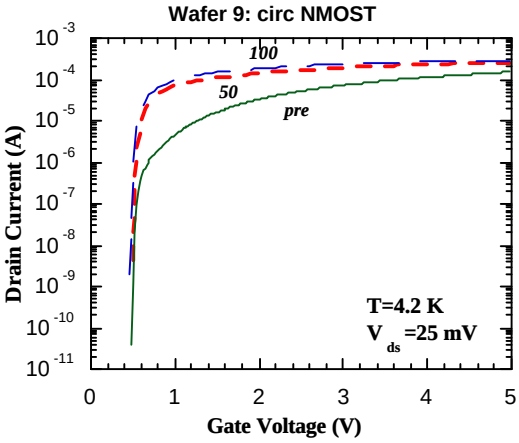


Fig. II.34. Input characteristics of a γ-irradiated #9 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

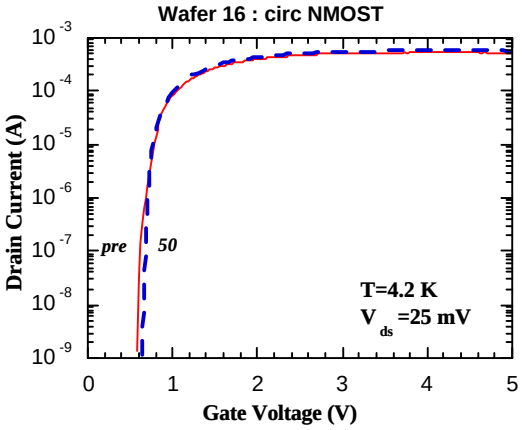


Fig. II.35. Input characteristics of a γ-irradiated #16 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

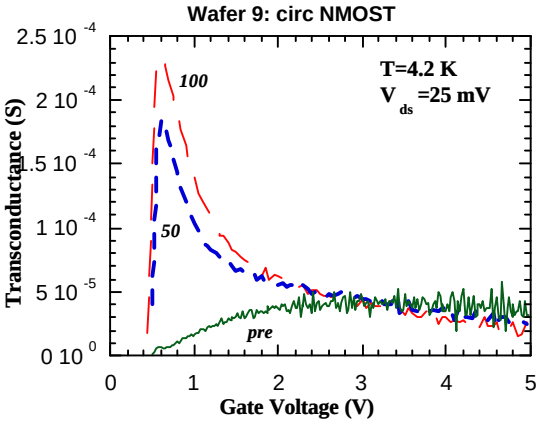


Fig. II.36. Transconductance of a γ-irradiated #9 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

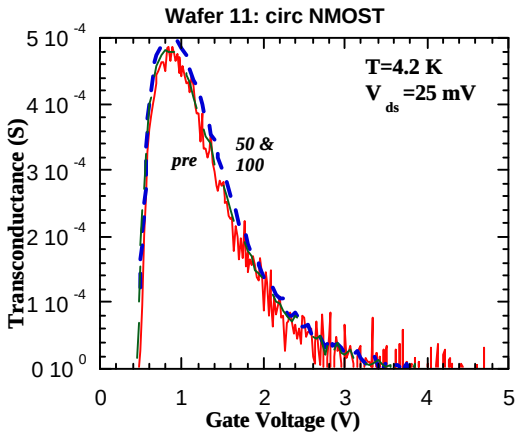


Fig. II.37. Transconductance of a γ-irradiated #11 n-MOSFET at 4.2 K and drain bias of 25 mV, corresponding to a dose of 50 and 100 krad.

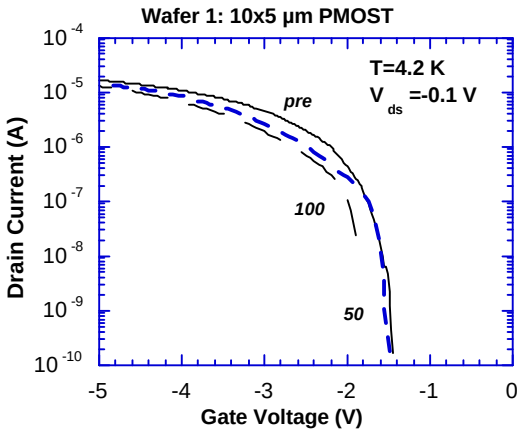


Fig. II.38. Input characteristics of a γ-irradiated #1 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

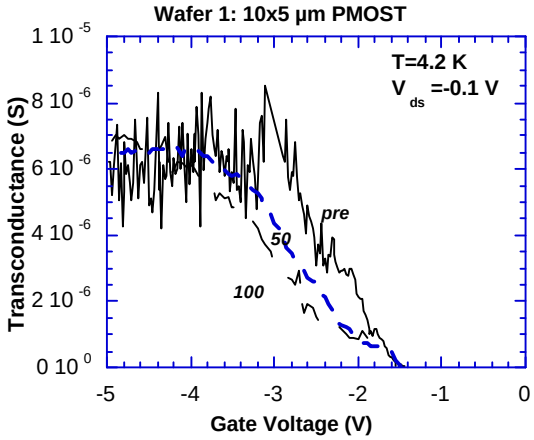


Fig. II.39. Transconductance of a γ-irradiated #1 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

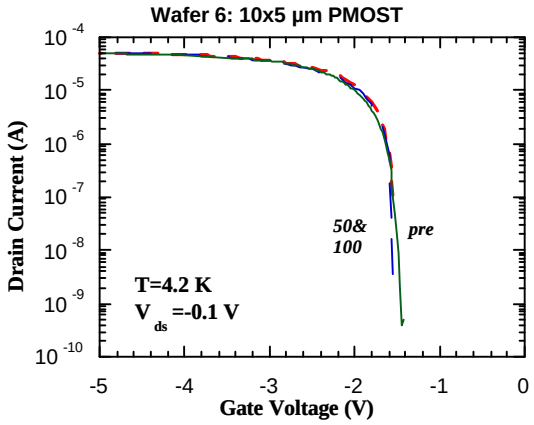


Fig. II.40. Input characteristics of a γ-irradiated #6 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

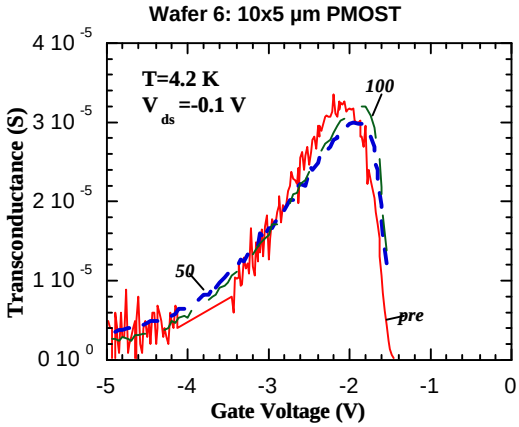


Fig. II.41. Transconductance of a γ-irradiated #6 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

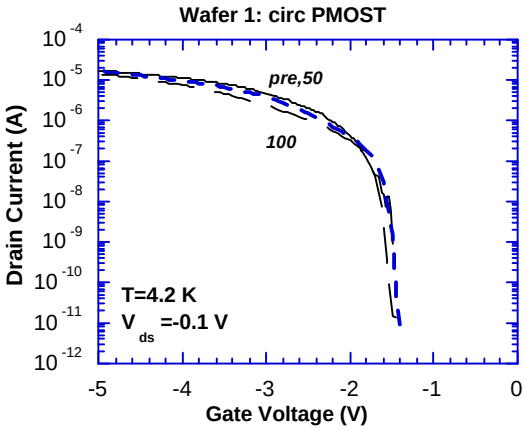


Fig. II.42. Input characteristics of a γ-irradiated #1 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

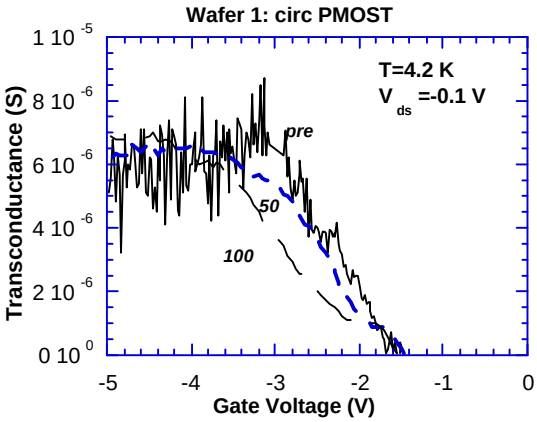


Fig. II.43. Transconductance of a γ-irradiated #1 p-MOSFET at 4.2 K and drain bias of -100 mV, corresponding to a dose of 50 and 100 krad.

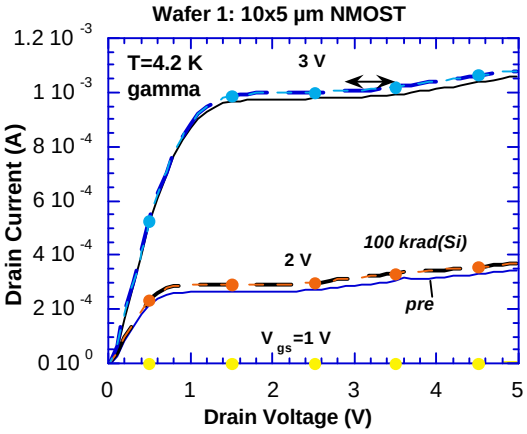


Fig. II.44. Output characteristics of a γ-irradiated #1 n-MOSFET at 4.2 K, corresponding to a dose of 100 krad. Both the LH and HL curves after 100 krad are shown.

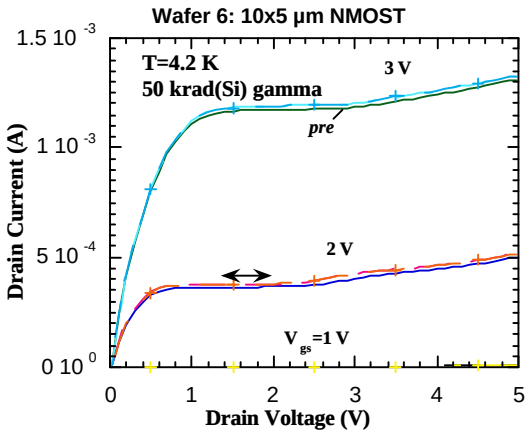


Fig. II.45. Output characteristics of a γ-irradiated #6 n-MOSFET at 4.2 K, corresponding to a dose of 50 krad. Both the LH and HL curves after 50 krad are shown.

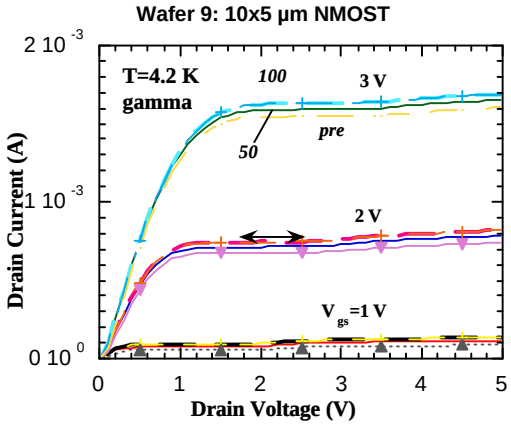


Fig. II.46. Output characteristics of a γ-irradiated #9 n-MOSFET at 4.2 K, corresponding to a dose of 50 and 100 krad. Both the LH and HL curves after 100 krad are shown.

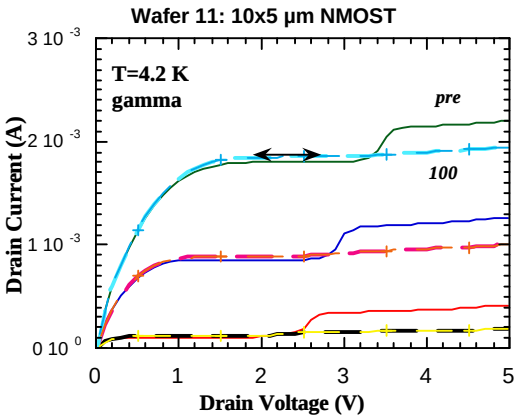


Fig. II.47. Output characteristics of a γ-irradiated #11 n-MOSFET at 4.2 K, corresponding to a dose of 100 krad. Both the LH and HL curves after 100 krad are shown.

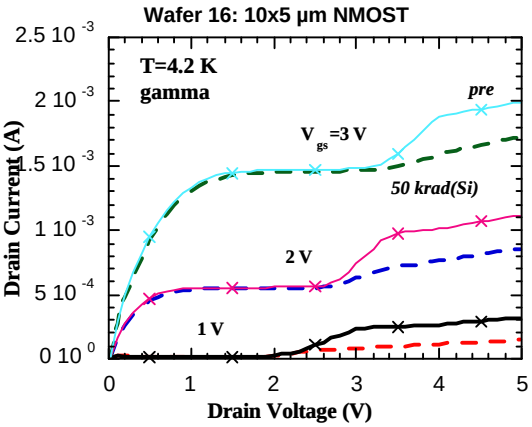


Fig. II.48. Output characteristics of a γ-irradiated #16 n-MOSFET at 4.2 K, corresponding to a dose of 50 krad.

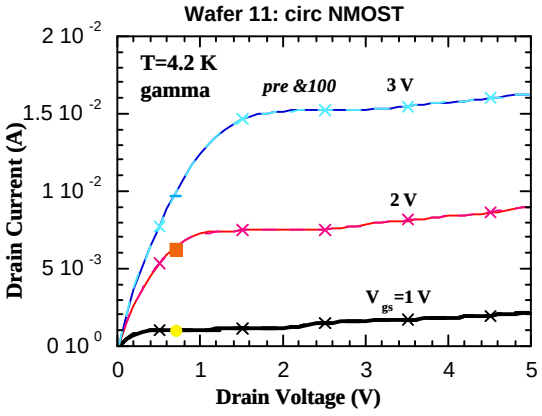


Fig. II.49. Output characteristics of a γ-irradiated #11 n-MOSFET at 4.2 K, corresponding to a dose of 100 krad.

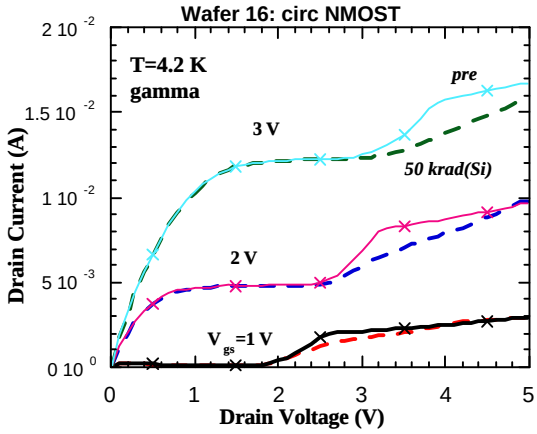


Fig. II.50. Output characteristics of a γ-irradiated #16 n-MOSFET at 4.2 K, corresponding to a dose of 50 krad.

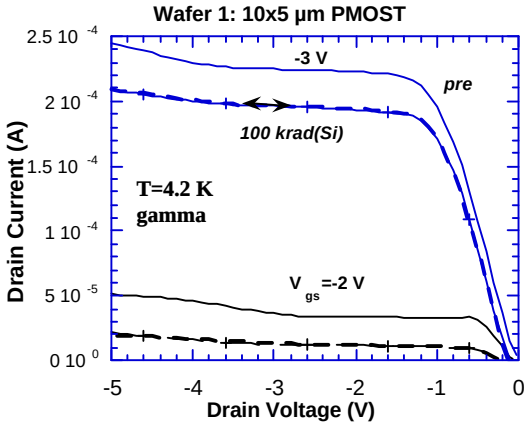


Fig. II.51. Output characteristics of a γ-irradiated #1 p-MOSFET at 4.2 K, corresponding to a dose of 100 krad. Both the LH and HL curves after 100 krad are shown.

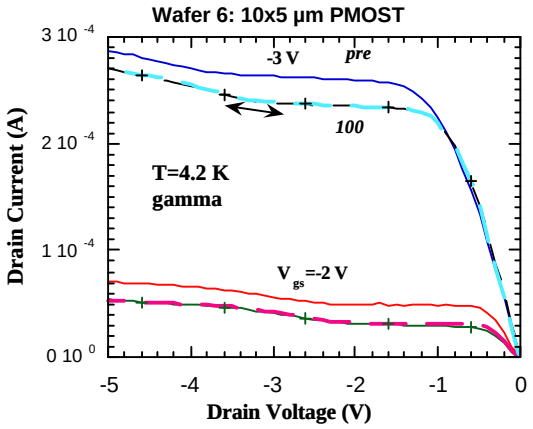


Fig. II.52. Output characteristics of a γ-irradiated #6 p-MOSFET at 4.2 K, corresponding to a dose of 100 krad. Both the LH and HL curves after 100 krad are shown.

Table II.6.a. Diary post γ-irradiation room temperature measurements.

Date	Sample	Remarks
10/06/98	1-7-7	
	1-8-7	Room Temperature
	6-5-6	
	9-5-6	
11/06/98		
	11-8-6	
	13-6-6	
	16-5-6	gate leakage p-MOSFETs
	1-8-7	RT: anneal effects?
	6-6-6	
	9-6-6	
	11-9-6	
	13-9-6	gate leakage n-MOSFETs
	16-7-6	no contact n-MOSFETs
	1-7-7	RT anneal effect ?

Table II.6.b. Diary post γ-irradiation LHT measurements.

Date	**Sample**	**Remarks**

11/06/98	1-7-7	-0.025 V --> -0.1 V p-MOSFETs
	6-5-6	n circ ?
	9-5-6	
	1-8-7	n-MOSFETs?
	6-6-6	n circ? n casc?
	9-6-6	
19/06/98	11-8-6	Leaky p-MOSFETs
	13-6-6	
	16-5-6	
	11-9-6	p-MOSFETs unstable
	13-9-6	gate leakage n and p
1/7/98	1-7-7	RT anneal effect ?
	1-8-7	
	6-5-6	
	6-6-6	floating n-MOSFETs no substrate contact
	9-5-6	
	9-6-6	

II.2.3. Device parameters after g-irradiation

Immediately after the γ-irradiation, a brief room temperature characterization has been performed. The results are summarized in Figs II.53-II.54 (n-MOSFET) and II.55-II.56 (p-MOSFETs).

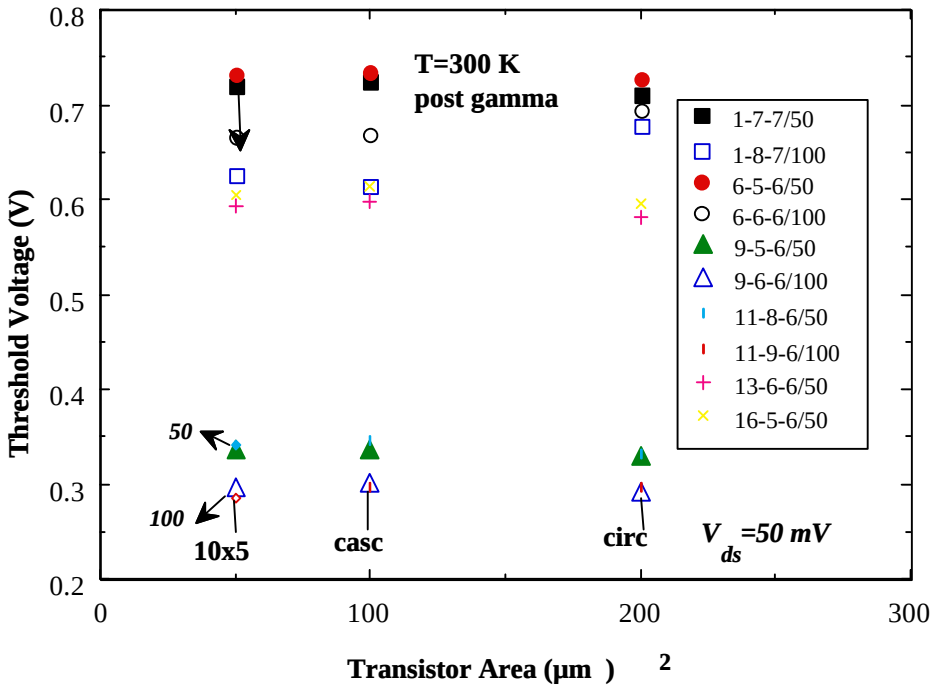


Fig. II.53. Threshold voltage at room temperature of the γ-irradiated n-MOSFETs.

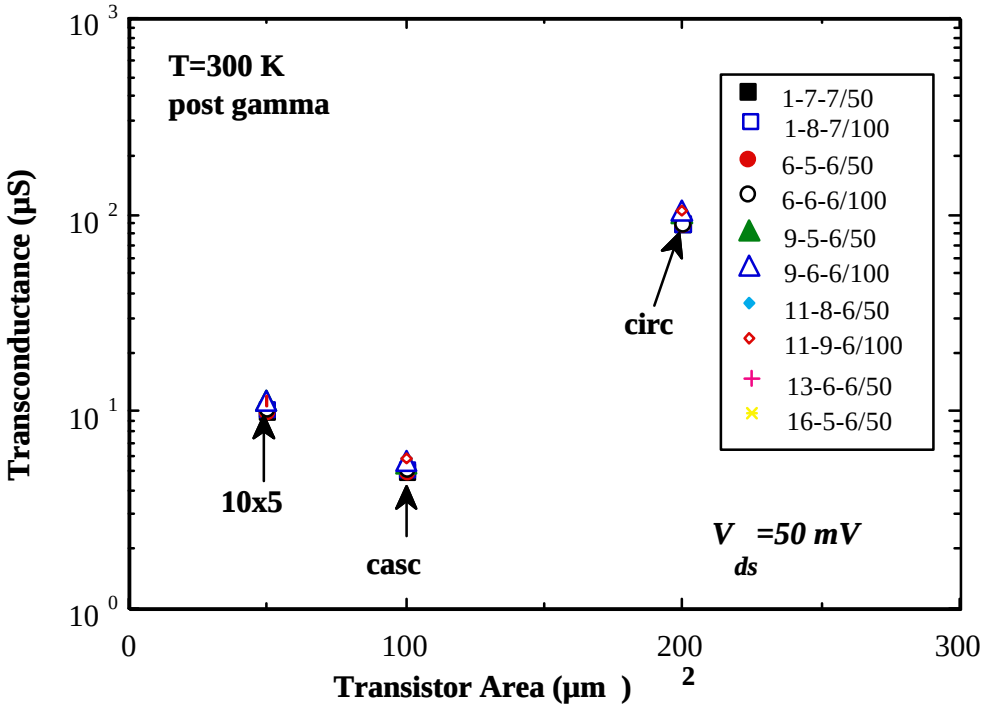


Fig. II.54. Maximum transconductance at room temperature of the γ-irradiated n-MOSFETs.

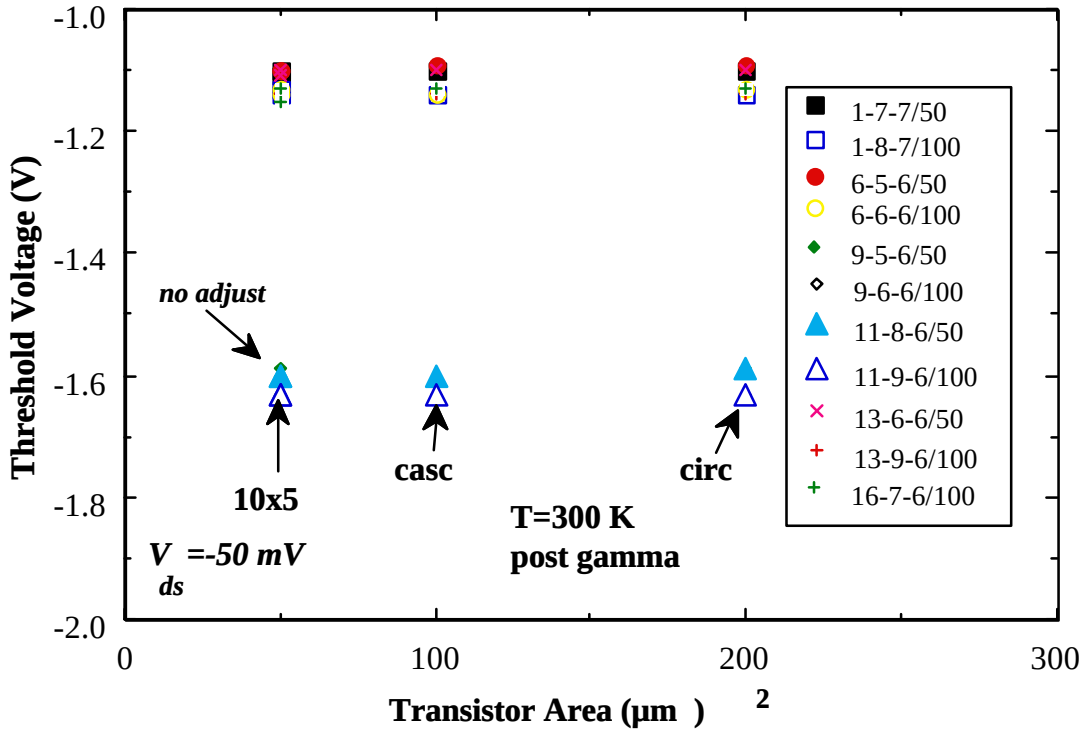


Fig. II.55. Threshold voltage at room temperature of the γ-irradiated p-MOSFETs.

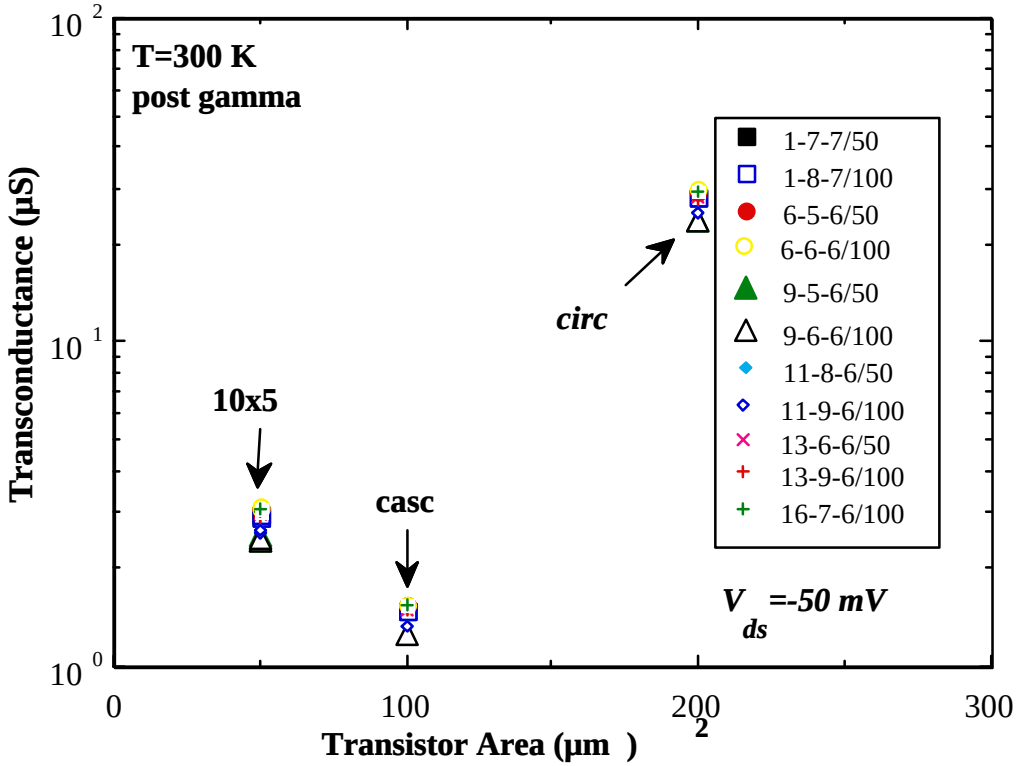


Fig. II.56. Maximum transconductance at room temperature of the γ-irradiated p-MOSFETs.

As can be seen, the threshold voltage at 300 K reduces for increasing total dose both for the n-MOSFETs (Fig. II.53) and the p-MOSFETs (Fig. II.56). The transconductance of the n-MOSFETs shows marginal changes (Fig. II.54), while a clear reduction is found for the p-channel devices (Fig. II.56). The corresponding values at LHT are summarized in Figs II.57 to II.60.

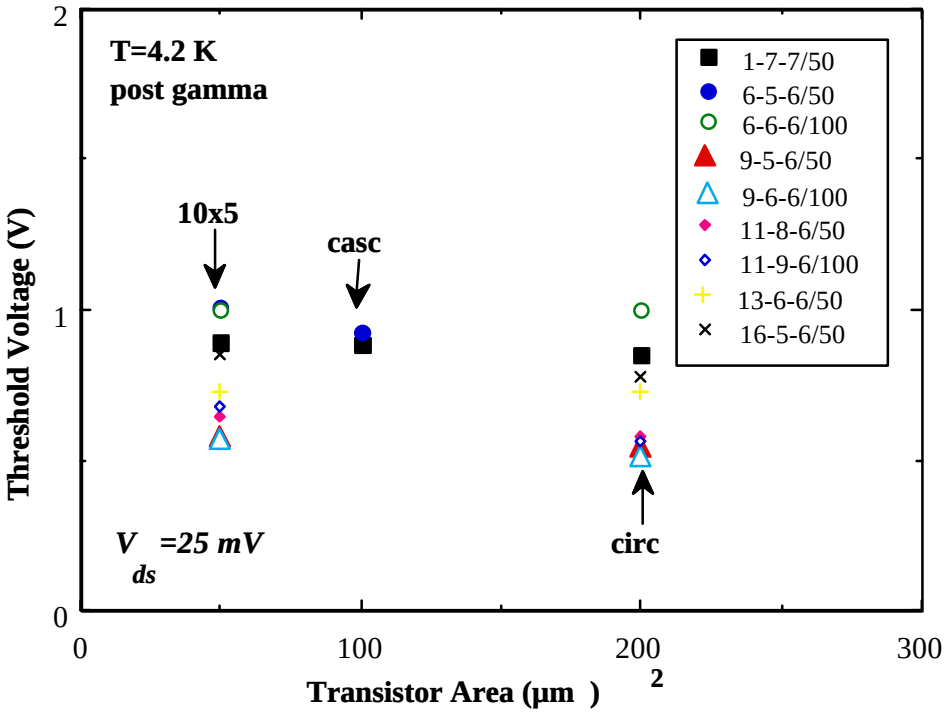


Fig. II.57. Threshold voltage at LHT of the γ-irradiated n-MOSFETs.

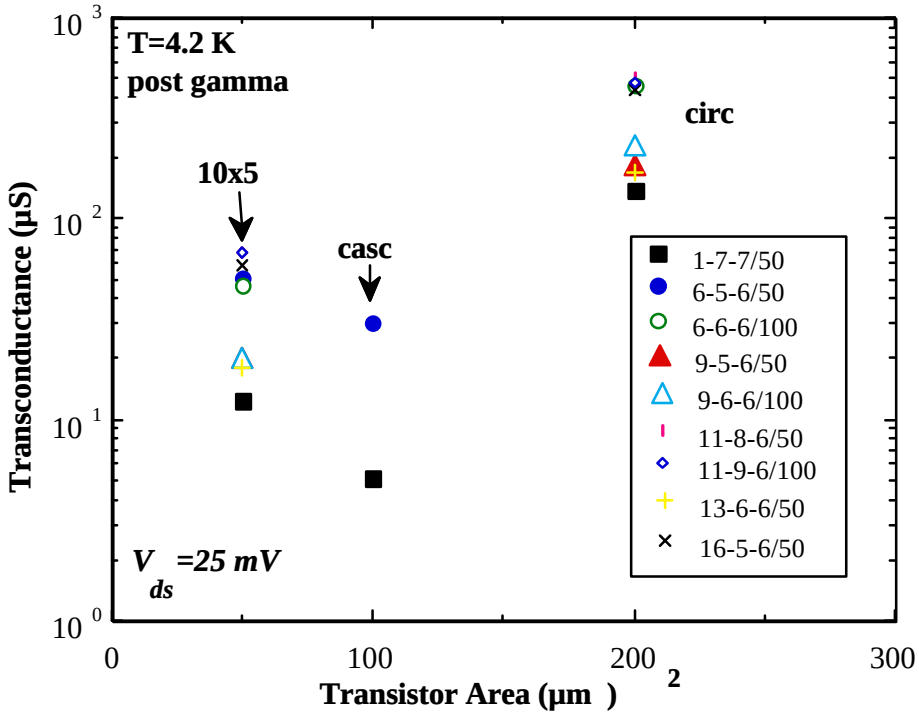


Fig. II.58. Maximum transconductance at LHT of the γ-irradiated n-MOSFETs.

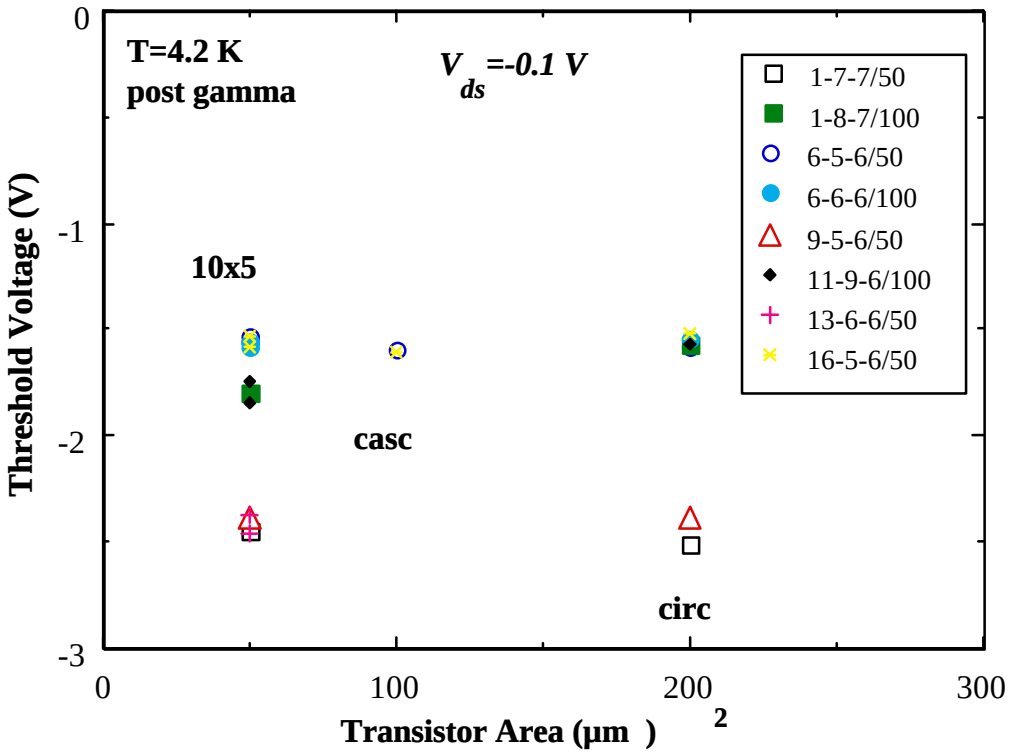


Fig. II.59. Threshold voltage at LHT of the γ-irradiated p-MOSFETs.

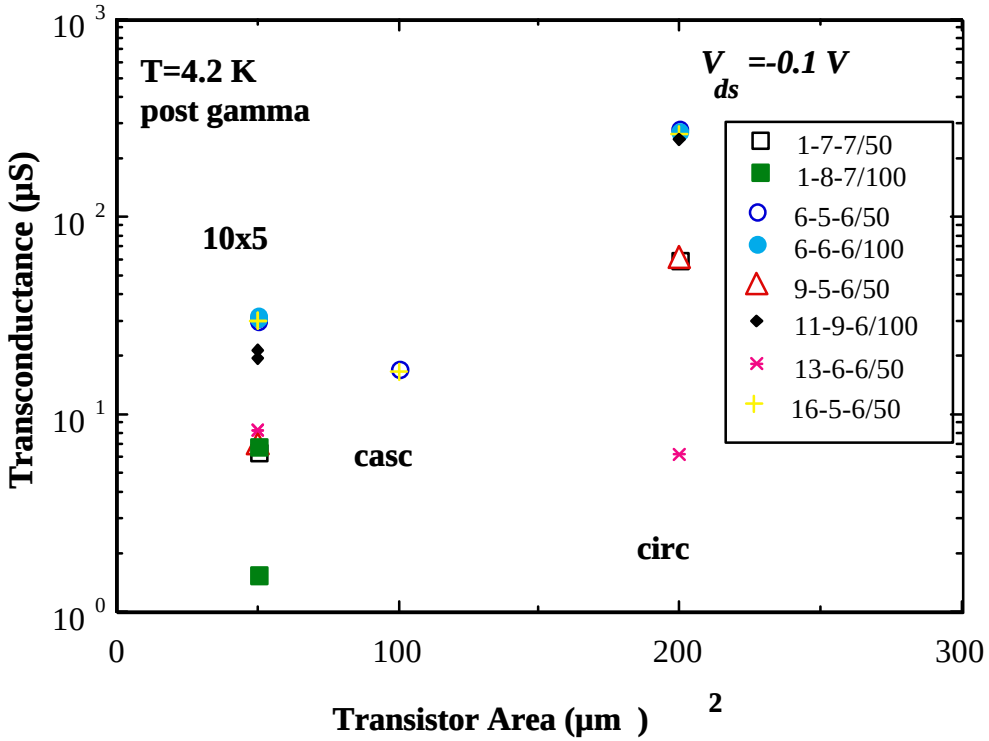


Fig. II.60. Maximum transconductance at LHT of the γ-irradiated p-MOSFETs.

In order to analyze the trends at 4.2 K more quantitatively, the observed changes in V_T and in maximum transconductance are summarized in Tables II.7 (n-) and II.8 (p-MOSFETs).

Table II.7. γ-irradiation induced changes in threshold voltage and in maximum transconductance for the non-LDD n-MOSFET at 4.2 K.

Device	ΔV_T(V)	%	Δg_{mmax} (µS)	%
6-5-6/50 n10x5	-0.13	-11.4	3.7	7.9
ncirc	---	---	---	---
6-6-6/100 n10x5	-0.14	-12.3	0.5	1.1
ncirc	---	---	---	---
11-8-6/50 n10x5	-0.04	-5.7	-1.9	-2.7
ncirc	-0.02	-2.9	4.0	0.8
11-9-6/100 n10x5	-0.01	-1.0	-2.5	-3.6
ncirc	-0.03	-5.2	-17	-.3.4

Table II.8. γ-irradiation induced changes in threshold voltage and in maximum transconductance for the non-LDD p-MOSFET at 4.2 K.

Device	ΔV_T(V)	%	Δg_{mmax} (µS)	%
6-5-6/50 p10x5	0.01	0.6	-2.4	-7.4
pcirc	-0.10	-6.8	6.4	2.3
6-6-6/100 p10x5	0.01	0.6	-0.3	-0.9
pcirc	-0.07	-4.7	-11.0	-3.9
11-8-6/50 p10x5	---	---	---	---
pcirc	---	---	---	---
11-9-6/100 p10x5	0.30	14.7	-2.3	-9.8
pcirc	0.44	21.9	+44.2	+22

Globally, no clear trends can be derived from the tables. However, in most cases, the changes in the parameters are in the range of a few % up to 10 %, similar as for the protons. Strikingly, the circular devices tend to show the opposite changes as the rectangular devices. Furthermore, no clear scaling with total dose is observed for the linear device parameters. With respect to the subthreshold slope, one can state that there is a tendency to reduce after the irradiation, although the measurement resolution is not

so very high. One should perform input measurements with very small gate voltage steps (order 1 mV) for that purpose.

II.2.4. Annealing effects

In contrast to the case of the proton irradiations, a significant change was observed in some cases between the initial post-irradiation 4.2 K measurement and a second measurement, a few weeks later. This is illustrated by the results of Figs II.61 to II.63 for n-channel devices of split 1. As can be seen from Fig. II.62, the transconductance peak has annealed out in the meantime. The same applies for the circular n-MOSFET of Fig. II.63 and for the wafer 9 n-MOSFETs (LDD devices). However, for the 100 krad case, the transconductance peak is still present after more than two weeks. At the moment, there is no clear explanation for this phenomenon. A kind of 'measurement' artifact can not completely be ruled out, although the second measurements have all been performed the same day.

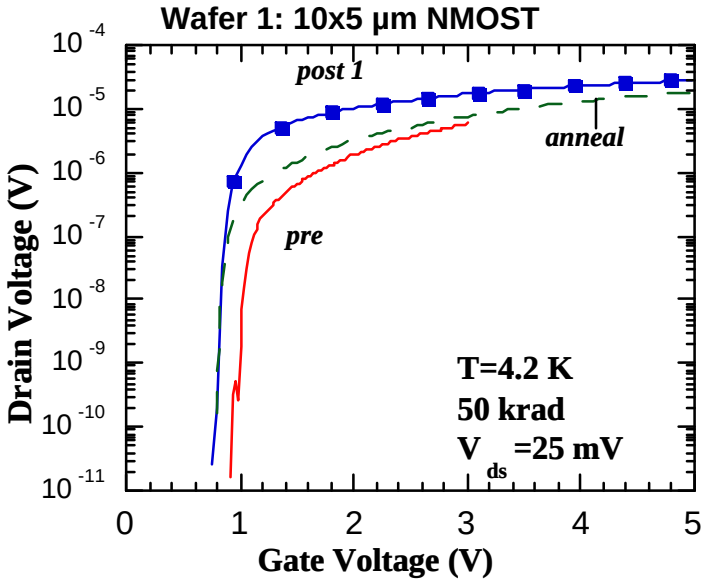


Fig. II.61. Impact of room temperature annealing on the linear input characteristics of a 10 µmx5 µm n-MOSFET, after 50 krad γ's.

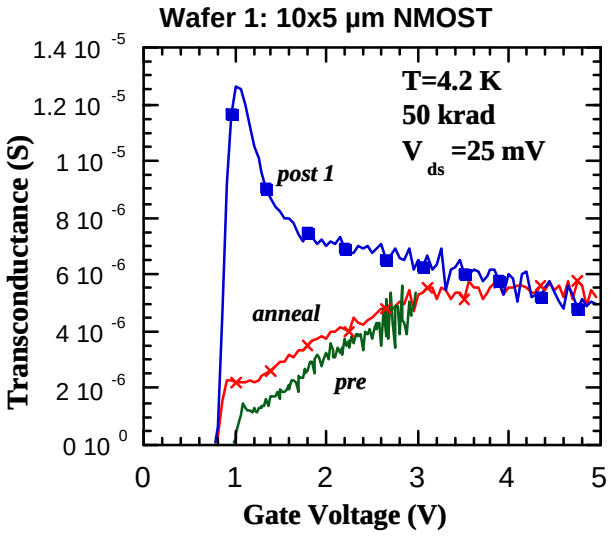


Fig. II.62. Impact of room temperature annealing on the linear transconductance of a 10 µmx5 µm n-MOSFET, after 50 krad γ's.

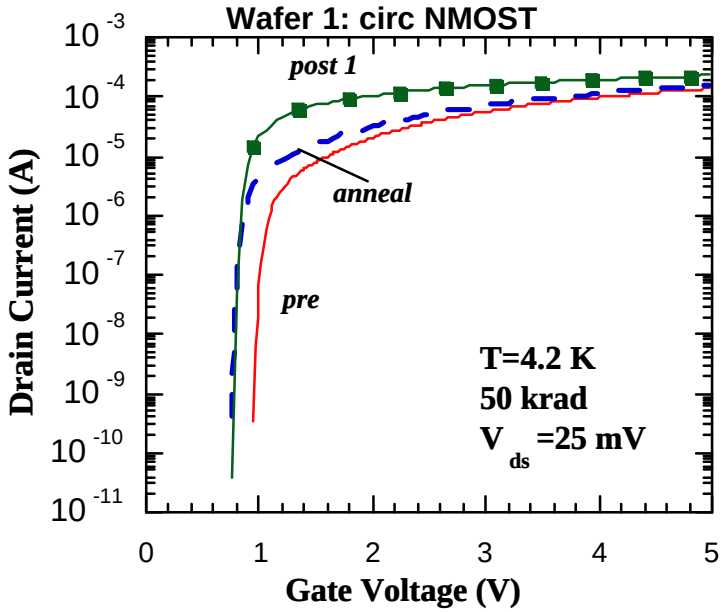


Fig. II.63. Impact of room temperature annealing on the linear input characteristics of a 10 µmx5 µm n-MOSFET, after 50 krad γ's.

The p-channel devices show little if any annealing effects, as can be seen from Fig. II.64. This is in line with the post-proton measurement results.

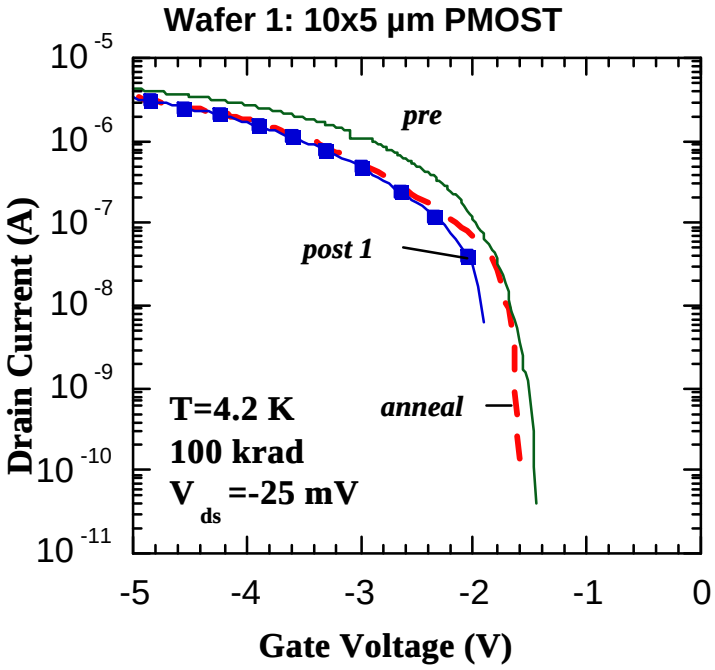


Fig. II.64. Impact of room temperature annealing on the linear input characteristics of a 10 µmx5 µm p-MOSFET, after 50 krad γ's.

II.2.5. Conclusions

The degradation at 4.2 K after room temperature γ-exposure shows the expected trends, namely, a reduction of the threshold voltage and an increase in the transconductance for the n- and opposite changes for the p-MOSFETs. This is in line with the creation of positive charge in the oxide regions. The rebound behavior found in the non-LDD p-MOSFETs after proton irradiations is not found here.

A striking result is the reduction of the kink effect after γ-irradiation, for the n-MOSFETs showing a clear kink before irradiation. The creation of positive oxide and interface charges could be well in line with these observations. No clear changes in the hysteresis behavior were observed. For the n-channel devices, the absence of the V_T adjustment implantation has a beneficial impact on the radiation hardness, with wafer 11 the most stable split.

The degradation of the device parameters is typically in the range of a few % up to 10 %. This leads to the conclusion that the technology is quite hard - at least for the room temperature irradiations. This is confirmed by the results of the circuits which show hardly any change after irradiation. There is, however, no pronounced scaling of the changes with dose. This may indicate the complexity of the degradation at 4.2 K. Another factor to take into account is the interference with room temperature annealing and partial recovery.

From a viewpoint of technology hardening, LDD devices show more pronounced changes in linear operation. Since the circuit is not using minimum length devices, one could consider removing the LDD and spacer steps from the processing. This reduces also the process complexity and number of masks. For the n-channel devices, removal of the V_T adjustment implantation seems to improve the radiation resistance. However, this leads to rather low and asymmetric threshold voltages, which may be a drawback. It should be reminded that the FIRGA design at the analog (input) side is mainly based on p-MOSFETs, which suffer far less from kink/hysteresis and other LHT artifacts.

II.3. Post-Irradiation Circuit Performance

The proton and γ-irradiations have been performed on SARP2 and SARP3 arrays. The pre-irradiation characterization consisted out of the following measurements

- functionality
- power dissipation
- number of defective channels for different integration capacitor values
- dynamic output range

and were repeated after irradiation

III.3.1. Irradiation effects on the circuit performance parameters

A comparison is made between the circuit performance before and after the different irradiations. As no difference is observed between the proton and the γ-irradiations, the type of irradiation is not mentioned anymore.

Functionality

After irradiation only 1 device was no longer working. As no performance degradation was noticed for the other devices, it may be concluded that the one circuit failure is not directly related to the irradiations but rather due to the device handling.

Power dissipation

For SARP2 device 42 μWatt at room temperature and 86 μWatt at liquid helium temperature were measured. For SARP3 devices the value is 58 and 116 μWatt, respectively. For both type of devices the same values were measured after irradiations

Defective Channels

A channel is defective if it drifts within 1s to its saturation value, due to the leakage current or a short-circuit. In most of the devices no defective channels were observed. In some cases it was observed that 2 or 3 channels per device drift to the saturation value within about 10s. For device S2-1-6-7 drift was observed in channels 1, 2 and 10. The drift in channel 10 was the largest and reached the saturation value after 6s (Cint = 10 pf).
The same measurements were done on devices before and after irradiation, and by selecting integration times resulting in a good functionality of the multiplexer. The performed irradiations had no impact on the performance of the SARP2 and SARP3s.

Dynamic Output Range

The dynamic range depends on the device biasing conditions. For SARP2 and SARP3 maximum values of 1.4 V have been achieved. The irradiations had no impact.

III.3.2. Conclusions

It can be stated that neither the proton nor the γ-irradiations have an impact on the electrical performance of the SARP2 and SARP3 circuits. Although this is a positive result, one has to be careful to conclude that the FIRST prototpye circuits are fabricated in a radiation hard cryogenic technology. The devices have been tested at cryogenic temperature, then irradiated at room temperature, and finally re-evaluated first at room and then at liquid helium temperature. The time in-between irradiation and cryogenic testing was maximum 48 hrs. However, some room temperature anneal effects can not be excluded. Also the testing at room temperature might have an annealing effect on the irradiation-induced defects. As will be discussed in the next section, some cryogenic irradiations should be done. It is important to remark that the devices have been designed in order to improve the radiation hardness during cryogenic operation. The two most important measures taken are the use of cascode amplifiers and the shielding of the

transistors. No comparison has been made between the radiation performance of circuits with and without these design features.

III. POST-IRRADIATION DEVICE CHARACTERIZATION - ROUND 2

In this section, the results of a second proton irradiation round are described and compared with the results from the first proton irradiation round(section II). For the second irradiation round, only test structures have been exposed to a 61 MeV proton beam at the Cyclone facility (Louvain-la-Neuve) on March 16, 1999. First, the radiation matrix and conditions will be described. Next, the results of the subsequent 4.2 K testing of the transistors are given, followed by a discussion and conclusion.

III.1. Proton Irradiation Matrix.

The flux of the room temperature exposure was 10^8 protons/cm^2, so that a fluence of 10^{11} cm^{-2} was reached in about 20 min. It was decided to explore higher fluences, as the changes observed in Round I (see section II) were rather small. As before, a bias of +5 V was applied to the gate of the n-MOSFETs, while the other terminals were grounded. In total 10 arrays have been irradiated, according to three different fluences (Table III.1). The description of the different splits have been given before in section I. It should be remarked that the first figure indicates the wafer number (process split).

Table III.1: Radiation matrix for the 61 MeV proton irradiations (300 K) on March 16, 1999 in Louvain-la-Neuve. A gate bias of +5 V has been applied to the n-MOSFETs, while all other terminals were grounded.

Fluence (10^{11} cm^{-2})	Sample	Remarks
1.0	T1-9-7 T6-8-6 T9-7-6 T11-5-6	p-MOS broken
5.0	T1-7-5 T9-8-6 T11-6-6 T16-6-6	n-MOS broken
10.0	T6-9-6 T13-7-6	p-MOS broken

III.2. 4.2 K Testing and Results.

III.2.1. Basic parameters

The 4.2 K characterization has been performed about one week after the irradiations due to some broken wires in the test probe. Only the 10x5 µm and the circular transistor were tested for the n-MOSFETs, while in addition, the isolated 10x5 p-MOSFET has also been evaluated. The resulting threshold voltage V_T and maximum transconductance g_{mmax} in linear operation are summarized in Table III.2. For the n-type devices a drain bias V_{ds} of 25 mV was applied, while for the p-MOSFETs -0.1 V has been utilized.

Table III.2: Basic transistor parameters at 4.2 K of the 61 MeV proton irradiated devices. Measurements have been performed on March 25-26, 1999.

Device	Fluence (10^{11} cm^{-2})	V_T (V)	g_{mmax}(µS)
T1-9-7 n10		?	?
T1-9-7 nc	1.0	1.42	48.1
T1-9-7 piso		1.93	11.2
T1-9-7 p10		-1.91	11.3
T1-9-7 pc		-1.85	101
T6-8-6 n10		1.14	50.4
T6-8-6 nc		1.03	416
T6-8-6 piso	1.0	-1.69	26.5
T6-8-6 p10		-1.63	26.2
T6-8-6 pc		-1.56	176
T9-7-6 n10		0.603	10.6
T9-7-6 nc		0.578	96.3
T9-7-6 piso	1.0	--	--
T9-7-6 p10		--	--
T9-7-6 pc		--	--
T11-5-6 n10		0.691	71.7
T11-5-6 nc		0.635	625
T11-5-6 piso	1.0	-1.70	22.4
T11-5-6 p10		-1.75	20.9
T11-5-6 pc		-1.80	223
T1-7-5 n10		0.852	14.3
T1-7-5 nc		0.529	140
T1-7-5 piso	5.0	-2.64	6.86
T1-7-5 p10		-2.65	7.73
T1-7-5 pc		-2.45	73.1
T9-8-6 n10		--	--
T9-8-6 nc		--	--
T9-8-6 piso	5.0	-2.47	8.32
T9-8-6 p10		-2.35	7.96

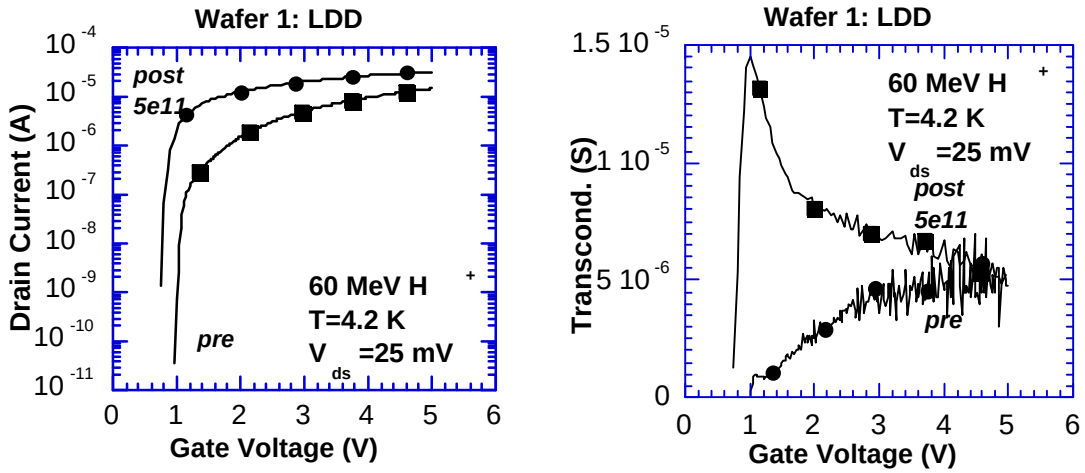
T9-8-6 pc		-2.35	74.4
T11-6-6 n10		0.667	70
T11-6-6 nc		?	?
T11-6-6 piso	5.0	-1.81	21.3
T11-6-6 p10		-1.77	21.6
T11-6-6 pc		-1.59	261
T16-6-6 n10		0.867	58.
T16-6-6 nc		0.933	494
T16-6-6 piso	5.0	-1.62	29.6
T16-6-6 p10		-1.65	29.1
T16-6-6 pc		-1.64	253
T6-9-6 n10		1.03	50.6
T6-9-6 nc		0.962	44.7
T6-9-6 piso	10.0	--	--
T6-9-6 p10		--	--
T6-9-6 pc		--	--
T13-7-6 n10		0.685	28.0
T13-7-6 nc		0.763	266
T13-7-6 piso	10.0	-2.72	6.93
T13-7-6 p10		-2.89	7.79
T13-7-6 Pc		?	?

III.2.2. Linear characteristics

The impact of the round-2 proton irradiations can be summarized as follows.

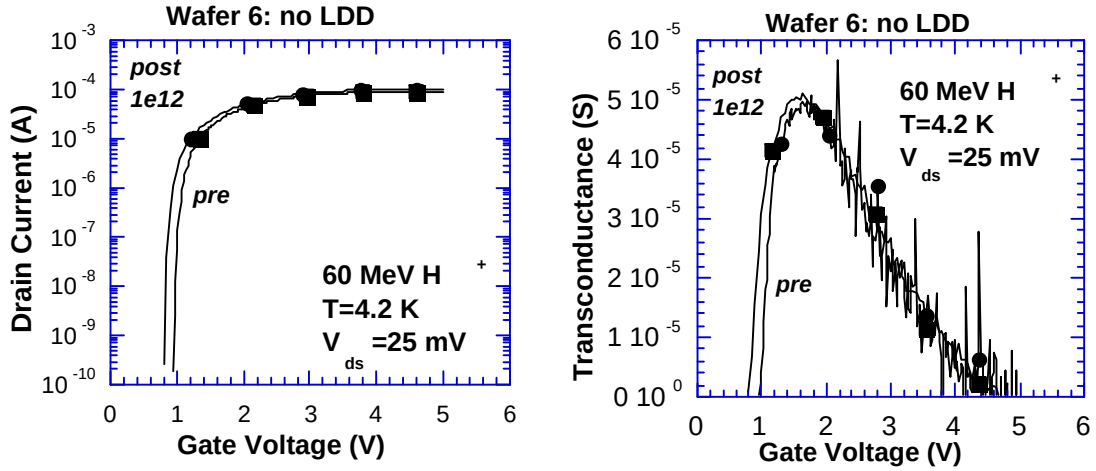
- The n-channel devices: The n-MOSFETs show an increase of the drain current I_D (Figs III.1a and III.2a) and of the transconductance g_m (Figs III.1b and III.2b) with increasing proton fluence. This is accompanied by a shift of the curves to more negative gate voltage V_{gs}, due to the reduction of the threshold voltage shown in Table III.2 This is in line with the observations reported in section II. Furthermore, the degradation is more pronounced for the LDD devices (split 1, Fig III.1) than for the non-LDD ones (split 6, Fig. III.2). This is confirmed by the results on the other splits (Figs III.3 to 6), whereby hardly no changes are observed for the wafer 11 n-channel transistors even after a fluence of $5x10^{11}$ cm^{-2}. A similar result was obtained after γ-exposure, as discussed previously. It is for example clear in Fig. III.1 that after irradiation, the transconductance of the LDD devices show a more peaked behavior, similar as their non LDD counterparts. This indicates that the impact of the source-drain series resistance and insufficient gate-source overlap reduces after the exposure, for low drain bias V_{ds}. Occasionally, a subthreshold hump appears after irradiation (see Fig. III.5, wafer 13). This could indicate radiation-induced parasitic conduction along the PBL edges of the devices. This has also been noted after γ-irradiation for one of the wafer 1 transistors (see Fig. II.22). Finally, a rather unusual result is noted for wafer 9 in Fig. III.3. Although qualitatively the degradation is as expected, the amount of shift and g_m

increase is high, compared with the previous 10^{11} cm^{-2} irradiation results (compare for example with Fig. II.9a). There is evidence from other devices as well, that the results corresponding with the Round-2 10^{11} cm^{-2} fluence are anomalous and should be considered with great care.



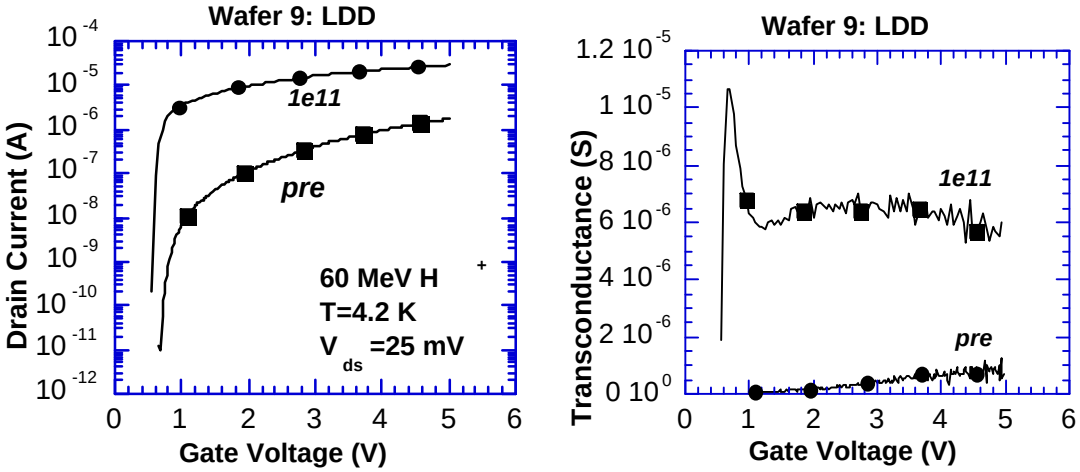
(a) (b)

Fig. III.1. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 μm n-MOSFET, belonging to wafer 1 (LDD), at V_{ds}=25 mV.



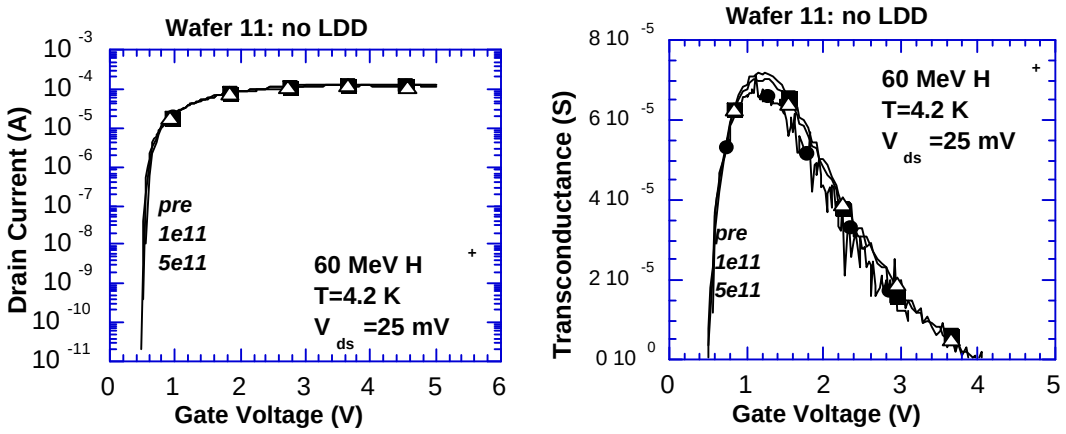
(a) (b)

Fig. III.2. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 μm n-MOSFET, belonging to wafer 6 (non LDD), at V_{ds}=25 mV.



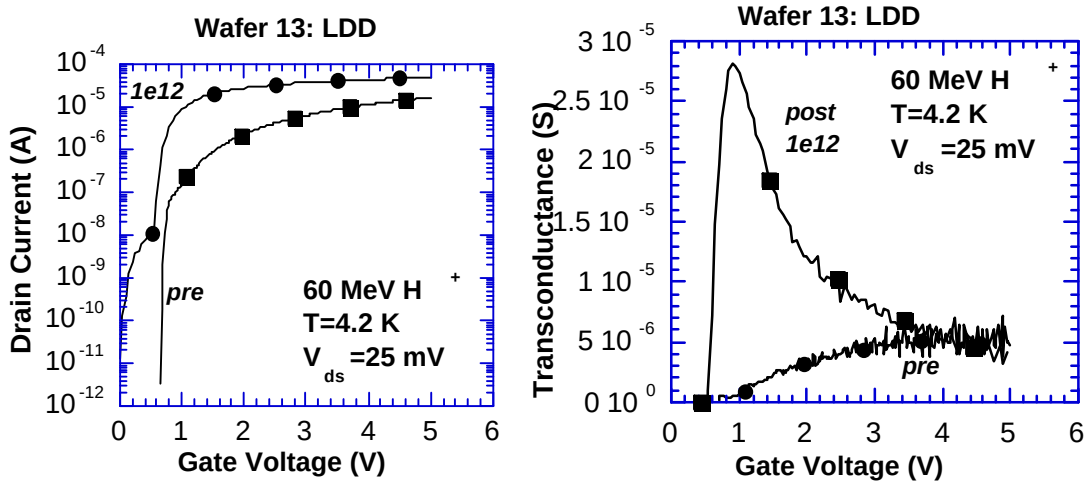
(a) (b)

Fig. III.3. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 μm n-MOSFET, belonging to wafer 9 (LDD), at V_{ds}=25 mV.



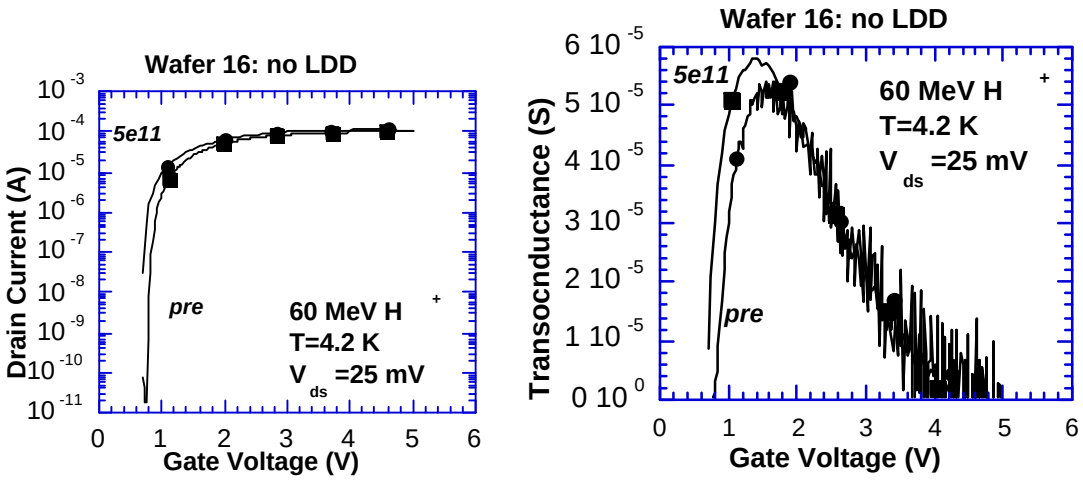
(a) (b)

Fig. III.4. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm n-MOSFET, belonging to wafer 11 (non LDD), at V_{ds}=25 mV.



(a) (b)

Fig. III.5. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm n-MOSFET, belonging to wafer 13 (LDD), at V_{ds}=25 mV.

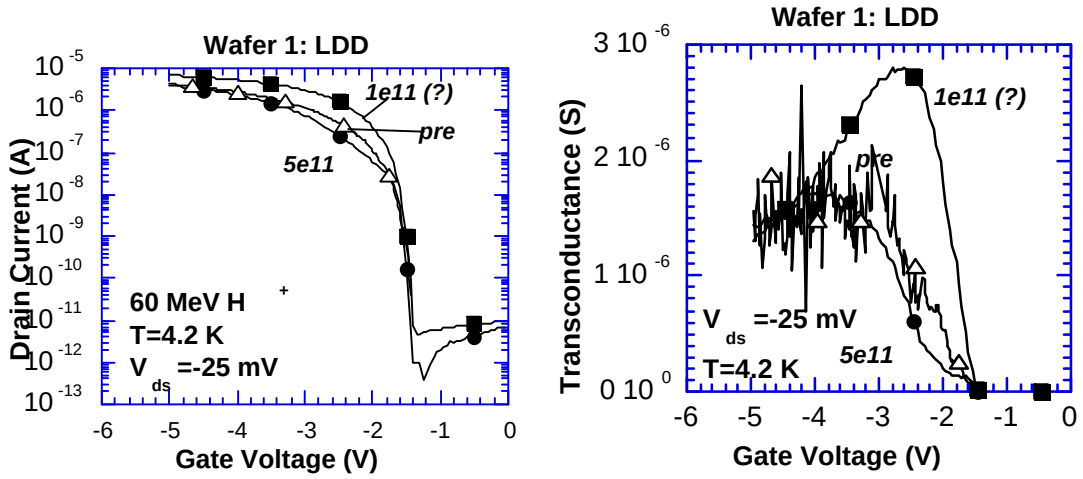


(a) (b)

Fig. III.6. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm n-MOSFET, belonging to wafer 16 (non LDD), at V_{ds}=25 mV.

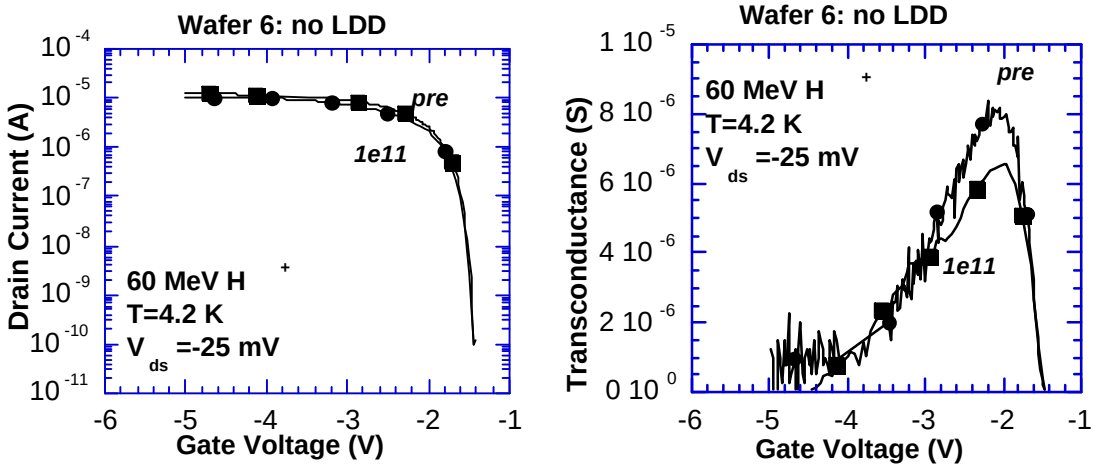
- The p-channel devices: The radiation-induced changes for the p-channel transistors are more complex and depend heavily on the processing split. For instance, LDD devices generally show a monotonous reduction of the current and the maximum transconduction with 60 MeV proton fluence, accompanied by a shift to more negative gate voltages. This is with the exception of some of the 10^{11} cm^{-2} results (Fig. III.7). The observed drain current shift is related to the lowering of the V_T, becoming more negative, due to the positive-charge trapping in the gate oxide. This is illustrated in Figs III.7 and III.11, while no marked changes have been found for split 9 devices in Fig. III.9.

For the non LDD splits (Figs III.8 and III.10), there is again a tendency to show a kind of rebound behavior noted before in Fig. II.8. This is particularly clear for the results of Fig. III.10, where the rebound seems to be shifted to even higher fluences than reported for split 6 p-MOSFETs in section II.



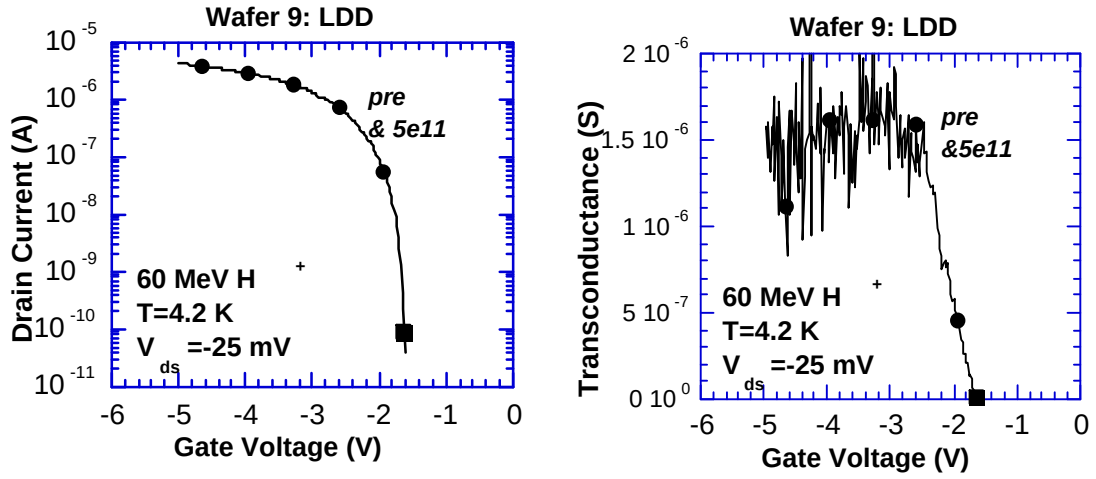
(a) (b)

Fig. III.7. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm p-MOSFET of split 1 (LDD), measured at a drain bias of -25 mV.



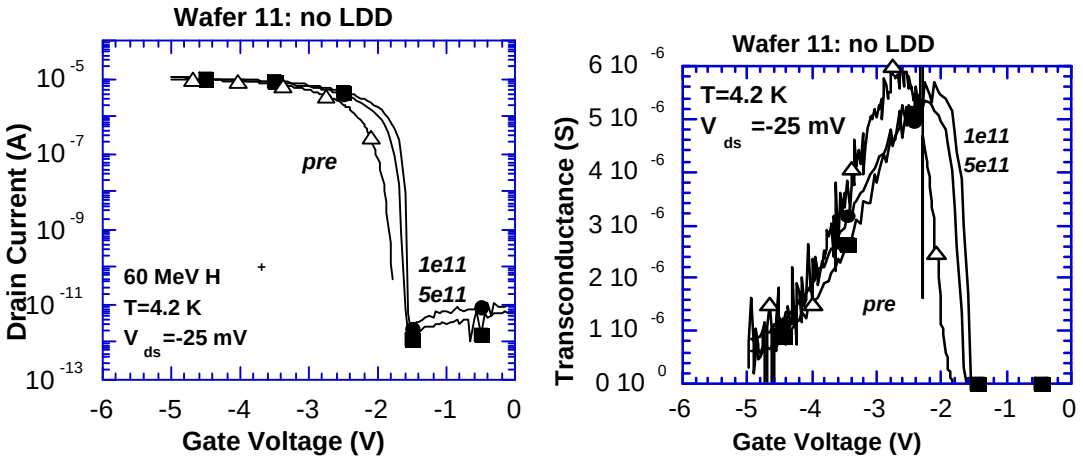
(a) (b)

Fig. III.8. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm p-MOSFET of split 6 (non LDD), measured at a drain bias of -25 mV.



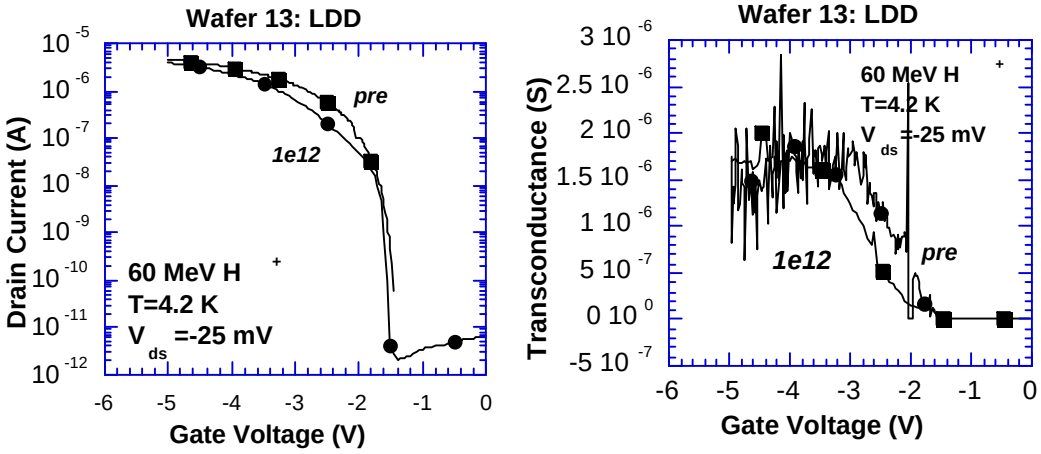
(a) (b)

Fig. III.9. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm p-MOSFET of split 9 (LDD), measured at a drain bias of -25 mV.



(a) (b)

Fig. III.10. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm p-MOSFET of split 11 (non LDD), measured at a drain bias of -25 mV.

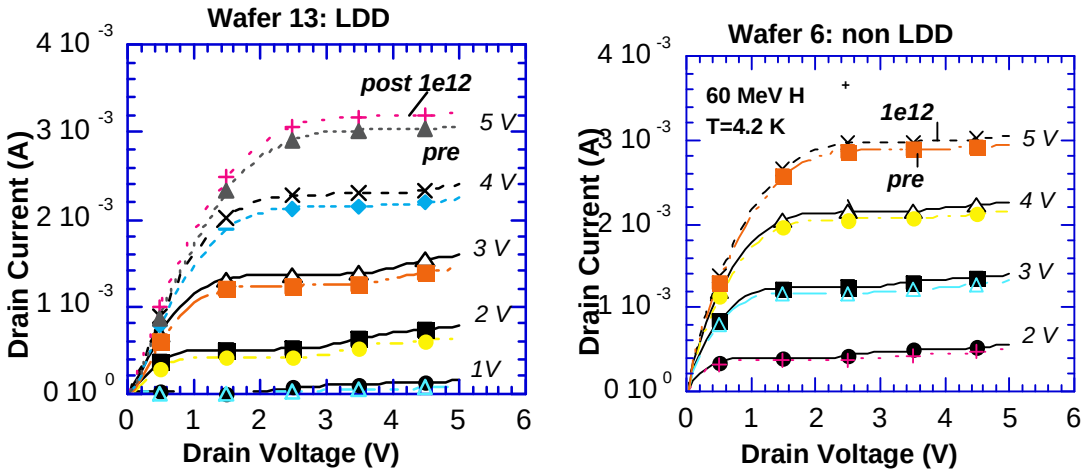


(a) (b)

Fig. III.11. Drain current (a) and transconductance (b) before and after a 60 MeV proton irradiated 10x5 µm p-MOSFET of split 13 (LDD), measured at a drain bias of -25 mV.

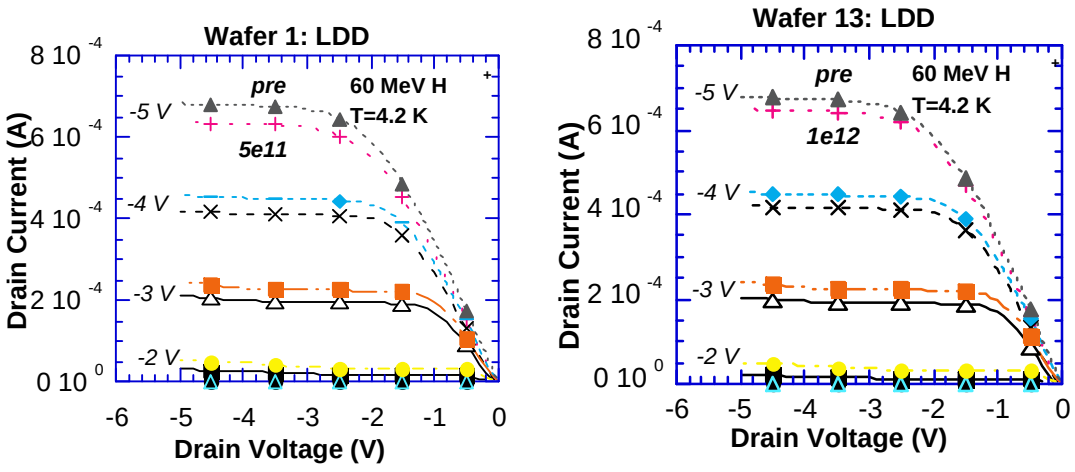
III.2.3. Saturation and kink effect

The results obtained in saturation confirm the previous observations. The n-channel devices show a slightly larger drain current, both for LDD (Fig. III.12a) and non LDD devices (Fig. III.12b). Although not shown, there is no marked increase in hysteresis, even after the 10^{12} cm^{-2} irradiations. Opposite changes are observed for the p-channel transistors in Fig. III.13.



(a) (b)

Fig. III.12. Output characteristics for a 10x5 µm LDD (a) and non LDD (b) n-MOSFET before and after a 60 MeV 10^{12} cm^{-2} proton irradiation at 300 K.



(a) (b)

Fig. III.13. Output characteristics for a 10x5 µm LDD (a) and non LDD (b) n-MOSFET before and after a 60 MeV proton irradiation at 300 K.

Finally, Fig. III.13 illustrates again the reduction of the drain current kink in saturation, observed after irradiation for non LDD n-MOSFETs. It has been suggested already that this is related to the fact that the radiation-induced positive charges in the oxide and charged interface traps cause a reduction of the multiplication current generation by increased carrier scattering.

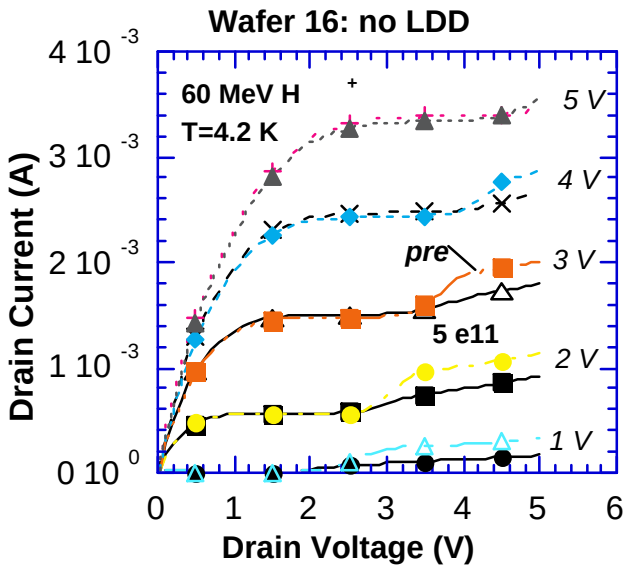


Fig. III.14. Output characteristics for a 10x5 µm non LDD n-MOSFET before and after a 60 MeV proton irradiation at 300 K.

III.2.4. Linear characteristics versus 60 MeV proton fluence.

Combining the data of both "60 MeV" proton irradiation rounds per split, the following trends can be derived. For the standard wafer 1 transistors (with LDD), a continuous roll-off of the threshold voltage is found for the n-MOSFETs (Fig. III.15). Assuming a more or less linear variation with fluence Φ, a value of 20 mV/10^{10} protons/cm^2 is found for the rectangular 10x5 µm^2 devices, which is approximately the same for the circular ones. Note in Fig. III.15 the anomalous (?) 10^{11} cm^{-2} data point(s) (Round 2 irradiation), which differ significantly from the first round results. This is confirmed by the data on the other arrays. The maximum transconductance of the n-MOSFETs increases with Φ and tends to saturate for the larger fluences studied (Fig. III.16).

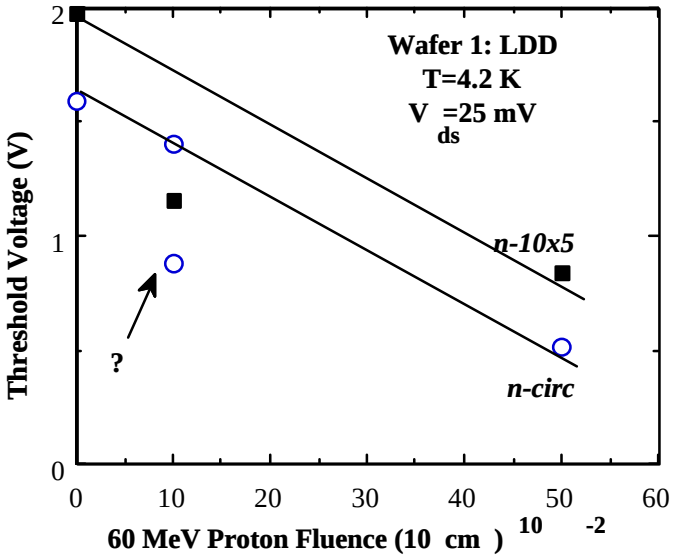


Fig. III.15. Threshold voltage as a function of 60 MeV proton fluence for the 10x5 µm^2 and the circular n-MOSFETs of split 1.

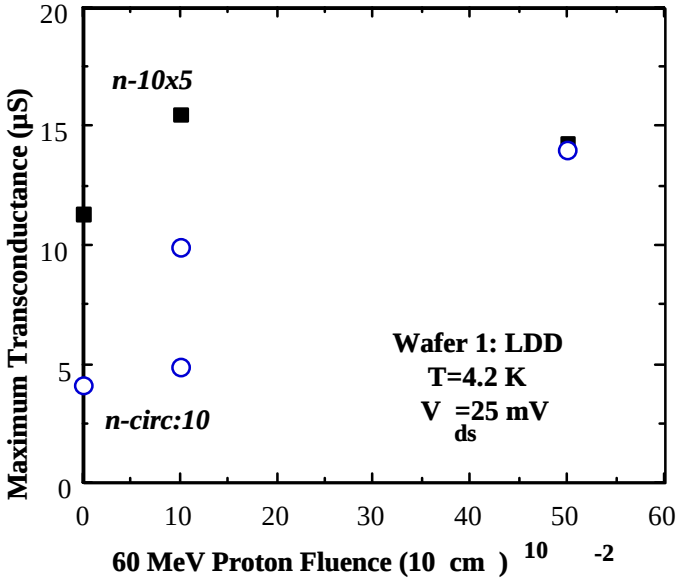


Fig. III.16. Maximum transconductance of the 60 MeV proton irradiated n-MOSFETs of split 1 in function of the fluence. The data for the circular devices has been divided by 10.

For the p-MOSFETs the opposite trends are observed in Figs III.17 and III.18. It should be noted that the linear characteristics in Round 2 have been obtained for a drain bias of -0.1 V. This has been taken into account in the derivation of the parameters by correcting the linearly extrapolated V_T by $-V_{ds}/2$ and by dividing the g_{mmax} by a factor 4, to normalise to a V_{ds}=-25 mV. Overall similar trends have been found for the other LDD splits (wafer 9,13). Note again the anomalous behaviour of the Round-2 10^{11} cm^{-2} data, showing an unusual increase (more positive) of the V_T.

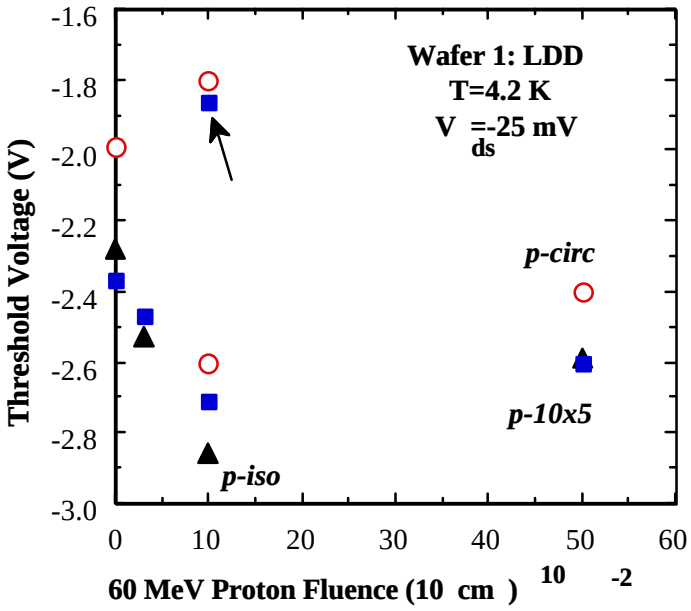


Fig. III.17. Threshold voltage as a function of 60 MeV proton fluence for the isolated (iso), the 10x5 µm^2 and the circular p-MOSFETs of split 1.

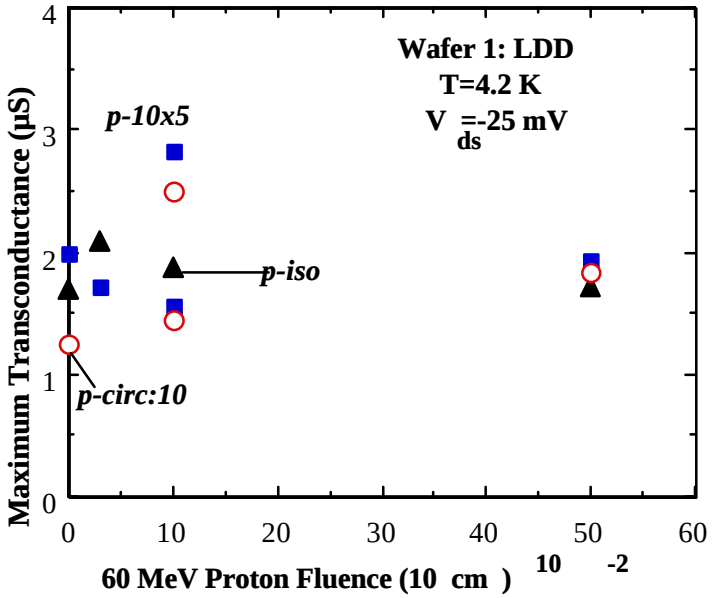


Fig. III.18. Maximum transconductance of the 60 MeV proton irradiated p-MOSFETs of split 1 in function of the fluence. The data for the circular devices has been divided by 10.

The picture is somewhat different for the non LDD devices (wafer 6), as already reported in section II. Figure III.19 demonstrates the results for the threshold voltage of the irradiated n-MOSFETs. The decay rate of the V_T is much lower than for the LDD devices and amounts to about 1 mV/10^{10} protons/cm^2. This points clearly to the detrimental impact of the LDD+spacer oxide on the linear current-voltage characteristics of the devices. One of the reasons is that due to insufficient gate overlap in the LDD devices, there exists a so-called drain-voltage threshold, which disappears for sufficiently large V_{ds}. Alternatively, one can think of a drain bias dependent series resistance, which lowers with increasing lateral field (see the literature overview [1]). Comparing Fig. III.19 with Fig. III.15, it becomes evident that for large Φ, the threshold voltage of both splits tend to similar values, at least for the rectangular devices. However, the fact that the circular transistors of split 1 show a more pronounced V_T reduction suggests that the presence of the spacer oxides forms an additional hardness risk. It is shown here that the non LDD transistors are inherently more radiation tolerant than the LDD ones, confirming the conclusions reached before. With respect to the transconductance, a gradual increase with fluence, followed by a saturation at higher Φ is found in Fig. III.20. The peak g_m is also a factor of 3 larger for the non LDD devices (compare with Fig. III.16). The Round-2 10^{11} cm^{-2} data stand out again, compared with the first results, both for V_T (Fig. III.19) and g_{mmax} (Fig. III.20).

Some interesting phenomenon occurs for the p-channel devices of split 6 (non LDD). It has been noted before that for low proton fluences a kind of rebound behavior occurs in both the V_T and the g_m. This is illustrated by Figs III.21 and III.22. Instead of the expected decrease of the threshold voltage upon irradiation (towards more negative values) the opposite is observed, i.e. the V_T becomes more positive. In fact, for the Round-2 10^{11} cm^{-2} data, V_T becomes even more positive in Fig. III.21, although it is believed that these data are somewhat anomalous. Similar type of rebound is noted for

the transconductance in Fig. III.21. These results are further supported by Figs III.23 and III.24, obtained on the p-MOSFETs of split 11 (non LDD).

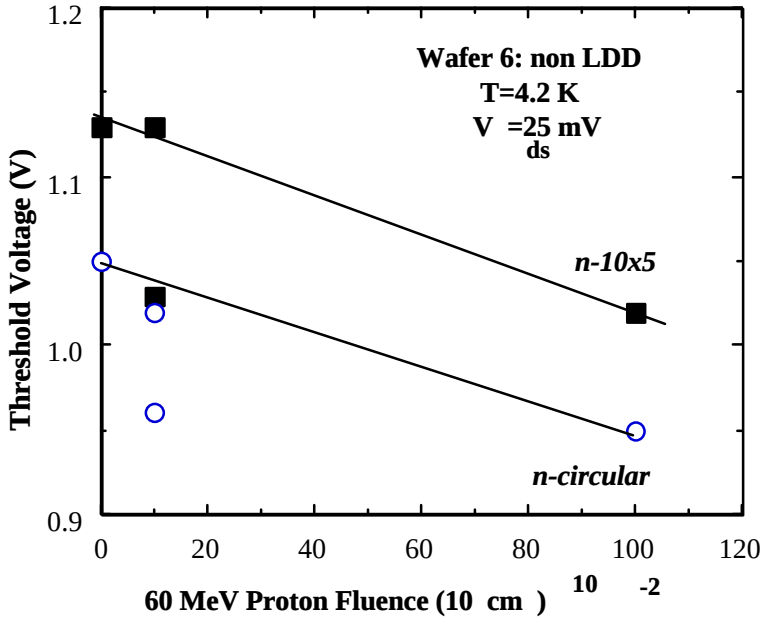


Fig. III.19. Threshold voltage as a function of 60 MeV proton fluence for the 10x5 μm^2 and the circular n-MOSFETs of split 6.

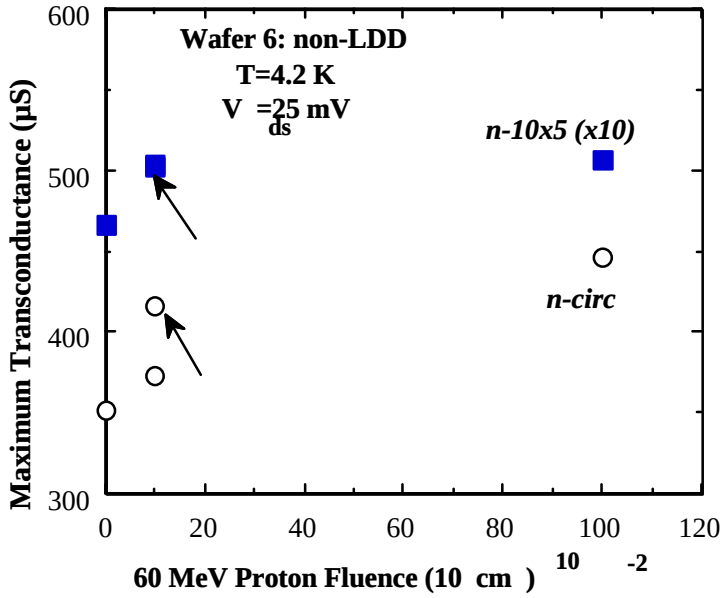


Fig. III.20. Maximum transconductance of the 60 MeV proton irradiated n-MOSFETs of split 6 in function of the fluence. The data for the 10x5 μm^2 devices has been multiplied by 10.

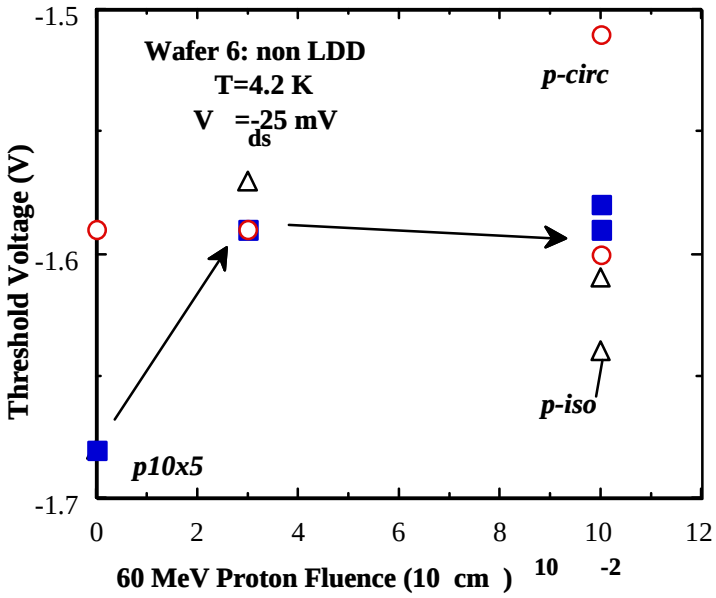


Fig. III.21. Threshold voltage as a function of 60 MeV proton fluence for the isolated, the 10x5 μm^2 and the circular p-MOSFETs of split 6.

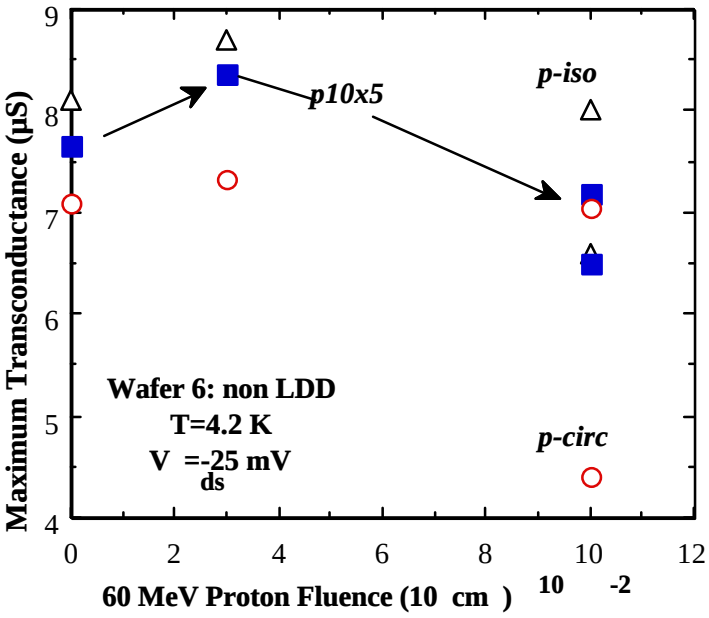


Fig. III.22. Maximum transconductance of the 60 MeV proton irradiated p-MOSFETs of split 6 in function of the fluence. The data for the circular devices has been divided by 10.

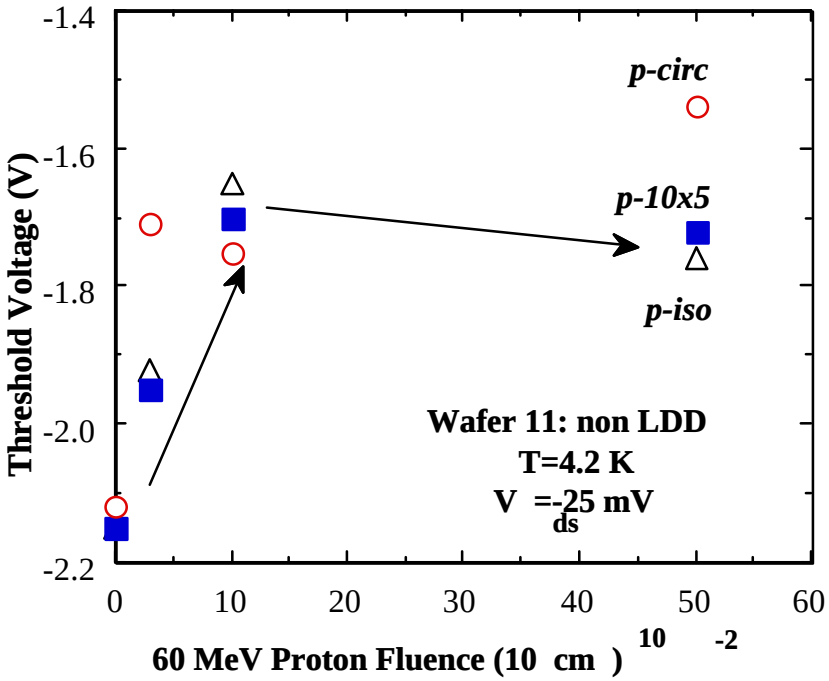


Fig. III.23. Threshold voltage as a function of 60 MeV proton fluence for the isolated, the 10x5 μm^2 and the circular p-MOSFETs of split 11.

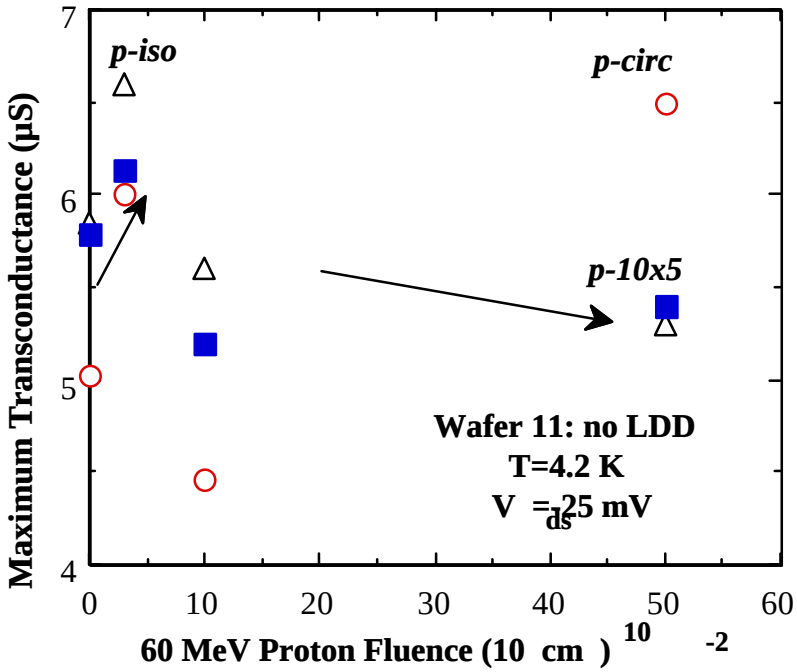


Fig. III.24. Maximum transconductance of the 60 MeV proton irradiated p-MOSFETs of split 11 in function of the fluence. The data for the circular devices has been divided by 10.

III.3. Conclusions

A first general conclusion is that the second round proton irradiations in first instance confirm the previous results and further support the conclusions and recommendations which were reached. Non LDD devices clearly outperform LDD ones from a viewpoint of radiation tolerance. This goes in fact also for the pre-radiation behaviour. Splits 6 and 11 are therefore recommended for further processing, whereby 6 requires the least changes to the standard processing.

In addition, the trends found previously have been confirmed. They include:

* a rebound behavior for the proton irradiated non LDD p-MOSFETs, which causes the characteristics to improve slightly after irradiation. This is undoubtedly related to a partial room temperature annealing during and after the exposure.

* a reduction of the drain current kink after proton irradiation for the non LDD n-MOSFETs. This is related to the reduction of the multiplication current generation.

* a more or less linear V_T roll-off has been found for the n-channel devices at 4.2 K, up to 60 MeV fluences of 10^{12} cm^{-2}. The roll-off is 20 times larger for the LDD n-MOSFETs compared with non LDD transistors. This points to the significant role played by the LDD+spacer regions in the degradation.

IV. CRYOGENIC IRRADIATIONS

It was stated in the conclusions of Deliverable D1 [1] that for displacement damage studies room temperature irradiation is a kind of worst case situation. This implies that no direct cryogenic irradiations are needed if one accepts that the taken measures to improve the radiation hardness are maybe an overkilling of the problem.

For total dose effects the situation is quite different. Operation at 77 K prevents the trapped holes first of all to move towards the negative interface and secondly to escape (tunnel), to recombine, to annihilate or to be transformed into interface traps. Therefore it is expected that the degradation of the field and eventually also of the gate oxide will be more pronounced during low temperatures irradiations. As also stated before, while some information can be found in the literature for 77 K irradiations, this is not the case for irradiations at liquid helium temperatures. This is very important for the studied FIRST prototypes as they have to function at LHT.

The main problem with the cryogenic irradiations are related to the following aspects:

- The irradiations have to be performed while the devices are cooled. This may cause some hardware configuration problems. There are not many irradiation facilities offering this option.
- The device and circuits have to be kept at cryogenic temperature untill after the post-irradiation characterization have been completed. This implies that one either needs access to test facilities near the irradiation place or that one has to transport the devices in a cooled Dewar. The latter may cause some problems with the safety regulations.

During the last year, several irradiation facilities have been contacted in order to check the possibility to have some cryogenic irradiations done. In most of the cases, no experience in the field was available. Some past experience exists in the Semiconductor Physics Laboratory in Kiev, Ukraine. They have, however, not the appropriate test equipment available.

As the radiation hardness assessment of the cryogenic electronics is gaining importance for future missions, IMEC has decided to allocate some effort to try to set up a cryogenic irradiation facility at Louvain-La-Neuve. For the moment the diffferent hardware aspects and the required safety regulations are under study.

V. CONCLUSIONS AND RECOMMENDATIONS

The experimental study allows drawing some important conclusions, especially related to the technology used for the fabrication of the cryogenic electronics, which will be applied for the prototypes. One has to differentiate between on one hand the irradiation type (protons or gamma's) and on the other hand between the device and the circuit performance.

For the studied fluences the impact of proton irradiation on the electrical device performance is typically of the order of 10%. A pronounced influence is seen when there is a Lowly Doped Region present. While for p-channel devices with LDDs the expected irradiation induced reduction of the threshold voltage and drain current is observed, non-LDD devices can show a rebound effect. The latter implies that for moderate fluences the drain current increases, while for higher fluences a reduction is noticed.

In the case of γ-irradiation the classical device performance degradation is observed, i.e. a reduction of the threshold voltage and an increase of the transconductance for n-channel devices and the opposite trend for p-channels. In contrast to the proton irradiations, no rebound effect is seen for the non-LDD p-channels. A particular feature, observed for the first time according to the author's knowledge, is the fact that γ-irradiations can reduce the pre-irradiation kink effect present in n-channel devices operating at cryogenic temperatures. This might be explained by the generation of positive oxide and interface charges. The well-known occurrence of hysteresis effects at cryogenic temperatures is not influenced by the irradiations. Although the used technology is quite hard from a total dose viewpoint, a further hardening is obtained by eliminating the threshold voltage adjustment ion implantation. There is no clear scaling of the performance degradation with the fluence.

The study of the post-irradiation device performance leads to the conclusion that the highest radiation hardness is achieved for a technology without LLD's, transistors without oxide spacers and removal of the threshold voltage adjustment implant. The latter may have an impact on the symmetry of the threshold voltages for the n- and p-channel devices. Whether or not the LDDs and the spacers can be eliminated depends on the minimum feature size of the circuits.

The study of the post-irradiation performance of the FIRST prototype circuits points out that the used technology is sufficiently radiation hard for the studied proton and total dose irradiations. However, it is essential to remark that in the case of total dose radiation hardness assessment room temperature irradiations are not the worst case situation. It is therefore essential to perform also some cryogenic irradiations.

The main recommendations for future activities related to the above mentioned conclusions are:

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- Modeling experiments in order to explain quantitatively the basic mechanisms leading to a reduction the kink phenomenon during cryogenic operation.
- Execution of low temperature irradiations in order to study in detail the total dose irradiation hardness of both the devices and the circuits.

- Dedicated experiments in order to determine the differences between room temperature and cryogenic irradiations to point out the impact of possible room temperature annealing effects in the first case.

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