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Manual for Cryogenic Electronics in Space Applications

Deliverable D3

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Abstract

This report constitutes the Deliverable D3 of Work Order 1938/96/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials". It formulates some practical guidelines for the development, design and testing of radiation hard cryogenic electronics, intended to operate at liquid helium temperature. Attention is given to the impact of the technology optimization for cryogenic operation on the radiation hardness. The dedicated approach needed for the extraction of the cryogenic device parameters is also addressed. In general, the report should be considered as a summary of the two previous reports associated with this Work Package, ie.e. the critical literature overview given in Deliverable D1 and the Cryogenic Radiation testing reported in Deliverable D2.

INTRODUCTION ESA_QCA00169T_C

This reports constitutes Deliverable D3, associated with RFQ/3-8938/97/NL/NB on “Study of Radiation Effects in Cryogenic electronics and Advanced Semiconductor Materials “ – Activity 1 related to Radiation Effects in Cryogenic Electronics. This 18 months activity started with a literature study on the radiation effects in cryogenic electronics, the result of which is summarized in depth in Deliverable D1 (doc. P35284-IM-RP-0003). Afterward, two irradiation rounds have been performed in order to generate additional data and to validate the main conclusions of the literature study. The experimental details of the irradiation rounds, together with an in-depth discussion of the obtained results are addressed in Deliverable D2(doc. P35284-IM-RP0012).

The objective of deliverable D3 is to formulate some practical guidelines for the development, the design and the testing of radiation hard cryogenic electronics intended for operation in the liquid helium temperature (LHT) range. They are formulated keeping two main goals in mind: first, successful operation at 4.2 K and, second, providing sufficient resistance against (space) radiation damage. As it is a summary report highlighting the key issues, the report is aimed to be concise and contains three parts. Part 1 is focusing on technology aspects, part 2 on design guidelines and in the third part some testing prescriptions are highlighted. As such, it can be considered as a summary of the two previous reports: the literature overview deliverable D1 [1] and the Cryogenic Radiation Testing report D2 [2] and, therefore, constitutes an update of the preliminary guidelines proposed in D1.

I. TECHNOLOGICAL ASPECTS

As a CMOS technology designed for cryogenic applications requires an optimization of some important process modules, a first section discusses the impact of key technological modifications on the pre-irradiation device- and circuit performance. Subsequently, the impact of process optimizations (from a cryogenic operation viewpoint) on the overall radiation hardness is addressed.

I.1 Pre-irradiation Performance

It is well known from previous studies that the current-voltage (I-V) characteristics of CMOS devices at LHT are a sensitive function of the processing conditions. In fact, even within the same technology, differences can be observed from batch to batch, implying that it is more difficult to control the cryogenic device performance due to an increase of the dispersion of the device parameters. One basic reason is that fluctuations occurring for example on a wafer level can be smeared out or smoothed at room temperature (RT) by the thermal energy. In other words, fluctuations smaller than kT (k Boltzmann's constant and T the absolute temperature) are not relevant in first instance. Given the proportional temperature dependence, it is readily derived that while 25 mV differences at 300 K are within the statistical limits, the value at 4.2 K is 300 times lower.

Another issue is that the most commonly used device simulators are not very well suited for predicting LHT operation, so that it is hard to predict essential static device parameters like e.g. the threshold voltage V_T, for given processing conditions. This means that the development of cryogenic CMOS is still more of an art and is heuristic in nature. Nevertheless, based on the IMEC experience in this field, gained over the past decade and on what is available in the open literature, the impact of a number of processing steps can be described quite accurately and their appropriateness for cryo-electronics judged upon. Within the frame of the present study, special attention was devoted to the following aspects: the presence of lowly doped drains (LDDs), the role of a p-well implantation (n-channel devices) and the role of a V_T adjust implantation. Some conclusions and trends can be drawn from this study.

While the presence of an LDD is beneficial for the room temperature operation of submicron devices, since it helps to increase the device lifetime by lowering the maximum electric field near the drain and thereby impacting short-channel effects such as e.g. hot carrier phenomena, its role at 4.2 K is far less advantageous. The major obstacle is that the LDD enhances drastically the parasitic

series resistance of the device, particularly for small drain bias V_{ds}. As a result, the device conductance in linear operation becomes lower at 4.2 K than at room temperature, so that the mobility increase advantage of cryogenic operation is lost. This effect becomes more pronounced for smaller gate-lengths of the device [3]. This has some important consequences for practical parameter extraction at 4.2 K as will be seen below.

Another problem is the fact that the associated series resistance R_S at 4.2 K becomes a function of the lateral electric field (the drain bias) [4]. This makes the extraction of both R_S and the length reduction ΔL more difficult, requiring a specific approach.

The increase of R_s is associated with the freeze-out of carriers in the LDD regions. As these regions are generally not degenerately doped like the source and drain regions, the density of free carriers can become quite small below 50 K typically [4], resulting in a low conductivity. It has also been observed that the LDD devices can show high low-frequency (LF) noise. It has for example been found that so-called Random Telegraph Signals (RTSs) occur at 4.2 K, even in fairly large structures [5]. The signals are thought to arise from the non-overlap interface region of the spacer oxides. Particularly for analog circuits (amplifiers, read-out electronics,…) this is a highly undesirable feature.

Based on this, it is concluded that a non-LDD architecture is to be preferred for LHT circuits, as long as the required minimum feature size is above 1 μm or so. For deep submicron technologies, LDDs (or extensions) are present in most cases. Fortunately, as the dimensions shrink, the doping density of the LDDs has to increase so that it is expected that freeze-out effects could be less of a problem there. Nevertheless, the implantation has to be optimized in order to achieve good cryogenic performance, as demonstrated in Ref. 3 for example.

With respect to the presence of a p-well, the following conclusions hold. No p-well enhances the freeze-out effect and the resistance (impedance) of the substrate at

4.2 K. This causes pronounced kink and hysteresis in the I-V curves [6]. In addition, the LF noise in the kink region shows a pronounced increase due to an associated generation-recombination (GR) component [5,7]. The reason for this behavior is the fact that a considerable potential drop can be built up across the substrate (or well) resistance, between the drain and the substrate (well) contact, when a small substrate current is flowing through the device [8]. This positive substrate potential (for an n-channel device) gives rise to a lowering of the threshold voltage and, therefore, to a kink effect. The hysteresis or transient effect is related to the slow response of the dopants to a change in bias and hence in charge state [9]. While the capture process proceeds quite fast, this is not so for the re-emission of trapped charge. The net result is a retarded buildup (response) of the depletion region in the substrate, an effect which is also referred to as the forced depletion layer formation [6].

Enhancing the doping density of the p-well lowers the susceptibility to these effects and is therefore recommended for cryogenic CMOS technologies. In fact, increasing the well doping density goes along with the scaling trend, so that the kink effect should become less of a problem for deep submicron CMOS. In addition, the kink effect has been noted to reduce for shorter device lengths, for devices fabricated within the same technology [3].

The role of the V_T adjustment implantation has also been studied. However, omitting this ion implantation step enhances the V_T (and current) asymmetry of the n- and p-MOSFETs, which is not particularly desirable. Overall (with the present COTS philosophy in mind) it is better to stay as close as possible to the standard room temperature technology. Eliminating the LDD step in fact simplifies the process, giving the additional benefit of reducing the processing cost.

I.2 Impact on the Radiation Response

The radiation testing performed during the first phase of the project yielded some interesting trends. In summary, the non-LDD devices gave rise to a better radiation performance, so that this is again an argument in favor of skipping this process module. One of the effects observed was that the change in V_T at 4.2 K was 20 times smaller for non-LDD devices compared with their LDD counterparts [2].

Furthermore, the non-LDD p-MOSFETs showed a slight improvement of the I-V characteristics for low to moderate proton irradiation fluence, which was not observed for the LDD case. Previous studies also highlighted the extra device degradation associated with the series resistance of the LDD devices [10]. The main reason for this enhanced susceptibility to radiation is the presence of the spacer oxides on top of the LDDs, which are of inferior quality than that of the gate oxide. This is due to the fact that spacer oxides are not thermally grown but rather deposited. (Positive charging of the spacers causes a change in the surface potential and in the carrier density of the LDDs, leading to a change in R_s.

With respect to the well processing, one positive feature which came out of the study was the reduction of the drain current kink in saturation after exposure to both protons or γs [2],[11]. The kink reduction can be explained by the change in the 4.2 K substrate current characteristic observed after the exposures.

II. Design Considerations

There are a number of well established design techniques for improving the radiation hardness of CMOS technologies. These include the use of closed geometry devices or of guard rings. It has been demonstrated in the past that these techniques are also successful for low temperature operation [10],[12]. Maybe more specific for cryogenic electronics, is the use of cascode transistors. It is a transistor consisting of two parts in series with a common contact, preferably left floating. It helps in reducing the kink effect. This has for example been shown convincingly for partially depleted (PD) SOI transistors operating in the so-called twin-gate mode [13]. Not only the drain current kink is removed, but also the associated LF noise overshoot [14]. It has furthermore been demonstrated that the noise margins of SOI inverters improve drastically for twin-gate structures [15]. This design concept has a good potential for analogue applications.

III. Cryogenic Testing

The problems and pitfalls of cryogenic testing have been reviewed on a few occasions [1, 16]. Important factors to take into account are the occurrence of transient and hysteresis effects at low drain bias V_{ds}, the variable series resistance for the case of LDD type of devices, etc. Some rules of thumb are summarized in this section. They will be discussed for n-channel devices (positive sign of the biases, but the same ideas are basically valid for p-MOSFETs as well).

III.1 Pre-irradiation Testing

A first important type of measurement is the input or I_{ds}-V_{ds} measurement at a constant gate bias V_{gs}. This enables the extraction of key device parameters like V_T, the subthreshold swing S or the maximum transconductance g_{mmax}. A first important factor is the choice of V_{ds} in the linear region. In order for the physics and the ohmic equations to be applicable, the device has to be biased for a V_{ds} which is substantially smaller than the saturation value V_{dsat}. While at room temperature a typical value is 100 mV, this could be at the high (non-linear) side for 77 or 4.2 K operation. As a rule, one should compare the applied V_{ds} with the thermal voltage kT/q (q the elementary charge). Therefore, a value of 10 (maximum 25) mV seems to be more appropriate, for 4.2 K measurements. One drawback of using a small V_{ds} is that the drain current transients become longer that way [9], so that it may take some time before the device reaches equilibrium. The occurrence of transient effects can cause a change of V_T with time. One possibility is to cool down a biased device so that the steady state situation is frozen. However, changing the gate bias inevitably will break the steady state so that this is not really a solution. In order to average out the transient effects at 4.2 K, one can use a long integration time (parameter analyser). It is also recommended to repeat the same measurement a few times to check the stability/repeatability of the results. As a compromise, one can use a somewhat higher V_{ds} value compared with what would be ideal for true linear operation at 4.2 K, e.g. 10 or 25 mV.

However, for LDD devices, measurement at low V_{ds} can give rise to characteristics, which are dominated by the series resistance, so that the curves can not be used for a reliable parameter extraction [3]. One solution is to record an input curve at larger V_{ds}, say 1 V. It suffices to extrapolate $I_{ds}^{0.5}$ [5] to zero current in order to obtain the threshold voltage in this way. The drawback of this "saturation" method is that it only works if the V_T has no drain bias dependence. The selected V_{ds} should also be small enough to avoid the kink region. This implies large device lengths L. For shorter devices, drain induced barrier lowering (DIBL), punch-through, etc could cause the threshold voltage to change with drain bias, so that this "high V_{ds}" method becomes questionable.

It is clear from the above that automation of 4.2 K parameter extraction is not a simple task, even if it could be performed on wafer level, using a cooled wafer chuck.

A few words of comment should also be devoted to the different V_T extraction techniques commonly used [16]. Comparing the different popular techniques, it turns out that the so-called double-derivative method [17] offers the most robust solution at low temperatures. It can cope with a broad range of device architectures and measurement conditions [18]. It is furthermore quite insensitive to series resistance effects [16-17], which is particularly important for LDD type of devices. In the double derivative method, the second derivative of the drain current I_{ds} is plotted versus the gate bias (linear operation). The threshold voltage is defined as the gate bias where a peak occurs in the second derivative of the drain current.

With respect to the extraction of the subthreshold slope at cryogenic temperatures, one should first of all record the linear I_{ds}-V_{gs} characteristic with a sufficient number of data point (small enough δV_{gs} step). The step should in principle be smaller for lower temperatures (kT argument). However, for too small a step, the extraction of S may become unreliable, because of noise and instability problems

[19]. An optimum choice has to be made, as described elsewhere for Silicon-on-Insulator (SOI) FETs, operated at 77 K.

Numerous techniques to extract R_S and ΔL at 300 K have been proposed, which, however, fail when applied to 77 K for example [16]. This has several reasons. For example, the popular "shift and ratio" method assumes that R_S is gate voltage independent in first instance [20]. This assumption is generally not valid at cryogenic temperatures, where a more pronounced V_{gs} dependence is expected to occur. In addition, for LDD devices there can also be a marked drain bias dependence of the series resistance. In order to cope with these problems, dedicated techniques have been proposed (for an overview see e.g. [16]). One simple method only uses two transistors, instead of an array of several devices with constant width W [21]. It is shown to be applicable at 77 K to both bulk and SOI transistors, for not too small length. For the deep submicron case, a modified shift and ratio method has been proposed, again only using a long reference device and a short one, which is in principle useful down to the LHT range [22].

Most of the basic device parameters necessary to model the device performance are derived from an input curve. However, from the output (I_{ds}-V_{ds}) curves some additional parameters can be extracted, like the output conductance $g_d=dI_{ds}/dV_{ds}$ and, of course, kink and multiplication current related quantities. One important parameter typical for saturation is the drain voltage corresponding to the onset of pinch-off in the channel, namely V_{dsat}. In the past, a number of empirical techniques have been proposed to extract it, which are even applicable at cryogenic temperatures [23]. It basically consists of extrapolating the curves of constant multiplication factor $M=I_b/I_{ds}$ (I_b the substrate current) to zero drain current. The intercept with the V_{ds} axis gives a measure of V_{dsat}. However, it is not always easy to apply the method, especially when the device suffers from the kink effect. An interesting alternative is to use the onset of the kink (V_{kink}) for this purpose [11]. The kink onset is derived in practice from the output conductance, which will show the

start of an increase there. Output curves measured with a sufficiently small V_{ds} step are required in order to have an accurate V_{kink}.

A quadratic curve is fitted to the V_{kink} versus I_{kink} curve of Fig. 1, the intercept of which determines V_{dsat}. A basic assumption is that the onset of the kink occurs for the same multiplication factor at the different V_{gs} considered and that it can be approximated by a quadratic function of $1/(V_{ds}-V_{dsat})$. Using this method, reasonably consistent M values can be derived as shown by Fig. 2. More details will be published in a forthcoming paper [24].

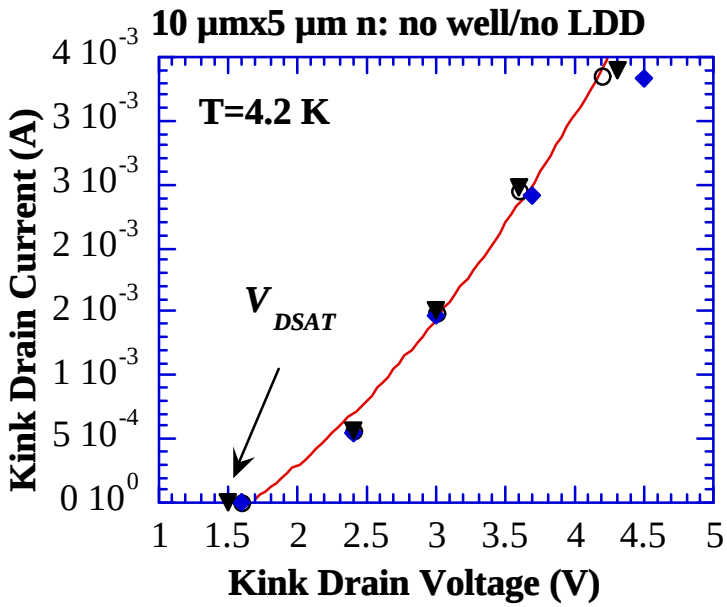

Fig. 1. Drain current at V_{gs}=1, 2, 3, 4 and 5 V corresponding with the onset drain voltage of the kink at 4.2 K. The data correspond with the following experimental conditions: pre-rad (o), after 50 krad γ's (diamonds) and after $5x10^{11}$ cm^{-2} H^+ (triangles).

III.2 Radiation Testing Aspects

With respect to the post irradiation testing, the above guidelines remain valid. In addition, it has been pointed out in Deliverable 1 [1] that for total-dose or ionisation damage the irradiation and subsequent testing is preferably done at the operation temperature. This is indirectly supported by the experimental results obtained in this study [2]: although the induced degradation was not very pronounced,

there are reasons to believe that some room temperature annealing has occurred. This can give rise to so-called radiation induced order effects, which correspond to an improvement of the device transport properties after low to moderate exposures. Also the reduction of the kink effect reported in [[11] can be understood along the same lines.

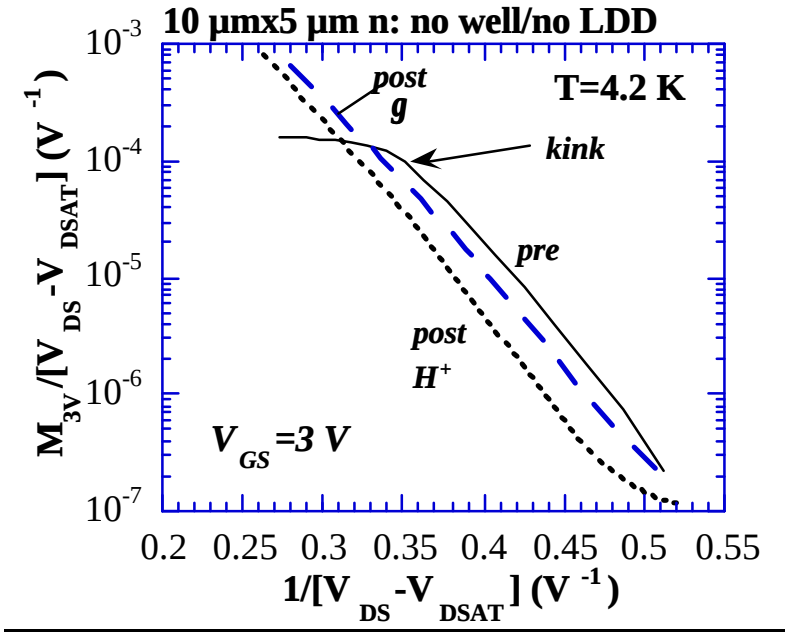

Fig. 2. Pre (full lines) and post (dashed lines) proton irradiation substrate current characteristics of a 10 µmx5 µm n-MOSFET at 4.2 K. The device has been exposed to a fluence of $5x10^{11}$ cm^{-2} 60 MeV protons.

IV. Conclusions

In summary, it can be stated that the development, design and characterization of space-born cryogenic electronics bring about specific problems, requiring a dedicated approach. Some guidelines have been formulated above, which in our view are recommended for achieving successful 4.2 K circuit development.

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