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Work Order 1938/96/NL/LB:

Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials

Radiation Damages Studies in Advanced Microelectronic Materials and Devices

Deliverable D5

E. Simoen, A. Poyai and C. Claeys

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Abstract

This report constitutes the Deliverable D5 of Work Order 1938/96/NL/NB on "Study of Radiation Effects in Cryogenic Electronics and Advanced Semiconductor Materials". It summarized the initial radiation experiments performed on n- and p-channel transistors processed in a 0.18 mm CMOS technology. In addition, the radiation hardness of a shallow Trench Isolation modules is studied, taking into account some technological parameters. The fact that some un-expected phenomena related to the shift in the electrical parameters of the devices are observed, necessitate additional irradiations and a more in-depth study. An interesting result is the device length dependence of the radiation hardness of deep submicron CMOS technologies.

Introduction

The second Activity of RFQ/3-8938/97/NL/NB concentrates on exploratory radiation damage studies in advanced semiconductor materials and devices which will become available for possible space applications in the coming 5 to 10 years. An overview of some of the future technologies of interest can be found in Deliverable D4 [1] and potential radiation issues have been pointed out there. Based on this literature study, it was decided to focus on the radiation damage in the 0.18 μ m CMOS technology, which is IMEC 's current workhorse technology. Also microelectronics industry is now moving towards this level of scaling.

In addition, p-n junction diodes surrounded by shallow-trench isolation (STI) have been included in the study for the following reason. STI will become the isolation technology of choice for future deep submicron CMOS technologies, replacing the standard LOCal Oxidation of Silicon (LOCOS) isolation schemes. Since there was not a mature STI module available at IMEC at the time of the development of the 0.18 µm CMOS, isolation was achieved by an aggressive Polysilicon Encapsulated LOCOS (PELOX) concept. However, the radiation testing of simple diode structures with STI will already reveal whether there are problems to be expected or not. At the same time, it is a simpler device structure, enabling a more fundamental study of the radiation effects. The separation of bulk, peripheral and corner leakage current components should help to elucidate the effect of both ionization and displacement damage. Furthermore, different processing splits for both STI and 0.18 µm CMOS batches are available, so that the impact of some process variables on the radiation response can be assessed. So far, it was decided to concentrate on high-energy proton and particle (electrons and neutron) irradiations, as in the literature, some information on total-dose can be found, while high energy proton data on advanced CMOS is lacking completely. Besides, this allows to study both the effects of ionisation and displacement damage, which is particularly interesting in the case of the diodes.

The report is organized as follows. Part I deals with the results of the radiation damage study in 0.18 µm CMOS, while part II focuses on the STI data. Each part contains 5 sections. In a first section, some technological details will be presented. Next, the irradiation and sample matrix will be described, followed by the pre- and post-irradiation characterization scheme. In a 4th section, the initial device characteristics will be briefly summarized and discussed, followed by the post irradiation results. The main conclusions and outlook will be summed up in a 5th section. The same structure applies for the STI part.

Finally, a general conclusion is drawn and some suggestions for next irradiation experiments are formulated. The Appendix lists detailed information on the individual devices and relevant remarks.

Part I: Radiation Study of 0.18 µm CMOS

I. 1. Technological details

Two wafers from lot PLINE 8008 have been selected for the radiation testing, namely Wafer 10 (w10) and Wafer 16 (w16). They belong, respectively, to a so-called n-MOSFET split (w16) and a p-MOSFET split (w10), corresponding as closely as possible to the targeted device performance (threshold voltage V_T, drive current, ...). Table I summarizes some of the relevant process information. In addition, it should be remarked that beside wet oxidized wafers, splits have been processed using an NO nitridation. These devices are interesting candidates for future irradiation tests, as NO oxidation is a good alternative to replace low temperature wet oxidation in the next technology generation. Expected benefits are a more reliable gate oxide, a higher resistance against boron penetration from the p⁺ polysilicon gate (p-MOSFET) and in the literature also a higher radiation tolerance has been quoted [1].

Table I: Relevant technological details for Wafer 10 (p) and 16 (n).

Gate oxide thickness (t _{ox})	3.5 nm
Gate oxidation	<u>wet@650</u> °C
Isolation	PELOX (400 nm)
p-well implantation	200 & 55 keV
n-well implantation	380 (P) & 120 keV (As)
n-LDD	w10 & w16
p-LDD	w16
Nitride spacer	80 nm (w10) & 95 nm (w16)
Silicidation	Ti/Co (8/15 nm)

I.2. Sample and radiation matrix

Radiation tests have been performed on 24 pins dual-in-line packaged transistors and ring oscillator circuits. Both L-arrays, containing short-channel n-and p-MOSFETs with a fixed width W=10 μ m (samples LA#) and W-arrays (length L=10 μ m; samples WA#) have been selected. The L-arrays contain transistors with a polysilicon gate length of L_{poly}=0.48, 0.38, 0.33, 0.28, 0.23, 0.205 and 0.18 μ m, respectively (both n- and p-channel devices). The designed (mask) length is in fact

approximately 0.02 μ m higher, because of patterning (i.e. lithography and etching). The W-array n- and p-MOSFETs are W=0.2, 0.225, 0.25, 0.275, 0.3, 0.325, 0.4 an 0.45 μ m wide.

In addition, polysilicon and metal Field-Isolation transistors have been packaged. However, after packaging no good characteristics were obtained so that it was decided not to expose these components. Meanwhile, it has become clear that the chosen test structures do not provide useful characteristics even on wafer level. However, other n-and p-type field-isolation transistors have been processed which yield normal I-V curves and which are candidates for future irradiation tests.

The ring oscillators (abbreviated RO#) have been designed at the CNET (France) and are based on 0.25 and 0.2 μ m designed length and a designed width of 0.8 μ m (n-MOSFET) and 1.6 μ m (p-MOSFET). The bonding pad configuration is given in Appendix I.

The irradiations were performed in Louvain-la-Neuve (Cyclone facility) on 24 November 1999 at a proton energy of 60 MeV. Two fluences are considered, namely $3x10^{10}$ cm⁻² and 10^{11} cm⁻². *No bias* has been applied to the devices. Irradiation was performed through the lid of the package.

60 MeV Proton Fluence (x10 ¹⁰ cm ⁻²)	Sample Matrix
3	LA16-1 LA10-1 WA10-2 RO10-1
10	LA10-2 LA10-3 RO10-2 WA10-4
10	RO10-3 RO10-4 RO10-5 RO16-1

Table II. Irradiation matrix for the 0.18 µm CMOS components.

I.3. Device characterisation

The following standard I-V characterization has been applied:

- Drain current (I_D) versus gate voltage (V_{GS}) @ constant drain bias $IV_{DS}I$ of 0.05 and 1 V
- Drain and substrate current (I_B) versus drain bias at different V_{GS} (output characteristics)

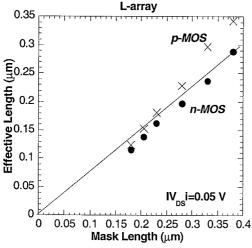
During the measurements, care was taken not to exceed a drain or gate bias of 2 V in absolute value. The nominal operation bias for this technology is 1.8 V. Above 2 V, it is expected that considerable hot-carrier degradation takes place in a short time, so it is better to avoid stressing the device during pre-rad and post-rad characterization.

From the curves in the ohmic regime, the threshold voltage V_T is derived using the linear extrapolation technique [2] at the point of maximum transconductance g_{mmax} . A 25 mV correction is applied to the extrapolated crossing point with the V_{GS} -axis in order to account for the $V_{DS}/2$ term. The threshold voltage for the ± 1 V input curve (n or p-MOSFET) is derived as follows: first the drain current corresponding to the extrapolated V_T is determined for the curve in the ohmic regime. Next, the gate bias corresponding with the same I_D , for the 1-V characteristic is obtained, which is considered as the $V_{T@1V}$. The difference between the two thresholds is considered a measure for the short-channel effect, which can be ascribed to the drain-induced barrier lowering (DIBL).

From the subthreshold regime, the subthreshold swing S is derived (in mV/decade), using the exponential low-V_{GS} part of the curve.

Two other important parameters, which can be derived from the measurements in linear operation on the L-array transistors are the series resistance R_s and the effective (metallurgical or electrical) device length L_{eff} , which differs from the technological gate length $L_{poly}.$ For deep submicron transistors, it is not straightforward to derive these parameters. There are many methods available in the literature [2] and each technique has its limited application range. Generally, more refined methods are necessary for next generation of devices. However, the most popular methods used today are a variant of the well-known shift and ratio (S&R) method [3]. A modified S&R method has also been applied to the L-array transistors of Wafer 10 and 16, yielding an average ΔL of 0.07 μm for the n- and of 0.05 μm for the p-MOSFETs [4]. The analysis was performed using a long (5 μm) reference transistor with the same width, from a neighboring long-channel L-array. The extracted effective length and series resistances of the devices are shown in Figs I.1 and I.2, respectively. The effective lengths versus the nominal length are also represented in Table III, allowing an easy conversion if necessary.

As can be seen from Fig. I.1, the result of the extraction is better for the n-MOSFETs compared with the p-channels (the lengths are better 'aligned' with the origin). This is probably connected with the stronger dependence of the series resistance on the gate length, shown in Fig. I.2. It should finally be noted that the series resistance is generally a function of the gate overdrive voltage. Quite often a linear decrease with increasing gate overdrive voltage $1/(V_{GS}-V_T)$ is found [5]-[6]. This probably explains the higher R_S values for the shorter p-MOS device lengths observed in Fig. I.2.



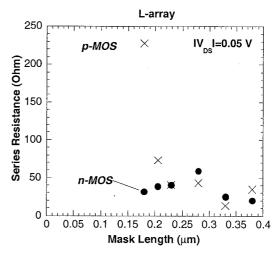


Fig. I.1. Effective length versus the polysilicon gate length of the $0.18~\mu m$ CMOS n- and p-channel transistors.

Fig. I.2. Series resistance versus the polysilicon gate length of the 0.18 μm CMOS n- and p-channel transistors.

Table III. Effective length of the n-(Wafer 16) and p-channel transistors (Wafer 10) extracted from an L-array, using a modified shift and ratio method.

L _{poly}	L _{effn}	L _{effp}
(μm)	(μm)	(μm)
0.18	0.116	0.124
0.205	0.138	0.153
0.22	0.162	0.181
0.28	0.197	0.229
0.33	0.237	0.297
0.38	0.288	0.342
0.48	0.388	0.442

I.4 Pre-rad characteristics

Pre-rad characterization has been performed for the available lengths on the mounted devices (Table III), both for the n-and p-MOSFETs of Wafer 10 and 16. This allows to study the length dependence of the main device parameters and to investigate so-called short-channel effects. First, the measured input curves will be briefly discussed, followed by a summary of the static parameters (V_T , the drain-induced barrier lowering ΔV_T , the g_{mmax} and the subthreshold swing S).

As can be seen from Figs I.3 to I.10, acceptable input curves have been obtained down to the 0.18 µm nominal device. The measured gate leakage current before irradiation is low and of the order of pA. The subthreshold leakage current is small. It

is clear from Fig. I.3 for example that there is a short-channel effect on the V_T , while the DIBL is also much more pronounced for the 0.18 μ m transistor.

Comparing the n-MOSFETs of Wafer 10 (Fig. I.3) and 16 (Fig. I.5), one can conclude that the threshold voltage is higher for the targeted process conditions (on the average 0.45~V for the 'long'-channels) than for the non-optimised Wafer 10 devices (0.35~V). This can be derived also from Fig. I.11. The V_T roll-off with shorter length is more pronounced for Wafer 16. On the other hand, the DIBL effect is very similar (Fig. I.13).

The targeted p-MOSFETs of Wafer 10 have a long-channel V_T of -0.2 V (Fig. I.12) which is larger than the -0.45 V for Wafer I.16. Both the V_T roll off and the DIBL is much stronger for the target condition (Fig. I.14), which is related to the different well and extension dopant profiles in/below the channel region.

The maximum transconductance is higher for the Wafer 10 MOSFETs (Fig. I.15 and I.16), both for the n- and the p-channels. There the g_{mmax} is plotted versus the reciprocal effective length. If the ΔL is properly extracted, it is expected that g_{mmax} follows exactly $1/L_{eff}$. In case of the n-MOSFETs, Wafer 10 follows more closely the theoretical behaviour. Both types of p-MOSFETs are reasonably well described by the model according to the data of Fig. I.16.

Finally, Fig. I.17 represents the subthreshold swing of the n-MOSFETs versus the effective device length. The usual short-channel increase of the swing is observed. The best values are obtained for Wafer 10, pointing to a lower depletion layer charge. This is in line with the lower threshold voltage. It was difficult to derive a unique swing for the Wafer 10 p-MOSFETs, while Wafer 16 yields a length-independent S of 82 mV/decade.

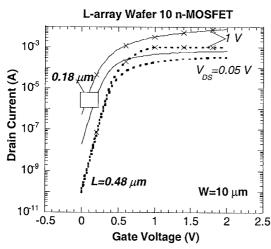


Fig. I.3. Input curves at V_{DS} =0.05 and 1 V for a 0.48 and a 0.18 μ m n-MOSFET of Wafer 10.

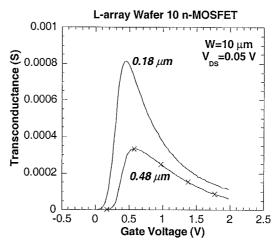


Fig. I.4. Transconductance at V_{DS} =0.05 for a 0.48 and a 0.18 μm n-MOSFET of Wafer 10.

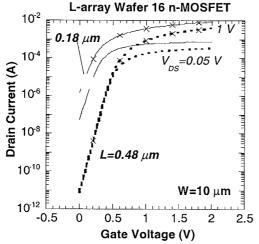


Fig. I.5. Input curves at V_{DS} =0.05 and 1 V for a 0.48 and a 0.18 μm n-MOSFET of Wafer 16.

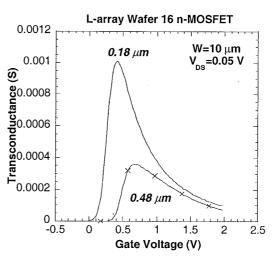


Fig. I.6. Transconductance at V_{DS} =0.05 for a 0.48 and a 0.18 μm n-MOSFET of Wafer 16.

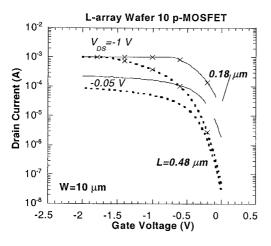


Fig. I.7. Input curves at V_{DS} =-0.05 and -1 V for a 0.48 and a 0.18 μm p-MOSFET of Wafer 10.

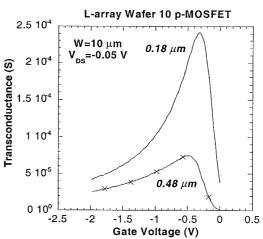


Fig. I.8. Transconductance at V_{DS} =-0.05 for a 0.48 and a 0.18 μm p-MOSFET of Wafer 10.

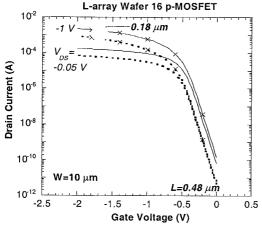


Fig. I.9. Input curves at V_{DS} =-0.05 and - 1 V for a 0.48 and a 0.18 μm p-MOSFET of Wafer 16.

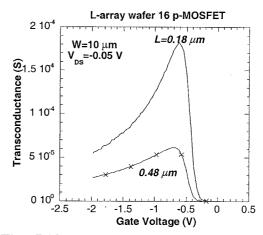


Fig. I.10. Transconductance at V_{DS} =-0.05 for a 0.48 and a 0.18 μm p-MOSFET of Wafer 16.

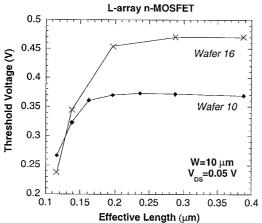


Fig. I.11. Threshold voltage versus the effective length for the n-MOSFETs.

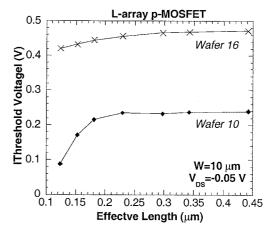


Fig. I.12. Threshold voltage versus the effective length for the p-MOSFETs.

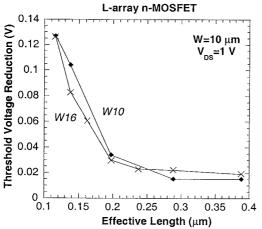


Fig. I.13. Threshold voltage shift versus the effective length for n-MOSFETs.

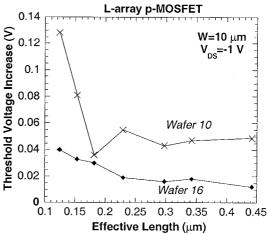


Fig. I.14. Threshold voltage shift versus the effective length for p-MOSFETs.

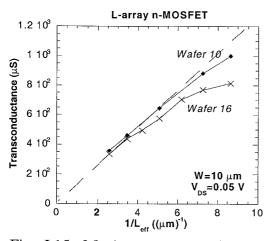


Fig. I.15. Maximum transconductance versus the effective length for the n-MOSFETs.

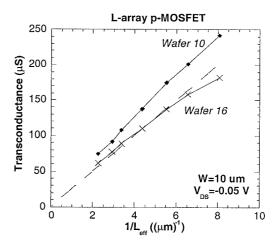


Fig. I.16. Maximum transconductance versus the effective length for the n-MOSFETs.

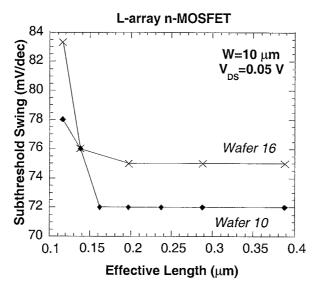


Fig. I.17. Subthreshold swing of wafer 10 and 16 n-MOSFETs before irradiation.

I.5. Post-rad characteristics

The different characteristics of a 60 MeV proton irradiated Wafer 10 n-MOSFET are represented in Figs I.18 to I.25 and this, respectively, for a short- (Figs I.18,20,22,24) and a long-channel transistor (Figs I.19,21,23 and 25). Comparing the input curves for the L=0.18 (Fig. I.18) and 0.48 µm (Fig. I.19) devices, it is clear that the short transistor shows little degradation, up to a fluence of 10¹¹ cm⁻², while a clear reduction of the current is observed for the long-channel case. This is more clearly evidenced by the transconductance shown in Figs I.20 and I.21. This leads us to the conclusion that there seems to be a kind of short-channel effect on the radiation damage response, whereby the short-channel characteristics are less degraded for the proton fluence range studied. Such type of behaviour has been noted before [1] and could be explained by considering the charge-sharing concept (in case of total-dose ionisation damage!) [7]. This will be discussed in more detail when the changes in the static device characteristics are discussed. However, it should be remarked that normally, both the drain current and transconductance of an n-MOSFET increase after exposure to ionisation damage (see e.g. the results for the 0.5 µm transistors [8]), while here a reduction is seen. It is clear that the degradation mechanism is different here (displacement damage?) or, alternatively, is not homogeneous along the channel, whereby damage preferentially occurs at the extensions of the devices for example [1].

Beside the direction (sign) of the changes, also its evolution with fluence Φ is rather peculiar and depends on the channel length. While there is a continuous reduction of g_m with increasing fluence for the short-channel transistor, a kind of rebound is found for the 0.48 μ m device. As will be demonstrated, this behaviour appears in the threshold voltage as well, suggesting a length-dependence of the ionisation damage in the gate oxide. It should be remarked here that while the gate leakage current was acceptable after a fluence of $3x10^{10}$ cm⁻², a rather high I_G (> I_D !) was generally found for the highest fluence. In some cases, anomalous I-V characteristics were obtained, rendering the devices useless for further analysis (see also Appendix II).

The same type of behaviour is reflected in the output curves:

- a larger degradation for the long-channel n-MOS transistor at $3x10^{10}$ cm⁻²
- a rebound behaviour for the long-channel transistor at 10¹¹ cm⁻², which is absent for the 0.18 µm device

The substrate current (I_B) shows a reduction after irradiation for sufficient drain bias. This points to a lowering of the probability for band-to-band impact ionisation near the drain, similar as reported in Ref 9. At low V_{DS} , a substantial leakage current is observed, which increases with fluence.

The p-channel devices of Wafer 10 show a degradation of the characteristics, which is more in line with the expectations (Figs. I.26 to I.33). However, there is again a tendency for larger current reduction for the longer transistors (compare e.g. Figs. I.30 and I.31). In addition, noticeable changes are found only after the 10¹¹ cm⁻² irradiation.

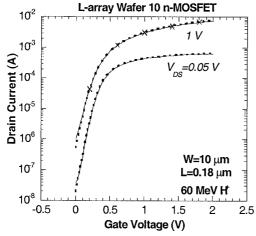


Fig. I.18. Input curves at V_{DS} =0.05 and 1 V for an irradiated W10 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

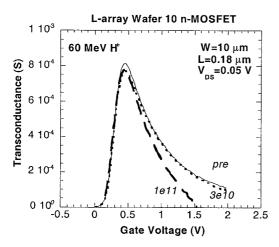


Fig. I.20. Transconductance at V_{DS} =0.05 for an irradiated W10 n-MOSFET before (full) and after a $3x10^{10}$ cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.18 μ m.

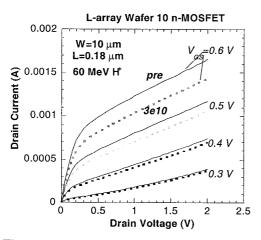


Fig. I.22. Output curves for an irradiated W10 n-MOSFET before (full) and after (dotted) a 3×10^{10} cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

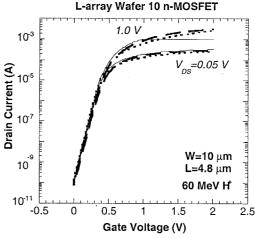


Fig. I.19. Input curves at V_{DS} =0.05 and 1 V for an irradiated W10 n-MOSFET before (full) and after a $3x10^{10}$ cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

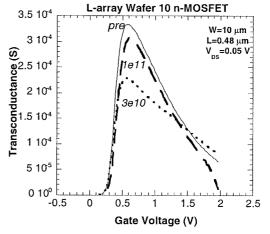


Fig. I.21 Transconductance at V_{DS} =0.05 for an irradiated W 10 n-MOSFET, before (full) and after (dotted) a 3×10^{10} cm⁻² or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

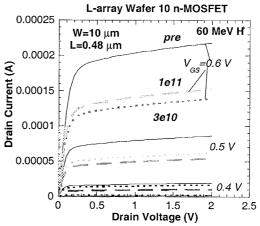


Fig. I.23. Output curves for an irradiated W 10 n-MOSFET before (full) and after a $3x10^{10}$ cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

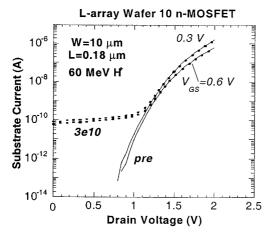


Fig. I.24. I_B curves at different V_{GS} for an irradiated W10 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

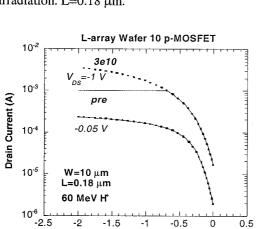


Fig. I.26. Input curves at V_{DS} =-0.05 and -1 V for an irradiated W10 p-MOSFET, before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

Gate Voltage (V)

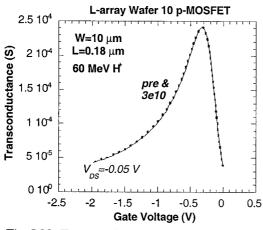


Fig. I.28. Transconductance at V_{DS} =-0.05 for an irradiated W10 p-MOSFET, before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

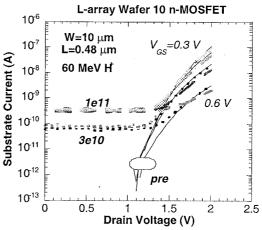


Fig. I.25. I_B curves at different V_{GS} for an irradiated W10 n-MOSFET before (full) and after a 3×10^{10} cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

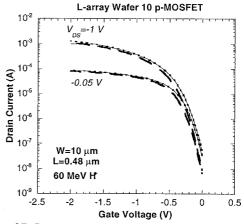


Fig. 27. Input curves at V_{DS} =-0.05 and -1 V for an irradiated W10 p-MOSFET before (full) and after a 3×10^{10} cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

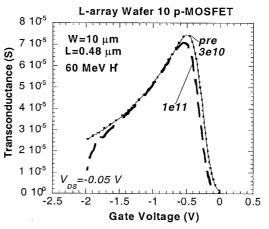


Fig. I.29. Transconductance at V_{DS} =-0.05 for an irradiated W10 p-MOSFET, before (full) and after a $3x10^{10}~cm^{-2}$ (dotted) or $10^{11}~cm^{-2}$ (dash) 60 MeV H⁺ irradiation. L=0.48 μm .

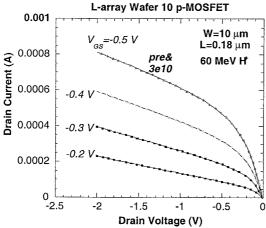


Fig. I.30. Output curves for an irradiated W10 p-MOSFET before (full) and after (dotted) a 3×10^{10} cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

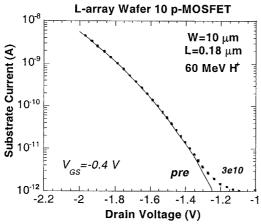


Fig. I.32. I_B curves at different V_{GS} for an irradiated W10 p-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.18 μ m.

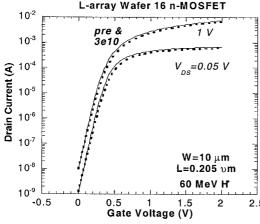


Fig. I.34. Input curves at V_{DS} =0.05 and 1 V for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.205 μ m.

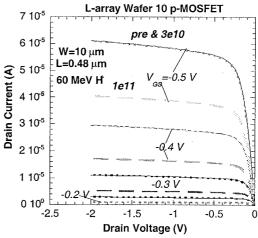


Fig. I.31. Output curves for an irradiated W10 p-MOSFET before (full) and after a $3x10^{10}$ cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

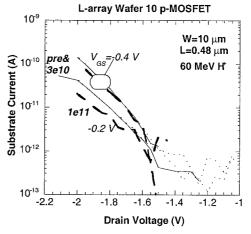


Fig. I.33. I_B curves at different V_{GS} for an irradiated W 10 p-MOSFET before (full) and after a $3x10^{10}$ cm⁻² (dotted) or 10^{11} cm⁻² (dash) 60 MeV proton irradiation. L=0.48 μ m.

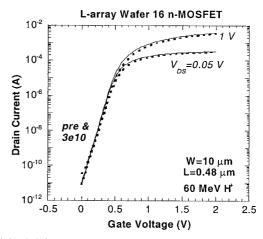


Fig. I.35. Input curves at V_{DS} =0.05 and 1 V for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.48 μ m.

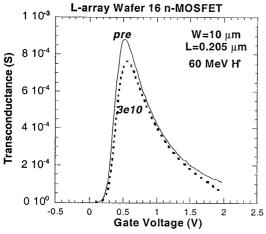


Fig. I.36. Transconductance at V_{DS} =0.05 for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.205 μm .

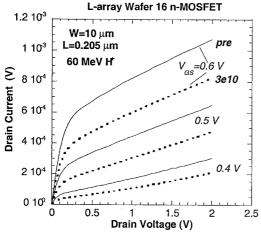


Fig. I.38. Output curves for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}\,\text{cm}^{-2}$ 60 MeV proton irradiation. L=0.205 μm .

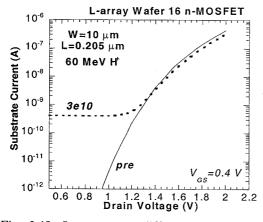


Fig. I.40. I_B curves at different V_{GS} for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.205 μm .

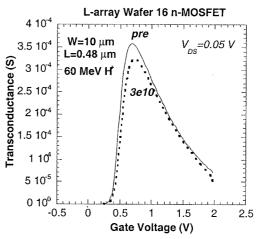


Fig. I.37. Transconductance at V_{DS} =0.05 and 1 V for an irradiated W16 n-MOSFET before (full) and after (dotted) a 3×10^{10} cm⁻² 60 MeV proton irradiation. L=0.48 μ m.

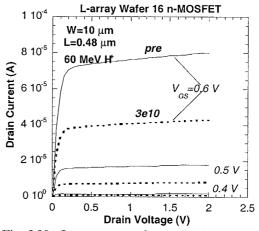


Fig. I.39. Output curves for an irradiated W16 n-MOSFET before (full) and after (dotted) a 3×10^{10} cm⁻² 60 MeV proton irradiation. L=0.48 μ m.

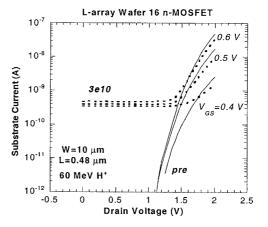


Fig. I.41. I_B curves at different V_{GS} for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.48 μ m.

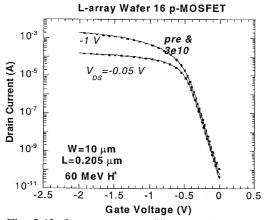


Fig. I.42. Input curves at V_{DS} =-0.05 and -1 V for an irradiated W16 p-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.205 μm .

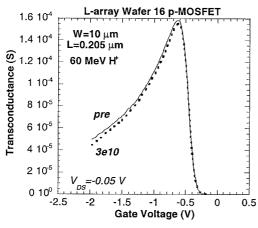


Fig. I.44. Transconductance at V_{DS} =-0.05 for an irradiated W16 p-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.205 μm .

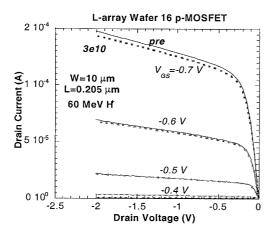


Fig. I.46. Output curves for an irradiated W16 p-MOSFET before (full) and after (dotted) a 3×10^{10} cm⁻² 60 MeV proton irradiation. L=0.205 μ m.

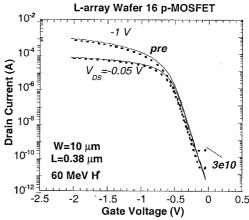


Fig. I.43. Input curves at V_{DS} =0.05 and 1 V for an irradiated W16 p-MOSFET before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.38 μ m.

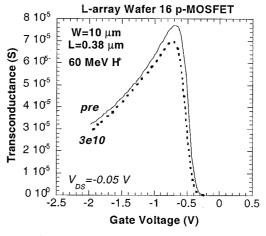


Fig. I.45. Transconductance at V_{DS} =-0.05 for an irradiated W16 p-MOSFET, before (full) and after (dotted) a $3x10^{10}$ cm⁻² 60 MeV proton irradiation. L=0.48 μ m.

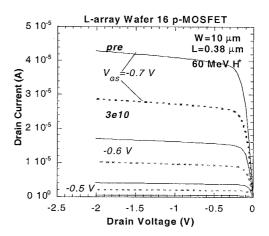
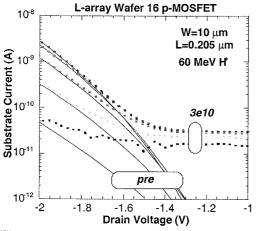
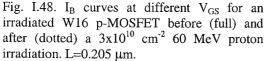


Fig. I.47. Output curves for an irradiated W16 n-MOSFET before (full) and after (dotted) a $3x10^{10}~\text{cm}^{-2}$ 60 MeV proton irradiation. L=0.38 μm .





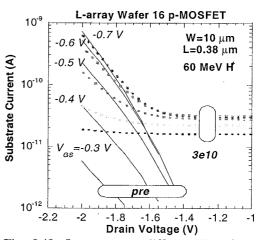


Fig. I.49. I_B curves at different V_{GS} for an irradiated W16 p-MOSFET before (full) and after (dotted) a $3x10^{10}~\text{cm}^{-2}$ 60 MeV proton irradiation. L=0.38 μm .

Grosso modo similar results have been obtained for the Wafer 16 n and p-channel devices (see Figs. I.34 through I. I.49), except for the rebound at 10¹¹ cm⁻², since no data were available at this fluence (see Table II).

The 60 MeV proton-irradiation induced change in the static device parameters is summarised in Figs. I.50 to I.64. As can be noted in Fig. I.50, the threshold voltage of the Wafer 10 n-MOSFETs shows a reduction for the longer channel lengths at a Φ =3x10¹⁰ cm⁻², while a marginal change is found for the short lengths. For the larger fluence, a rebound of the V_T is observed for the longer channels, while the shortest channel shows a reduction of V_T. This V_T increase for the long channels is rather unusual since one normally expects a reduction after the creation of positive charge in the gate oxide. This needs further studies in order to understand the cross-over behavior. It appears as if two competing damage mechanisms are operating, one which dominates for the long and the other for the short transistors.

In case of Wafer 16 and Φ =3x10¹⁰ cm⁻², the same V_T cross-over behavior as for Wafer 10 at 10^{11} cm⁻² is observed in Fig. I.51: while the short devices show a lowering of the threshold voltage, an increase is found for the longer transistors. Apparently, there seems to be an optimal length around 0.23 μ m which is rather insensitive to the radiation damage. This length shifts to lower values for a larger proton fluence and probably also for Wafer 10 compared to 16. At first sight, the Wafer 10 devices are more hard than Wafer 16, from a perspective of V_T change.

The V_{TS} of the p-MOSFETs are represented in Figs. I.52 and I.53, showing little changes in both cases after $3x10^{10}~\text{cm}^{-2}$ and a marked increase after $10^{11}~\text{cm}^{-2}$ for the Wafer 10 p-MOSFETs. In the latter case, the increase in absolute value of V_{T} again appears to be somewhat larger for the longer channels compared with the shortest L_{eff} in Fig. I.52.

With respect to the short-channel DIBL effect on the V_T , there seems to be little impact of a $3x10^{10}$ cm⁻² proton irradiation for the n-channel devices (Fig. I.54 and I.55). There is maybe a slight enhancement for the case of the long-channel Wafer 16 devices. The Wafer 10 p-MOSFETs also show little changes in ΔV_T in Fig. I.56, while it becomes length-independent for Wafer 16 after $3x10^{10}$ cm⁻² (Fig. I.57).

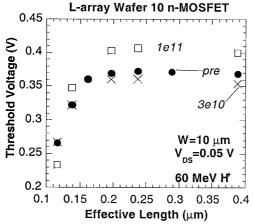


Fig. I.50. Threshold voltage vs effective length for the Wafer 10 n-MOSFETs before and after a 60 MeV proton irradiation.

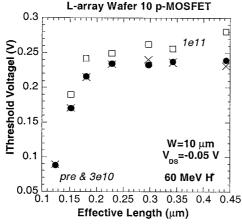


Fig. I.52. Threshold voltage vs effective length for the Wafer 10 p-MOSFETs before and after a 60 MeV proton irradiation.

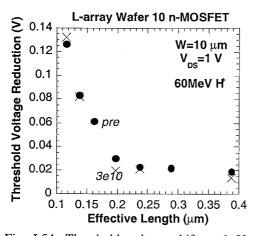


Fig. I.54. Threshold voltage shift at 1 V vs effective length for the Wafer 10 n-MOSFETs before and after a 60 MeV proton irradiation.

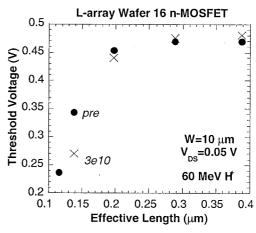


Fig. I.51. Threshold voltage vs effective length for the Wafer 16 n-MOSFETs before and after a 60 MeV proton irradiation.

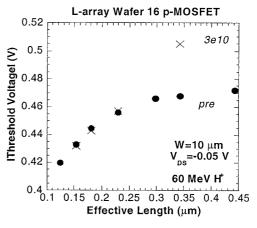


Fig. I.53. Threshold voltage vs effective length for the Wafer 16 p-MOSFETs before and after a 60 MeV proton irradiation.

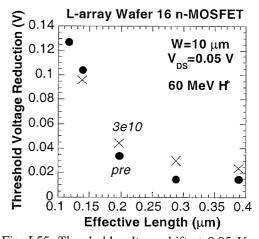


Fig. I.55. Threshold voltage shift at 0.05 V vs effective length for the Wafer 16 n-MOSFETs before and after a 60 MeV proton irradiation.

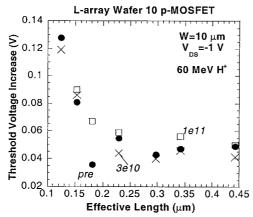


Fig. I.56. Threshold voltage increase at -1 V vs effective length for the Wafer 10 p-MOSFETs before and after a 60 MeV proton irradiation.

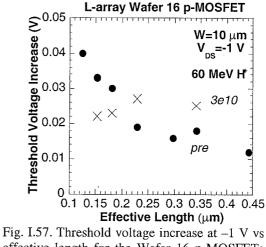


Fig. I.57. Threshold voltage increase at -1 V vs effective length for the Wafer 16 p-MOSFETs before and after a 60 MeV proton irradiation.

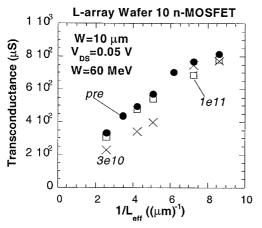


Fig. I.58. Transconductance vs effective length for the Wafer 10 n-MOSFETs before and after a 60 MeV proton irradiation.

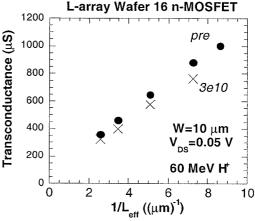


Fig. I.59. Transconductance vs effective length for the Wafer 16 n-MOSFETs before and after a 60 MeV proton irradiation.

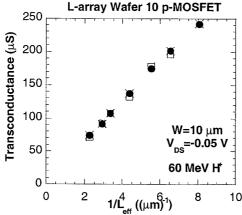


Fig. I.60. Transconductance vs effective length for the Wafer 10 p-MOSFETs before and after a 60 MeV proton irradiation.

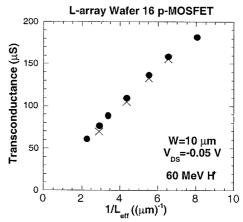


Fig. I.61. Transconductance vs effective length for the Wafer 16 p-MOSFETs before and after a 60 MeV proton irradiation.

The transconductance of the n-MOSFETs mirrors largely the changes of the threshold voltage (see Figs. I.58 to I.61). In other words the following trends are noted:

- A lowering of g_{mmax} is found for the n-MOSFETs, while the p-MOSFETs hardly show any change.
- A rebound after 10¹¹ cm⁻² exposure for the Wafer 10 n-MOSFETs, however, no cross-over seen for this parameter.
- There is no clear length dependence of the degradation for the transconductance.

Finally, the subthreshold swing before and after exposure is shown in Figs. I.62 to I.64. In all cases, an increase of S is observed. For the Wafer 10 devices there is a kind of cross-over behaviour between the 3×10^{10} cm⁻² and the 10^{11} cm⁻² data points in Fig. I.62. It appears that while the S was strongly increasing with shorter L_{eff}, this is no longer the case after a 10^{11} cm⁻² proton exposure. The Wafer 16 n-MOSFETs, show a bigger increase of S for the 3×10^{10} cm⁻² fluence, compared with Wafer 10. For the Wafer 16 p-MOSFETs, a constant increase of S is seen in Fig. I.64, which remains constant with L_{eff} after irradiation.

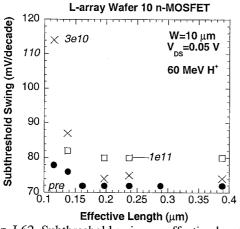


Fig. I.62. Subthreshold swing vs effective length for the Wafer 10 n-MOSFETs before and after a 60 MeV proton irradiation.

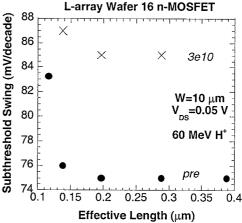


Fig. I.63. Subthreshold swing vs effective length for the Wafer 16 n-MOSFETs before and after a 60 MeV proton irradiation.

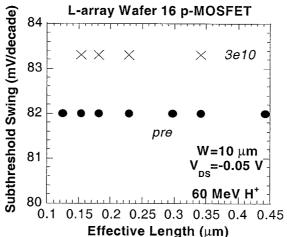


Fig. I.64. Subthreshold swing vs effective length for the Wafer 16 p-MOSFETs before and after 60 MeV proton irradiation.

It should finally be noted that so far, no ring-oscillator measurements have been performed. They are scheduled for the final part of the project. Given the slight reduction of g_{mmax} and drive current, a more or less slight increase of the gate delay time is expected after proton irradiation.

I.6. Conclusions and Outlook

From these initial 60 MeV proton irradiation studies of $0.18~\mu m$ CMOS transistors the following general conclusions can be drawn.

- A few unusual changes have been observed particularly with respect to the current and transconductance *reduction* of the n-channel devices.
- There appears to be a short-channel effect on the radiation response, whereby the longer channel transistors overall suffer more than the short-channels. This leads to rebound and cross-over effects for certain static device parameters.
- Based on this, it can be concluded that for the n-channel devices, there exists an intermediate optimum length, which is more or less insensitive to the radiation damage mechanisms. This optimum L_{eff} depends on the proton fluence and on the technological split, i.e. the extension and p-well profile.
- Physically speaking, this length dependence can only be explained by assuming at least two opposite degradation mechanism to be operating in the n-MOSFETs. Whether it is ionisation and displacement damage which are in the balance, or it is an inhomogeneous degradation along the channel has to be clarified by further experiments.

Giving these exciting and original results, it is clear that in a following experiment(s) they should be reproduced. In addition, it seems worthwhile to compare the degradation of wet-oxide devices with NO oxidized wafers. It is also considered to include in a next round PELOX field transistors, in order to clarify their role in the observed radiation response. This should be compared with the results obtained on the STI diodes, reported in the second part.

Part II. Impact of High Energy Particle Irradiation on STI diodes

II.1. STI diodes: technological details

Shallow Trench Isolation (STI) offers some unique features which makes it very suitable for scaling CMOS to the deep submicron regime. STI consists basically of the following steps: first, a shallow trench is dry-etched in the silicon substrate, surrounding the device active regions. The sidewalls of the trench are next oxidized and finally filled with a deposited oxide (TEOS). A schematic representation of an STI isolated diode is given in Fig. II.1.

The advantages of STI compared with LOCOS-type of isolation are the following: a bird's beak free device isolation is achieved, as shown in Fig. II.1, which allows a higher packing density of the active devices. In addition, STI facilitates planarisation by CMP (Chemical Mechanical Polishing) which is very important for deep submicron lithography.

The devices studied belong to the different splits of PLINE 980312 and are described in Fig. II.2. Both mounted and non-mounted diodes of wafers 3,6,9,12 and 14 have been irradiated. The main differences in the splits relate to the removal of the back-side layer or not, before CMP and to the thickness of the nitride and TEOS layers (Fig. II.2). As will be shown, there are no marked differences in the forward or reverse I-V of the different STI diodes before irradiation. It is important to remark that the n⁺p junctions have been processed in the retrograde p-well (double B implantation) which is also used for 0.18 µm CMOS (see part I), by As ion implantation. The resulting junction depth is in the range of 0.17 µm. Finally, Co/Ti (20/10 nm) silicidation is applied for contacting the active region.

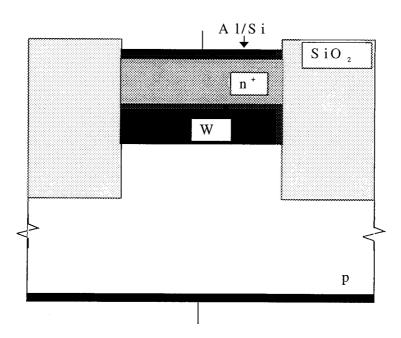


Fig. II.1. Schematically representation of a n⁺p junction surrounded by STI isolation. W is the width of the depletion region in the p-type substrate.

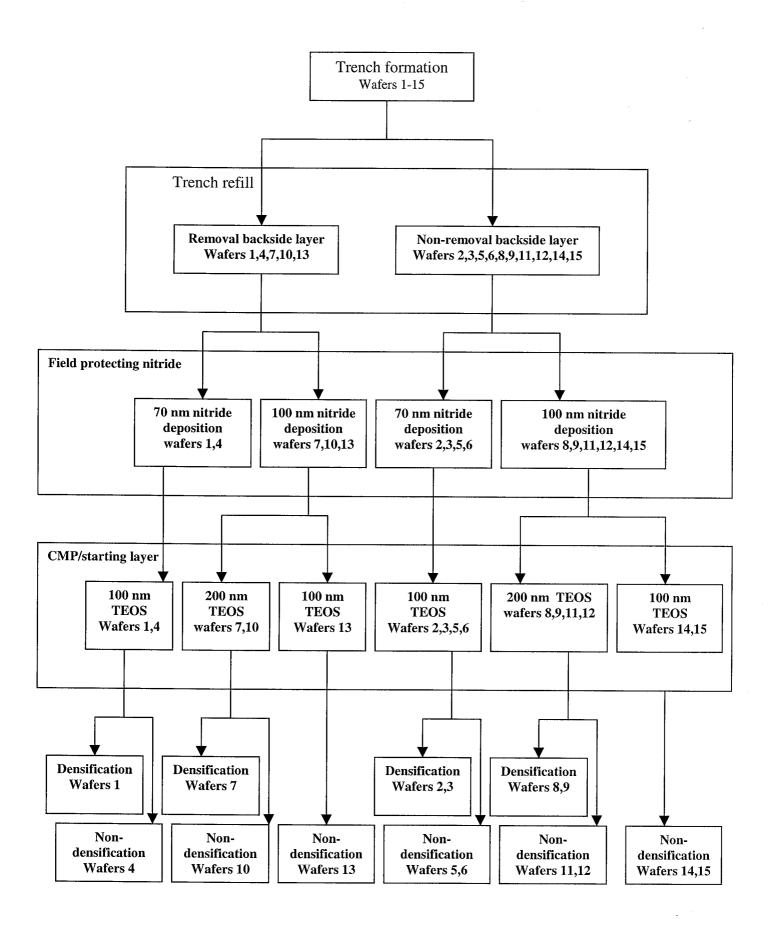


Fig. II.2. Process flow of PLINE 980312, illustrating the different splits studied.

II.2. Sample description, characterisation and radiation matrix

In order to study the different geometrical current components, diodes with different geometry have been studied. The area (A), the perimeter (P) and the number of corners (N_C) of the test structure are summarized in Table IV. Beside rectangular ("square" SQ) diodes also meander (ME) or perimeter diodes have been included in the study. Combining a number of SQ and ME diodes allows to separate the volume or bulk current density J_A (A/cm²) which scales with the diode area, from the perimeter density J_P (A/cm), assumed proportional with P. In principle, also a corner component J_C (A/corner) can be separated. Especially for STI down-scaled source and drain junction diodes, the perimeter and corner contributions become more and more important, due to the increased P/A ratio and are, therefore, worthwhile analyzing.

From a radiation damage viewpoint, the separation of J_A from J_P allows to distinguish the impact of non-ionising displacement damage and ionisation damage. Indeed, the lattice damage will only influence the generation/recombination lifetime in the bulk depletion region, yielding an increase of J_A with fluence Φ , while ionisation damage in the STI isolation will be the dominant degradation mechanism of J_P .

The separation of the geometrical current components is based on the assumption that the total reverse current density J_R is a linear combination of the different components, given by [10]-[11]:

$$J_R = A J_A + P J_P + N_C J_C + J_{par}$$
 (1)

As is seen from Eq. (1), at least 4 different geometry diodes have to be measured to separate the different components. J_{par} represents a parasitic sample-independent system leakage. In principle, the same separation scheme can be applied for the forward current density J_F or for the junction capacitance [10].

Table IV. Description of the diode geometry used in the analysis of the different components.

Diode Label	A (cm ²)	P (cm)	$N_{\rm C}$
SQ1 SQ2 SQ3 ME1 ME2 ME3 ME4	0.1 0.001 0.000064 0.001 0.001 0.001	1.3 0.13 0.032 8.04 2.04 1.04 0.54	4 4 4 320 80 40 20

In order to identify the dominant physical current mechanism, it is often useful to perform measurements as a function of the temperature T. This is based on the fact that the reverse diode current either shows a dependence of the form [11]:

$$J_R \sim T^3 \exp(-E_G/kT) \tag{2}$$

or:
$$J_R \sim T^{1.7} \exp(-E_T/kT)$$
 (3)

with E_G =1.12 eV the band-gap energy of silicon, k Boltzmann's constant and E_T the activation energy of the dominant generation-recombination level. Equation (2) is indicative of a dominant diffusion current mechanism and generally prevails at higher temperatures (i.e. >50 °C). This diffusion current component is normally determined by the diffusion length and by the recombination lifetime τ_r in the lower doped region of a p-n junction.

When the reverse (or forward current) is dominated by trap-assisted generation (recombination) in the depletion region of the diode, an activation energy E_T is derived which is frequently close to the mid gap value of 0.56 eV for the volume leakage current. This corresponds with the most efficient electron-hole generation centres, provided the corresponding capture cross sections are not too different. The generation current generally dominates at lower temperatures, given the lower activation energy (e.g. compare Eqs (2) and (3)) and is a reciprocal function of the generation lifetime τ_g . The relationship between the two lifetimes can be approximated by [12]:

$$\tau_{g} = \tau_{r} \exp(IE_{T}-E_{i}I/kT) \tag{4}$$

with E_i the intrinsic Fermi level (~0.56 eV). It is clear from Eq. (4) that if the trap level is not at mid gap, the generation lifetime is (much) larger than the minority carrier recombination lifetime [12]. On the other hand, the peripheral component J_P usually yields E_T values in the range of 0.7 eV, which is typical of Si-SiO₂ interface state generation [13]-[14]. It should finally be remarked that the activation energy can depend on the reverse bias, i.e., on the maximum field at the junction [10], which should be taken into account when comparing the obtained energy level with data derived from other techniques like Deep Level Transient Spectroscopy (DLTS). As will be shown, for the STI diodes fabricated in the highly doped p-well (~2x10¹⁷cm⁻³), field-enhancement of the carrier generation through Poole-Frenkel or tunneling effects will reduce the activation energy.

The temperature exponents in Eqs (2) and (3) stem from the temperature dependence of both fundamental and material parameters [15]. However, especially for the generation current (Eq. (3)), the exponent 1.7 can be over- or underestimating its true value, as discussed in Ref. 16.

Another way to separate the different physical components is to combine the I-V and the capacitance-voltage (C-V) characteristics of the same diode, as outlined elsewhere [10]-[11]. It is based on an original separation scheme proposed by Murakami et al. [17]. An example of this procedure is given in Fig. II.3.a for a non pwell, LOCOS isolated diode. As can be seen from the figure, in good approximation a linear increase of J_A with W can be observed. Fitting a straight line yields the diffusion current density as the intercept, while the slope is proportional to $J_{\rm gen}$. However, no linear dependence is observed for the STI diodes with p-well in Fig. II.3.b, due to the strong field dependence of the reverse current. The straight-line fitting technique is, therefore, not applicable in this case. At the moment, work is going on alternative approaches to achieve a physically based extraction of the recombination and generation lifetime for the STI diodes. This work is in progress and the outcome will be used for the analysis of the results after irradiation, whenever

available. In fact, it turns out that also the separation of the geometrical components is not straightforward for the STI diodes and requires a fine-tuning of the existing methods and/or an alternative layout of the diode test structures.

The C-V measurements at 100 kHz are used to assess the free carrier profile in the subtstrate before and after irradiation. The capacitance of the large area SQ1 diodes is corrected for perimeter contributions, similar as for the diode current, based on Eq. (1). Also temperature dependent measurements have been performed yielding no important variations up to 120°C.

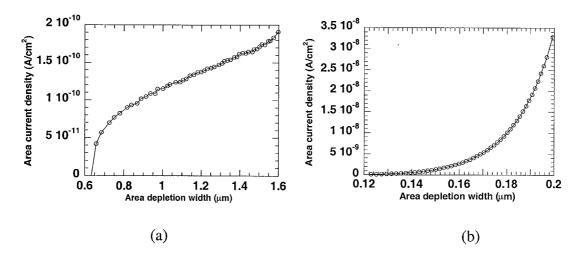


Fig. II.3. Plot of the volume leakage current density versus the depletion width W for a LOCOS diode in a p-type substrate (a) and for an STI diode in a p-well (b).

In practice, I-V measurements have been performed on a HP4156 Parameter Analyzer with a thermo-chuck, able to operate up to at least 120° C. I-V measurements have been performed with a bias step of 0.01 V, from reverse (V_R) to forward voltage (V_F), using a hold time of 30 s before the start of the voltage sweep. The latter is necessary to avoid any leakage current transients, which may occur after switching off the microscope light of the wafer probe-station [18]. Temperature dependent measurements have been performed on wafer (fragments) in the range from 25°C to 120° C. Sufficient waiting time is allowed in order to stabilize the wafer at each selected temperature. The whole set of diodes of one chip is measured before selecting the next higher temperatures, after each set of Arrhenius plot measurements, a control at 25° C was performed, to verify the amount of annealing.

C-V measurements are performed on a HP 4275 multi-frequency LCR meter at 100 kHz and 30 mV ac modulation signal for reverse diode operation. A V_R step of 0.1 V is applied from 0 to -5 V. Temperature measurements in the same range have been performed. In order to calculate the carrier density profile the derivative of $1/C^2$ is plotted versus the depletion width. The latter is derived from the volume capacitance C_A (F/cm²) (derived from the total capacitance after correction for the perimeter contribution) as follows:

$$W = \varepsilon_s / C_A \tag{5}$$

 $\varepsilon_{\rm s}$ is the permittivity of silicon.

The irradiation matrix is given in Tables Va to Vc, representing the 20 MeV proton, the 2 MeV electron and 1 MeV neutron experiments. Proton and electron irradiations were performed at the linear accelerator of the Takasaki JAERI, while neutron exposures took place at the nuclear reactor of the Rikkyo University both in Japan (May 1999). Post-rad I-V and C-V characterization was performed in IMEC from 1 till 10 September 1999 by Dr. Hayama, P. Van Dorpe and A. Poyai.

S denotes a packaged device, in TO-12 headers. Only the unpackaged proton irradiated diodes have been studied as a function of temperature.

Table Va. 20 MeV proton irradiation matrix for the STI diodes. No bias was applied during the irradiations. The exposures took place in May 1999 at Takasaki JAERI.

Wafer	Sample	Fluence (cm ⁻²)
3	3-1 3-2 3-3	$10^{12} \\ 10^{13} \\ 10^{14}$
6	6-1 6-2 6-3	$ \begin{array}{c} 10^{12} \\ 10^{13} \\ 10^{14} \end{array} $
9	9-1 9-2 9-3	$ \begin{array}{c} 10^{12} \\ 10^{13} \\ 10^{14} \end{array} $
12	12-1 12-2 12-3	$ \begin{array}{c} 10^{12} \\ 10^{13} \\ 10^{14} \end{array} $
14	14-1 14-2 14-3	$10^{12} \\ 10^{13} \\ 10^{14}$

Table Vb. 2 MeV electron irradiation matrix for the STI diodes. No bias was applied during the irradiations. The exposures took place in May 1999 at Takasaki JAERI.

Wafer	Sample	Fluence (cm ⁻²)
3	S3-1	10 ¹³
	S3-2	10^{14}
	S3-3	10 ¹⁵
6	S6-1	10^{13}
	S6-2	10 ¹⁴
	S6-3	10 ¹⁵
9	S9-1	10 ¹³
	S9-2	10^{14}
	S9-3	10 ¹⁵
12	S12-1	10^{13}
	S12-2	10^{14}
	S12-3	10 ¹⁵
14	S14-1	10 ¹³
	S14-2	10^{14}
	S14-3	10 ¹⁵

Table Vc. 1 MeV neutron irradiation matrix for the STI diodes. No bias was applied during the irradiations. The exposures took place in May 1999 at Rikkyo University.

Wafer	Sample	Fluence (cm ⁻²)
3	S3-4 S3-5	$10^{12} \\ 10^{13}$
6	S6-4 S6-5	$10^{12} \\ 10^{13}$
9	S9-4 S9-5	$10^{12} \\ 10^{13}$
12	S12-4 S12-5	$10^{12} \\ 10^{13}$
14	S14-4 S14-5	$10^{12} \\ 10^{13}$

II.3. Pre-radiation characteristics (summary)

Extensive pre-radiation characterization of the STI diodes has been and is being undertaken. This goes beyond purely electrical characterization and includes the application of spectroscopical techniques like DLTS, dedicated lifetime measurements, using a cross-sectional microwave absorption technique, stress measurements (Raman spectroscopy) and structural characterization (TEM). Some of the results will be published shortly [19]. Here, only a brief summary will be given. Furthermore, it has been observed recently that the classical separation scheme does not properly work for STI diodes because of the typical structure (see Fig. II.1). In addition, it is not straightforward to combine square and meander diodes in order to separate the components, implying that Eq. (1) may no longer be applicable in certain cases. Refined techniques are currently under investigation to improve our methodology.

In Fig. II.4a and II.4b, the I-V and C-V characteristics of a set of square and meander diodes is represented. The scaling of I and C with the area for the SQ diodes is obvious in these figures. To some extent, this also goes for the ME diodes. Overall, acceptable pre-rad characteristics are obtained, with a high yield across the wafer. As can be seen from Fig. II.5a and II.5b, there is little impact of the splits on the SQ1 or ME1 diode characteristics. The same applies for the other geometries. It should be remarked, however, that there is some spread in the I-V across each wafer, whereby the central part generally yields the lowest leakage current. The curves in Fig. II.5 have all been obtained from diodes at exactly the same wafer position to rule out this position dependence.

Figure II.6 illustrates the impact of the temperature on the current (a) and capacitance (b) of a SQ1 diode. While there is an evident increase of the reverse (and to a lesser extent of the forward current) with T, marginal changes are found for the capacitance. This is explained by the fact that the only temperature dependent parameter is the built-in potential V_{bi} , which is weakly reducing with T and, furthermore, occurs under a square root of $(V_{bi}+V_R)$.

The extracted volume leakage current density for the different splits is represented in Fig. II.7, the corresponding Arrhenius plot is shown in Fig. II.8. From the Arrhenius plot, a low activation energy of 0.28 eV is extracted for the generation current density, while at higher temperatures an activation energy of 1.15 eV is observed, in agreement with the expectations.

Finally, Fig. II.9 gives a typical example of the carrier density profile in part of the depletion region, which is accessible by the C-V measurement. No uniform hole density is observed, as expected for the double boron implanted retrograde p-well. This may complicate the interpretation of the post-rad data.

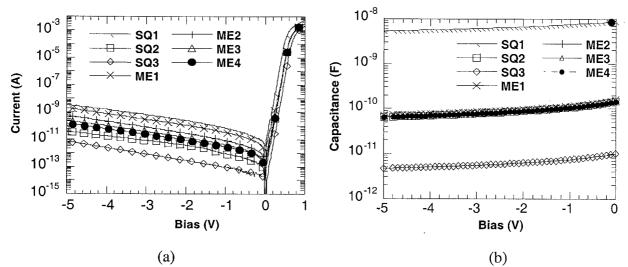


Fig. II.4. I-V (a) and C-V (b) characteristics of a set of different geometry STI diodes, belonging to wafer 11.

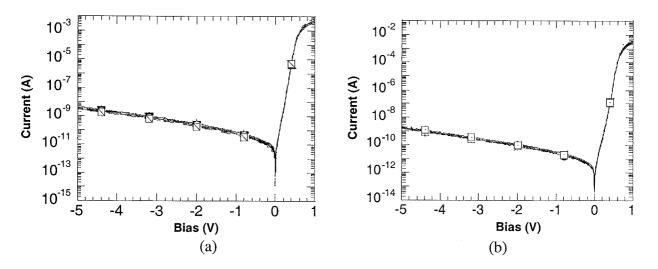


Fig. II.5. I-V characteristics of SQ1 (a) and ME1 (b) diodes of different splits.

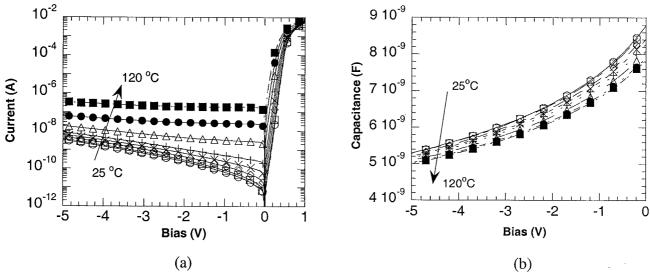


Fig. II.6. I-V (a) and C-V (b) characteristic of a SQ1 diode as a function of temperature. The diode belongs to wafer 11.

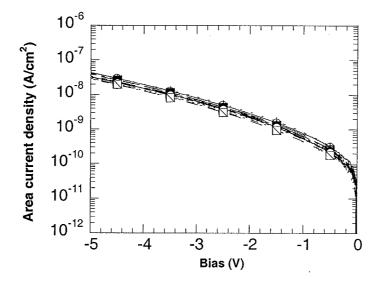


Fig. II.7. Area current density versus reverse bias for the different STI wafer splits (central diode).

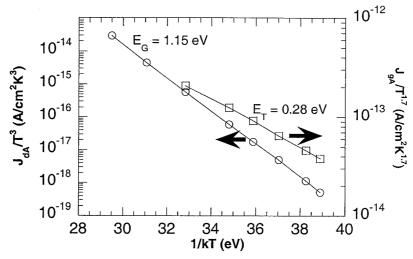


Fig. II.8. Arrhenius plot of the generation current density for wafer 11 showing an activation energy of 0.28 eV for low T at -1V and of 1.15 eV for higher temperatures. Two vertical axes are used to represent the diffusion current (Eq. (2)) or the generation current (Eq. (3)).

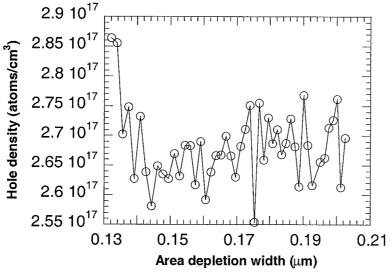


Fig. II.9. Hole density profile in part of the p-well region below the p-n junction, derived from a corrected C-V measurement on a SQ1 diode.

II.4. Post-radiation characteristics

This section gives a summary of the post-radiation characteristics. First, a brief description will be given of the characteristics of a proton irradiated set of diodes: the impact of the geometry and temperature will be described. Qualitatively similar results have been obtained for the electron and neutron irradiated samples. The impact of annealing during the temperature measurements will be discussed and the activation energies will be given. Next, the change of the I-V characteristics with particle fluence will be reported. From the increase of the current with fluence, a damage coefficient will be derived as follows:

$$K_{\Phi} = \Delta I / \Delta \Phi \tag{6}$$

and the impact of the different particles will be outlined.

Figure II.10a represents the I-V characteristics of the different geometry diodes of sample 12-2 at 25°C, corresponding with a 20 MeV proton irradiation and a fluence of 10^{13} cm⁻²; Fig. II.10.b shows the same characteristic after a temperature dependent measurement up to 120° C. As can be derived from comparing the two figures, a roughly 10 % reduction in current is observed. This is illustrated more clearly in Fig. II.11. At 120° C, the reverse current is nearly 2 decades larger (compare e.g. Fig. II.10 with Fig. II.12). This increase is, however, less pronounced as before irradiation (Fig. II.6a), implying a lower effective activation energy in a broad temperature range. In Fig. II.13, the C-V plots corresponding with the diodes of Fig. II.10 are given, showing a scaling with the diode area.

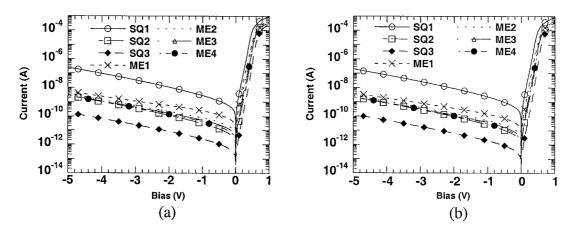


Fig. II.10. I-V characteristics at 25°C before (a) and after (b) heating the 20 MeV 10¹³ cm⁻² proton irradiated chip to 120°C.

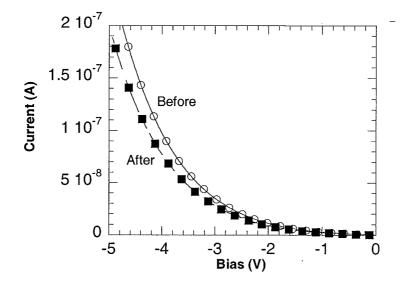


Fig. II.11. I-V curve of a SQ1 diode at 25°C before and after a high temperature measurement.

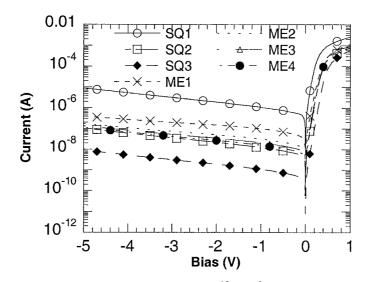


Fig. II.12. I-V characteristics of sample 12-2 (10^{13} cm⁻² H⁺) at 120° C.

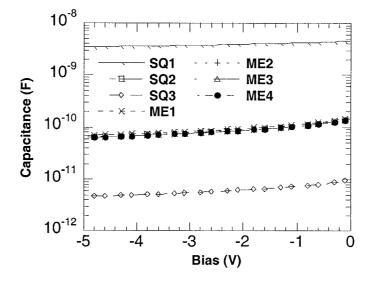


Fig. II.13. C-V characteristics of sample 12-2 (10¹³ cm⁻² H⁺) at 25°C.

The Arrhenius plot of Fig. II.14 shows that there are at least two slopes in the curve, corresponding with an activation energy of around 0.58 eV at low T and remarkably reducing to 0.50 eV for higher T. The reverse bias is low (-1 V) in order to minimise field effects. Other samples show qualitatively a similar tendency, e.g. E_{actlow} =0.48 eV and $E_{acthigh}$ =0.66 eV for 12-1, while a unique value of 0.54 eV has been found for #9-3.

Figure II.15 illustrates the impact of the 20 MeV proton fluence on the I-V characteristics of a wafer 12 SQ1 diode at 25 °C. Hereby corresponds the curve labeled **non** with the pre rad conditions. The figure shows that:

- the reverse current increases roughly one decade for a decade increase in fluence.
- this increase is parallel in function of the reverse bias.
- there is also an increase of the forward current at low V_F with Φ , indicating an enhancement of the recombination current component.
- On the other hand, for large V_F , the I_F drops continuously with Φ , suggesting an increase of the series resistance and, hence, a deactivation of the B dopants in the p-well. This is confirmed by the post-rad reduction of the capacitance (compare e.g. Figs II.4a and II.13).

Similar conclusions can be drawn for the ME1 meander diodes of Fig. II.16.

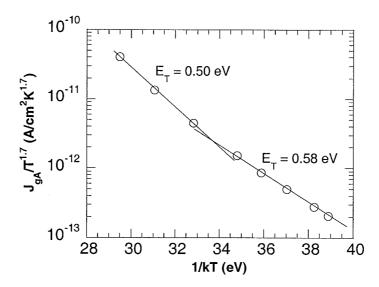


Fig. II.14. Arrhenius plot for the generation current density of sample 12-2 (10^{13} cm⁻² H⁺). V_R =-1 V.

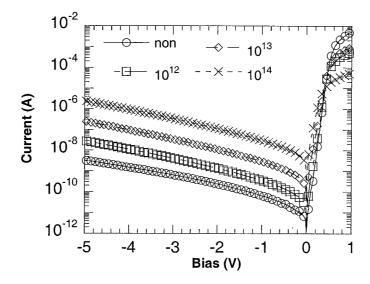


Fig. II.15. I-V characteristic of 20 MeV proton irradiated SQ1 STI diodes in function of the fluence Φ. Curve **non** corresponds to a non exposed sample.

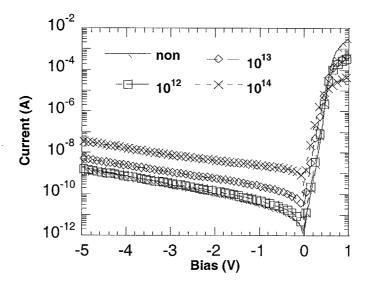


Fig. II.16. I-V characteristic of 20 MeV proton irradiated ME1 STI diodes in function of the fluence Φ. Curve **non** corresponds to a non exposed sample.

The degradation of the reverse current after proton irradiation for a SQ1 diode is summarised in Fig. II.17, for different reverse biases. As can be seen, a more or less linear increase is found. From the slope of the straight line fits a first order damage coefficient, as defined in Eq. (6) can be derived. It is clear that the damage coefficient increases strongly with the reverse bias. Similar results are obtained e.g. for the ME1 diode shown in Fig. II.18. The results for the different STI splits are represented in Fig. II.19, showing a marked impact of the STI processing on the perimeter leakage current. Split 6 yields the best overall K_{Φ} for proton irradiation.

Qualitatively similar results are obtained for the electron and neutron irradiations, summarised in Figs II.20 to II.25. Finally, the damage coefficients for the different particles corresponding to split 12 are shown in Fig. II.26. As expected from the particle mass and energy, the highest coefficients are observed for the 20 MeV proton irradiations, followed by neutron and, finally, electron $K_{\Phi S}$. This is also observed in

Fig. II.27, giving the damage coefficient for the ME1 diodes at a reverse bias of -1 V. Interestingly, there is a more or less systematic dependence on the STI split, both for charged and neutral particle irradiations. The most pronounced effect is for proton exposures, with a minimum for split 6. Also for electron and neutron irradiations, wafer 6 (and 3) yield a lower degradation. This could point to a different amount of ionisation damage in the ST-isolation for different processing conditions, which may vary a factor of 1.5 between the lowest and the highest damage. The fact that there is also an effect for neutron exposures could emphasize the role of displacement damage in the peripheral diode region, thereby enhancing the bulk generation current in the lateral depletion region.

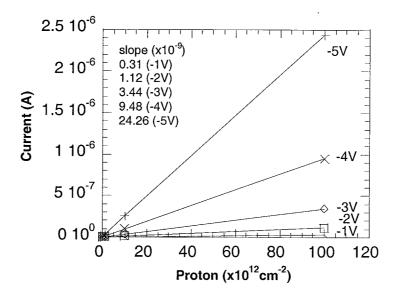


Fig. II.17. Reverse current at different reverse bias for the SQ1 diodes of split 12 at 25°C, after proton irradiation.

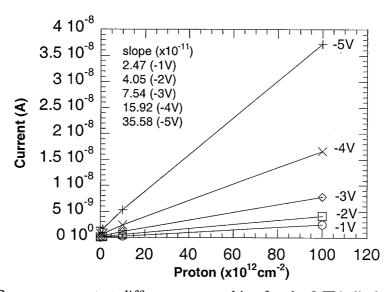


Fig. II.18. Reverse current at different reverse bias for the ME1 diodes of split 12 at 25°C, after proton irradiation.

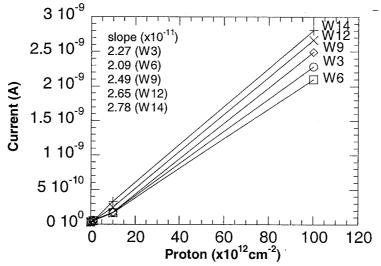


Fig. II.19. Reverse current at -1 V for the proton irradiated ME1 diodes at 25° C, corresponding with the different processing splits.

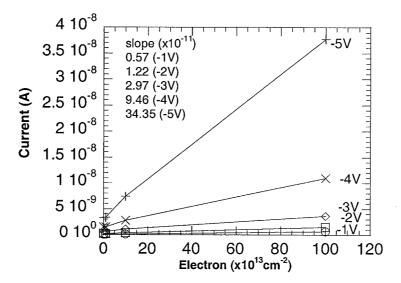


Fig. II.20. Reverse current at different reverse bias for the SQ1 diodes of split 12 at 25°C, after electron irradiation.

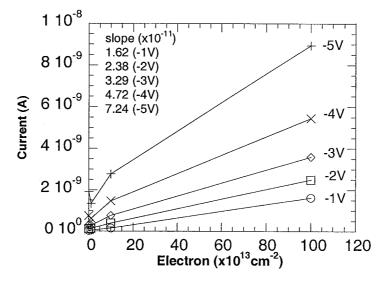


Fig. II.21. Reverse current at different reverse bias for the ME1 of split 12 diodes at 25°C, after electron irradiation.

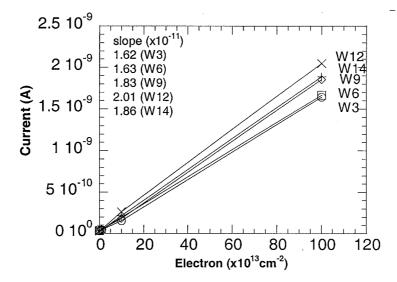


Fig. II.22. Reverse current at -1 V for the ME1 diodes of the different STI processing splits at 25°C, after electron irradiation.

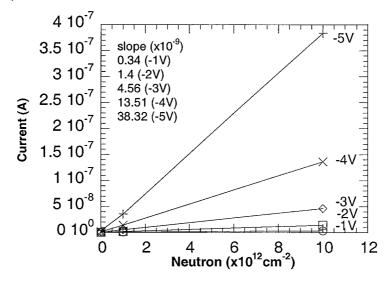


Fig. II.23. Reverse current at different bias for the neutron irradiated SQ1 diodes of split 12 at 25°C.

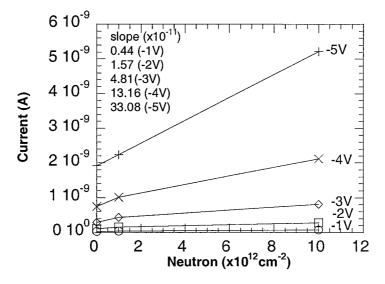


Fig. II.24. Reverse current at different reverse bias for the neutron irradiated ME1 diodes of split 12 at 25°C.

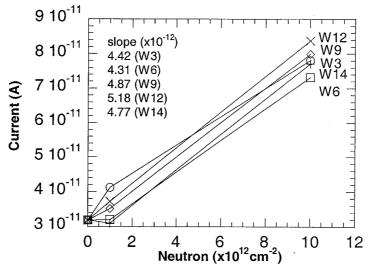


Fig. II.25. Reverse current at -1 V for the neutron irradiated ME1 diodes at 25° C, corresponding with the different processing splits.

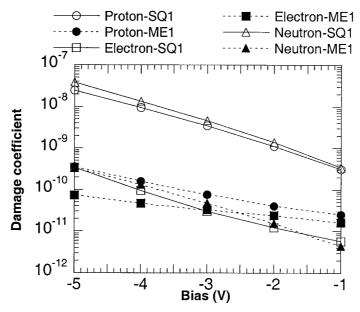


Fig. II.26. Damage coefficient at different reverse bias for the SQ1 and ME1 diodes of split 12, for the different particle irradiations. T=25°C.

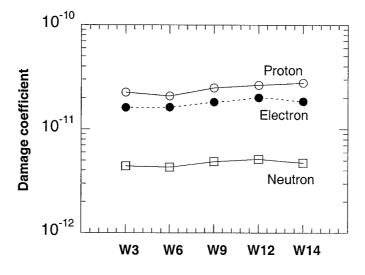


Fig. II.27. Damage coefficients of the irradiated ME1 diodes at -1 V and 25 °C corresponding with the different particles and STI processing splits.

II.5. Summary and Outlook

In summary, it can be said that these initial radiation studies of STI diodes have revealed that:

- there is an impact of the STI processing on the radiation response, for high energetic particles generating ionisation damage in the trench oxide.
- this sensitivity of the perimeter leakage to particle irradiation will certainly also has an impact on the behavior of CMOS devices with STI.
- the study of different geometry diodes is helpful in resolving the different leakage current mechanisms and the response to irradiation.
- from the post-rad Arrhenius measurements, activation energies are retrieved with should provide information on the dominant radiation induced generation centers.

Future studies should first of all focus on a further refined analysis of the raw data presented above. This will proceed along with the development of improved I-V and C-V extraction methods, dedicated to the analysis of the shallow-trench diodes. In addition, the I-V and C-V data should be backed up by complementary analysis techniques like DLTS, microwave absorption measurements, etc... This will help in establishing physical models for the radiation-induced damage. In addition, it should be investigated whether part of the observations can be described in the frame of the NIEL concept or not. Therefore, proton irradiations at other energies (8, 60 MeV,...) are scheduled in order to enlarge the data base.

General Conclusions

It has been demonstrated in that deep submicron transistors and process modules suffer from radiation damage albeit for a higher fluence range than typically encountered in a space environment. However, even for a fluence of $3x10^{10}$ cm⁻² 60 MeV protons, some subtle changes are induced particularly in the n-channel transistors. In fact, unusual device parameter shifts have been noted, i.e. an increase of the threshold voltage for example, which become furthermore length dependent. These two aspects deserve and require further in-depth studies in view of the ongoing trend in downscaling. The results suggest that some new or modified degradation mechanisms occur, which are maybe no longer related to the thin gate oxide itself, but to other parts of the device structure, such as e.g. the isolation along the edges or the extension region. In addition, one should not overlook the impact of non-ionising energy losses in the highly doped p-well (substrate) regions upon interaction with protons. The generation of radiation-induced trap levels generally increases with the doping density. This is certainly the case for boron, which is known to interact with interstitials to create mobile interstitial boron B_i. It could be worthwhile in future experiments on MOS transistors to assess the changes (if any) in the p-well doping density by measuring for example the body factor dependence on the threshold voltage V_T. Also the study of diodes processed in the corresponding well could facilitate such a study, by using C-V measurements.

The observed length-dependence of the parameter shifts is quite intriguing and can be to some extent understood in view of the charge-sharing concept. However, a further modeling is required in order to fully understand what is going on and to include the role of inhomogeneous damage creation along the channel. This is related to the LDD/HDD device architecture used for deep submicron transistors. In addition, it is worthwhile to extend these studies to the next generation of technologies (0.15 µm and beyond) which contains STI and other advance processing steps (e.g. Cu metallisation,...). Additional device parameters which are of great potential interest are the low-frequency noise and the series resistance.

From the radiation studies of the STI diodes it has become clear that ionisation damage in the trench oxide occurs and affects the surface generation/recombination current of ST-isolated diodes. Given the large impact of peripheral and corner components on the leakage currents of downscaled source/drain junctions, this is an important observation. The advantage of using a diode as a test vehicle is that it is more easy to assess such degradation effects, which should allow a better insight in what is going on. In addition, the study of the bulk current component enables to investigate whether the NIEL concept is useful for such advanced diodes and allows the extraction of the lifetime parameters τ_r and τ_g . Combining lifetime and Arrhenius measurements should give an indication of the dominant generation-recombination (GR) centers in irradiated p-well diodes. This information could then be linked to more spectroscopic studies like DLTS or low-frequency noise.

Another exciting observation is that there appears to be some effect of the STI processing on the radiation damage and response of the diodes. This means that in principle one can optimise the STI module for radiation hardness. The data are in any case useful if this would become an issue later on. A similar approach could be

followed in order to study other advanced processing modules, which are currently under development for future technology generations.

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Appendix I: Bonding Diagram of the Ring-Oscillators

	Osc25	Osc	15r
4	VSSA	7	VSSA VDDA VSSB Output VDDB Input
5	VDDA	8	
6	VSSB	9	
19	Output	16	
20	VDDB	17	
21	Input	18	

Appendix II: Measurement Diary of the Individual Transistors

Sample Proton Fluence (x10 ¹⁰ cm ⁻²)	Transistor L _{poly} (μm)	V_T S g_{mmax} V_{TIV} (V) (mV/dec) (μS) (V)	Remarks
L10-1	N0.48	0.369 72 333.8 0.35	
No (pre)	N0.38 N0.33 N0.28	0.372 72 438 0.35 0.373 72 495.1 0.35 0.370 72 574.0 0.34	
	N0.23 N0.205 N0.18	0.361 72 704.2 0.30 0.323 72 768.2 0.24 0.266 78 815.8 0.14	
	P0.48 P0.38 P0.33 P0.28 P0.23 P0.205 P0.18	-0.239 ? 74.6 -0.19 -0.237 ? 91.5 -0.19 -0.233 ? 107.7 -0.19 -0.235 ? 137.2 -0.18 -0.216 ? 174.9 -0.18 -0.171 ? 201.0 -0.09 -0.088 ? 241.4 +0.04	Unique S difficult to extract p-MOS
L10-1	N0.48	0.354 74 228.8 0.34	
3x	N0.38 N0.33 N0.28	? ? ? ? 0.361 75 341.6 0.34 0.360 74 395.4 0.34	Gate Leakage
	N0.23 N0.205 N0.18	? ? ? ? 0.322 87 745.3 0.24 0.267 114 772.6 0.135	Gate Leakage
	P0.48 P0.38	-0.231 ? 74.5 -0.19 -0.236 ? 91.5 -0.19	Unique S difficult to
	P0.33 P0.28 P0.23 P0.205 P0.18	-0.24 ? 107.0 -0.20 -0.234 ? 137.0 -0.19 ? ? ? ? -0.089 ? 242.2 +0.03	extract p-MOS

Sample Proton Fluence (x10 ¹⁰ cm ⁻²)	Transistor L _{poly} (μm)	$ \begin{array}{c cccc} V_T & S & g_{mmax} & V_{T1V} \\ \hline (V) \ (mV/dec) \ (\mu S) & (V) \end{array} $	Remarks
L10-2 10x	N0.48 N0.38 N0.33 N0.28 N0.23 N0.205 N0.18	0.400 80 306.7 ? ? ? ? ? 0.407 80 476.5 0.37 0.403 80 542.1 0.36 ? ? ? ? 0.348 82 687.0 ? 0.233 ? 778.7 ?	Gate Leakage Gate Leakage
	P0.48 P0.38 P0.33 P0.28 P0.23 P0.205 P0.18	-0.280 ? 70.8 -0.23 -0.256 ? 92.2 -0.20 -0.262 ? 106.9 -0.075 -0.249 ? 131.9 -0.190 -0.242 ? 178.0 -0.175 -0.190 ? 196.6 -0.100 ? ? ? ?	Unique S difficult to extract p-MOS Gate Leakage

Sample Proton Fluence (x10 ¹⁰ cm ⁻²)	Transistor L _{poly} (μm)	V_T S g_{mmax} V_{TIV} (V) (mV/dec) (μS) (V)	Remarks
L16-1	N0.48 N0.38	0.470 75 357.6 0.455	
No (pre)	N0.33 N0.28 N0.23 N0.205	0.470 75 459.3 0.455 0.454 75 644.6 0.42 0.344 76 882.7 0.24	
	P0.48 P0.38 P0.33 P0.28 P0.23 P0.205 P0.18	0.237 83.3 1000.9 0.11 -0.472 82 61.4 -0.46 -0.468 82 77.3 -0.45 -0.466 82 89.0 -0.45 -0.456 82 109.7 -0.437 -0.445 82 136.8 -0.415 -0.433 82 158.3 -0.400 -0.420 82 182.0 -0.380	
L16-1	N0.48	0.504 ? 323.1 0.480	Gate Leakage
3x	N0.38 N0.33 N0.28 N0.23 N0.205	0.505 85 398.0 0.475 0.484 85 577.4 0.440 0.366 87 762.8 0.270	Gate Leakage Gate Leakage
	P0.48 P0.38 P0.33 P0.28 P0.23	 -0.505 83.3 69.8 -0.48 -0.457 83.3 105.1 -0.43 -0.443 83.3 132.7 -0.42	Gate Leakage Gate Leakage Gate Leakage
	P0.205 P0.18	-0.432 83.3 155.3 -0.41	Gate Leakage