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GUIDELINES FOR CRYOGENIC SPACEBORN CMOS TESTING AND OPTIMIZATION

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ABSTRACT

The development of cryogenic CMOS for space applications is a complex matter, which should combine a number of desired features: good electrical device performance at the operating temperature, low power dissipation and noise and, naturally, good radiation tolerance. Generally, one faces conflicting interests, so that a compromise for optimizing the device architecture, technology and design must be found. When dealing with Liquid Helium Temperature (LHT) applications some additional hurdles need to be overcome. First of all, device and circuit simulators have not been developed for the LHT regime. At best, they can be extended down to 77 K or so, by implementing the temperature dependence of the basic material and transport properties. However, to predict or reproduce 4.2 K operation, additional features should be included like the occurrence of the kink effect and the related noise, or the transient and hysteresis behavior found typically below carrier freeze-out (T<30 K). This is the more true for the radiation response of cryogenic CMOS, where a lack of experimental data exists. An additional factor to be accounted for is the peculiarities often encountered when testing devices or circuits at LHT, complicating the extraction of the first-order device parameters.

The aim of the present paper is to define some practical guidelines for the development, the design and the testing of radiation-hard cryogenic electronics intended for operation in the liquid helium temperature (LHT) range. They are formulated keeping two main goals in mind: first, successful operation at 4.2 K and, second, providing sufficient resistance against (space) radiation damage.

1. INTRODUCTION

The successful operation of CMOS circuits at cryogenic temperatures is often hampered by carrier freeze-out, leading to an increase of the series resistance and kink, transient and hysteresis effects caused by carrier multiplication phenomena near the drain region [Refs 1-2]. The occurrence of a kink will have a direct influence on the excess 1/f noise of the devices [Refs 3-4]. To suppress multiplication effects at room temperature, it is common for submicron devices to implement lowly-doped drain (LDD) regions since they lower the maximum electric field, thereby impacting short-channel effects such as e.g. hot-carrier phenomena. In this respect, it should be remarked that carrier heating is generally much more pronounced for electrons than for holes, explaining why n-MOSFETs are more of concern than their p-channel counterparts. However, for cryogenic temperatures less information is available and below 30 K these regions will be more prone to carrier freeze-out [Ref. 5]. This implies that in addition to a threshold voltage shift, also the series resistance strongly increases for small drain biases. The device conductance in linear operation becomes lower at 4.2 K than at 300 K, so that the mobility increase advantage is lost. Especially for smaller gate lengths the effect can be pronounced [Ref. 6]. Submicron CMOS technologies to be implemented in cryogenic electronics for future space missions should therefore be optimised. This aspect will be addressed more in detail for the pre-irradiation electrical performance of a 0.7μm CMOS technology, for the moment a strong candidate for the read-out electronics of the FIRST mission.

Due to the cryogenic operation of the devices, special attention has to be given to simulations, measurements and parameter extraction [Ref. 7]. The commonly used device simulators are not very well suited for LHT operation, so that it is hard to predict essential static device parameters like e.g. the threshold voltage V_T, for given processing conditions. This means that the development of cryogenic CMOS is still more of an art and is heuristic in nature. Nevertheless, based on the experience in this field, gained over the past decade and on what is available in the open literature, the impact of a number of processing steps can be described quite accurately and their appropriateness for cryo-electronics judged upon. The present paper gives special attention to some important processing steps, such as the presence of a lowly doped drain, the impact of a p-well implantation for the n-channel devices, and the role of a threshold voltage adjust implantation. Some dedicated test features will also be addressed.

It has to be taken into account that during space missions, non-negligible amounts of radiation are encountered. This refers to both ionizing irradiation due to e.g. γ's and bulk damage associated with high-energy protons [Ref. 8]. Recent investigations have pointed out that a radiation environment may have a beneficial impact on the low temperature electrical performance of the devices, i.e., a post-irradiation suppression of the kink effect has been reported [Ref. 9]. The next section therefore discusses the post-irradiation performance of submicron CMOS devices at 4.2 K.

Finally, the last sections define some practical guidelines and recommendations for cryogenic operation of microelectronics circuits in a radiation environment. Beside technological and testing aspects, design considerations are also addressed.

2. EXPERIMENTAL

Although the defined guidelines are intended to be generic in nature, the experimental validation has been on devices and test circuits processed in an optimised cryogenic 0.7 μm CMOS technology, fabricated at Alcatel-Microelectronics. The optimisation, which will be discussed further in detail, was aimed at the fabrication of the read-out electronics for the FIRST mission. A standard polysilicon-buffered LOCal

Oxidation of Silicon (PBL) isolation is used, in combination with a 16 nm gate oxide. As mentioned before, the optimization is focussed on three technological parameters, i.e., the implementation of LDDs, the use of a p-well for the n-channel devices and the conditions for the threshold voltage adjust ion implantation. The description of the different processing splits is summarized in table I. Although the starting basis was a standard 0.7 µm CMOS technology, the optimization for cryogenic operation is focused on these process modules. Initially, optimization for pre-irradiation cryogenic operation was envisaged. However, as will be demonstrated, the irradiation conditions strongly impact the preferred process matrix.

Table I. *Processing splits used to optimize the 0.7 μm cryogenic CMOS technology.*

Wafer	p-well	V_T-adjust	LDD
1	+	+	+
6	+	+	
9	+		+
11	+		
13		+	+
16		+	
19			+
22			

Pre- and post-irradiation testing is based on the input drain current – gate voltage (I_D-V_{GS}) and output drain current – drain voltage (I_D-V_{DS}) characteristics, the threshold voltage V_T, the subthreshold slope S, and the transconductance g_m. Important phenomena such as kink effect, transient and hysteresis behavior are also taken into account. Measurements have been done on dual-in-line packaged devices, mounted in a sample-holder which was immersed directly in the liquid helium.

To investigate some design aspects, both isolated and circular (CIRC) or closed-geometry devices, with an inner drain contact surrounded by the source and, therefore, no edge isolation region, were tested. In some cases also cascode (CASC) transistors, i.e., consisting of a dual gate structure whereby two MOSFETs of the same gate length are placed in series, were studied.

The proton and ^{60}Co-irradiations were performed using the facilities in Louvain-la-Neuve (Belgium). For the 60 MeV protons a fluence range of $3x10^{10}$ cm^{-2} up to 10^{12} cm^{-2} and a flux of $5x10^{8}$ $cm^{-2}s^{-1}$ was used, while total dose experiments were done at a dose rate of 5 krad/hr for 50 and 100 krad(SiO_2). All irradiations were done at room temperature, with a +5 V (0 V) gate bias for the n-MOSFETs (p-MOSFETs) while the other terminals (source, drain, p-well) were grounded. The post irradiation measurements took place within 24 h of the exposures, in order to limit the impact of room temperature annealing.

3. PRE-IRRADIATION PROCESS OPTIMISATION

3.1 Impact of LDD

The main reason for implementing an LDD structure in a submicron technology is to increase the reliability by reducing hot-carrier effects. For cryogenic operation, LDDs also have a beneficial impact on the kink effect by suppressing multiplication phenomena. However, as illustrated by figure 1 for some process options, LLDs are not an absolute requirement for obtaining kink-free devices. In case of no LDD, a V_T adjust implant has a beneficial impact (see figure 1c). This is believed to be related to an enhanced Coulomb scattering probability, which lowers the occurrence of hot-carrier energy loss by a band-to-band impact ionisation event.

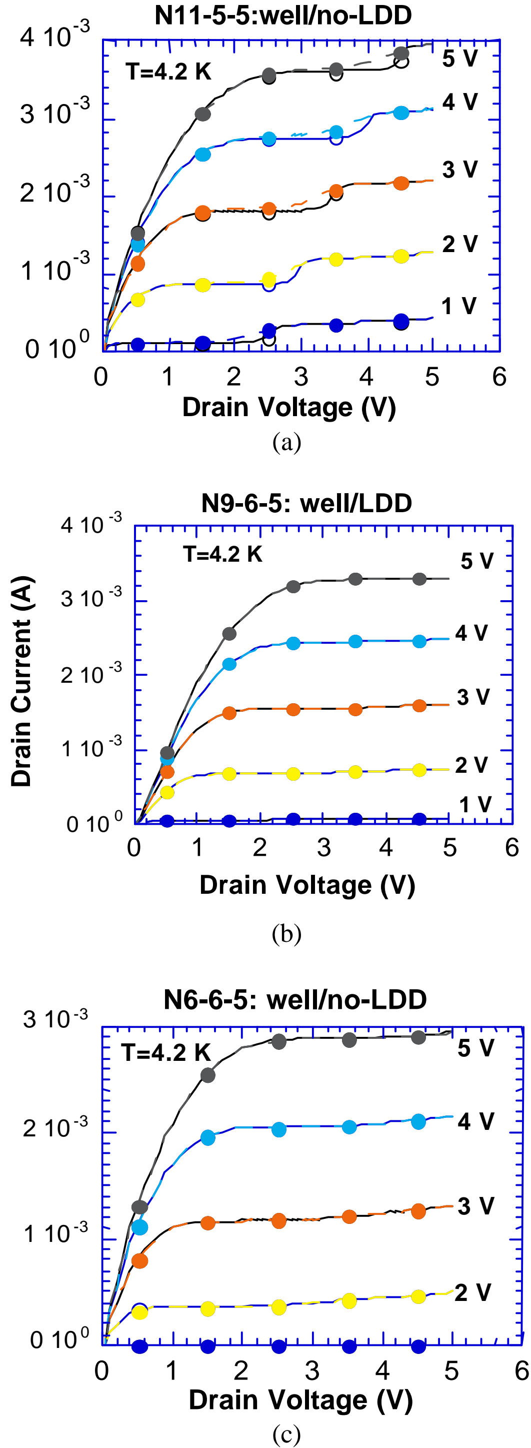


Figure 1. *Output characteristics at 4.2 K of a 10 μmx5 μm n-MOSFET for different process conditions: a) well/no-LDD/no*

adjust implant (wafer 11), b) well/LDD/no adjust implant (wafer 9), and c) well/no-LDD/adjust implant (wafer 6).

Therefore, preference is given to the wafer with p-well, without LDD and with V_T adjust implant as these processing conditions are close to the standard room temperature process of wafer 1. Leaving out the p-well would increase the tendency of kink and hysteresis effects, as will be discussed further.

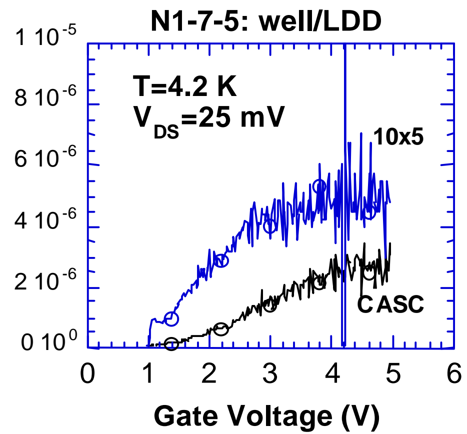
As already mentioned, when LLDs are implemented the associated series resistance R_S at 4.2 K will increase due to carrier freeze-out. For deep submicron devices (0.25 µm and below) the device scaling requires an increase of the LDD doping, so that it is expected that carrier freeze-out will be less problematic. It has been reported that at LHT the R_S becomes a function of the lateral electric field [Ref. 10], making the extraction of R_S and also ΔL (the difference between the electrical and the polysilicon gate length) more difficult and requiring a special approach [Ref. 7], as discussed below. LLD devices are also more prone to low frequency noise, associated with the interface region underneath the oxide spacers, hampering their use for analog circuit applications.

Numerous techniques to extract R_S and ΔL at 300 K have been proposed, which, however, fail when applied to 77 K for example. This has several reasons. For example, the popular "shift and ratio" method assumes that R_S is gate voltage independent in first instance [Ref. 11]. This assumption is generally not valid at cryogenic temperatures, where a more pronounced gate-source voltage V_{GS} dependence is expected to occur. In addition, for LDD devices there can also be a marked drain bias dependence of the series resistance. In order to cope with these problems, dedicated techniques have been proposed (for an overview see e.g. Ref. 7). A simple method only uses two transistors, instead of an array of several devices with constant width W [Ref. 12]. It is shown to be applicable at 77 K to both bulk and SOI transistors, for not too small gate lengths. For deep submicron devices, a modified shift and ratio method has been proposed, again only using a long reference device and a short one, which is in principle useful down to the LHT range [Ref. 13].

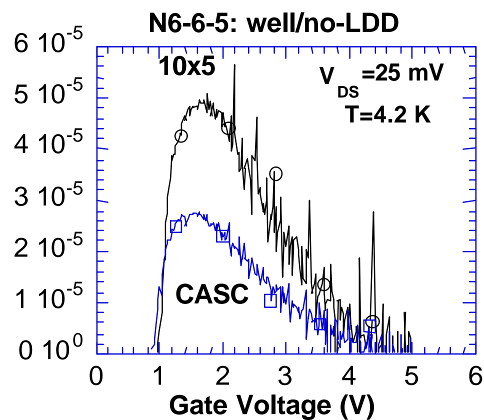
Beside the carrier multiplication related phenomena, however, it is also important to look at the other static device parameters. Figure 2 illustrates for isolated (ISO) and cascode (CASC) nMOSFETs the 4.2 K transconductance behavior for devices with and without LDD. It can clearly be seen that the no-LDD devices give the expected peak-shape of the transconductance curve. At LHT the dominant scattering mechanisms are on the one hand the Coulomb scattering associated with ionized dopant impurities and on the other hand scattering due to the presence of oxide charges (for low V_{GS}) or surface roughness (for high V_{GS}). The presence of an LDD reduces the maximum transconductance by a factor 10 in the ohmic regime. As will be shown in section 4, irradiation of an n-MOSFET generally yields a reduction of the series resistance at low V_{DS} due to the positive charge buildup in the spacer oxides and a clear increase of the transconductance.

3.2 Impact of the p-well

Concerning the impact of a p-well the following considerations can be given. Leaving out the p-well for cryogenic operation will enhance freeze-out effects and increase the impedance of the substrate. This may cause pronounced kink and hysteresis effects in the I-V characteristics. The reason for the kink is related to the fact that a considerable potential drop can be built up across the substrate (or well) resistance, between the drain and the substrate (well) contact, when a small substrate current is flowing through the device. This positive substrate potential (for an n-channel device) gives rise to a lowering of the threshold voltage and, therefore, to a kink effect. The hysteresis or transient effect is associated with the slow response of the dopants in the drain depletion region to a change in bias and hence in charge state [Ref. 14]. While the capture process proceeds quite fast, this is not so for the re-emission of trapped charge. The net result is a retarded buildup (response) of the depletion region in the substrate, an effect which is also referred to as the forced depletion layer formation [Ref. 15]. Enhancing the doping density of the p-well lowers the susceptibility to these effects and is, therefore, recommended for cryogenic CMOS technologies. This implies that the kink effect will become less pronounced for devices with smaller feature size. Also the transient and hysteresis effects should be reduced for a higher well doping density, as the higher electric field enhances the field-assisted generation of carriers from the frozen-out dopant atoms, either through the Poole-Frenkel or the tunnelling effect.



(a)



(b)

Figure 2. *Transconductance at 4.2 K of a 10 µmx5 µm n-MOSFET with (a) and without (b) LDD.*

3.3 Threshold Voltage Adjust

A third process modification studied is the threshold voltage adjustment implantation. However, omitting this step would

enhance the V_T asymmetry of the n- and p-channel devices. In addition, one has to keep into account that the trend toward the use of COTS (Commercially-of-the-shelf) devices for space applications necessitates to stay as close as possible to the standard technology, optimized for room temperature operation. Eliminating a process step, such as e.g. the LDD structure, only simplifies the process and should, therefore, have a beneficial impact on the processing cost.

3.4 Summary: Technological Guidelines

A systematic study of the static device parameters for the different processing splits clearly indicates that for the investigated 0.7 µm CMOS technology, i) the spread in threshold voltage is the smallest, and ii) a decade higher maximum transconductance is found for no-LDD devices. Omission of the V_T implantation has a beneficial impact on the mobility and the transconductance, but increases the V_T asymmetry. However, if no p-well is used for the n-MOSFETS then the implementation of a LDD has a pronounced impact on the suppression of the kink.

4. POST IRRADIATION PROCESS OPTIMALISATION

This section focuses on both proton irradiation and total dose effects. Although for space missions testing up to 50 krad is sufficient, experiments with 100 krad(SiO_2) are also performed.

4.1 60 MeV Proton Irradiations

The used processing split has a clear impact on the post-irradiation electrical performance. This is clearly illustrated in figure 3 for a proton irradiated p-MOSFET with and without a LDD structure and for a no-LDD n-MOSFET.

While for the LDD p-MOSFETs of figure 3a there is a systematic reduction of the drain current with increasing proton fluence Φ, a rebound effect is noticed for no-LDD p-channel devices. The physical origin of the difference in behavior for LDD and no-LDD devices is not fully understood yet, but is related to the radiation response of the spacer regions above the LDDs. It is generally accepted that irradiation results into the creation of positive trapped charge in the oxides. For p-channel devices this will cause a reduction of the near surface hole density in the LDDs and hence in an increase of the series resistance after irradiation. The improvement for the no-LDD p-MOSFETs at low Φ studied ($3x10^{10}$ cm^{-2}) may suggest the creation of either negative charge in the gate oxide, or positive charges in the substrate or at the interface induced by the resulting displacement damage. The first mechanism is very unlikely as the electrons created in the oxide should remain immobile so that mainly hole trapping prevails. Additional studies are needed to obtain a better insight into the occurring physical mechanisms. Moreover, the role of room temperature annealing should be further investigated. The post-irradiation observations for the n-channel devices, on the other hand, are fully explainable by positive charge buildup in the spacer oxide. It is also important to remark that the change in V_T after irradiation is about 20 times smaller for no-LDD devices compared to their LDD counterparts (see figure 4 for p-MOSFETs).

It is important to remark that the irradiations have been done at room temperature and that some time elapsed between the irradiation and the cryogenic measurement, which may lead to an in-situ room temperature anneal of the irradiation damage. However, in order to check this, some measurements have been repeated after 1.5 week. In all investigated devices, no significant room temperature anneal effects have been observed.

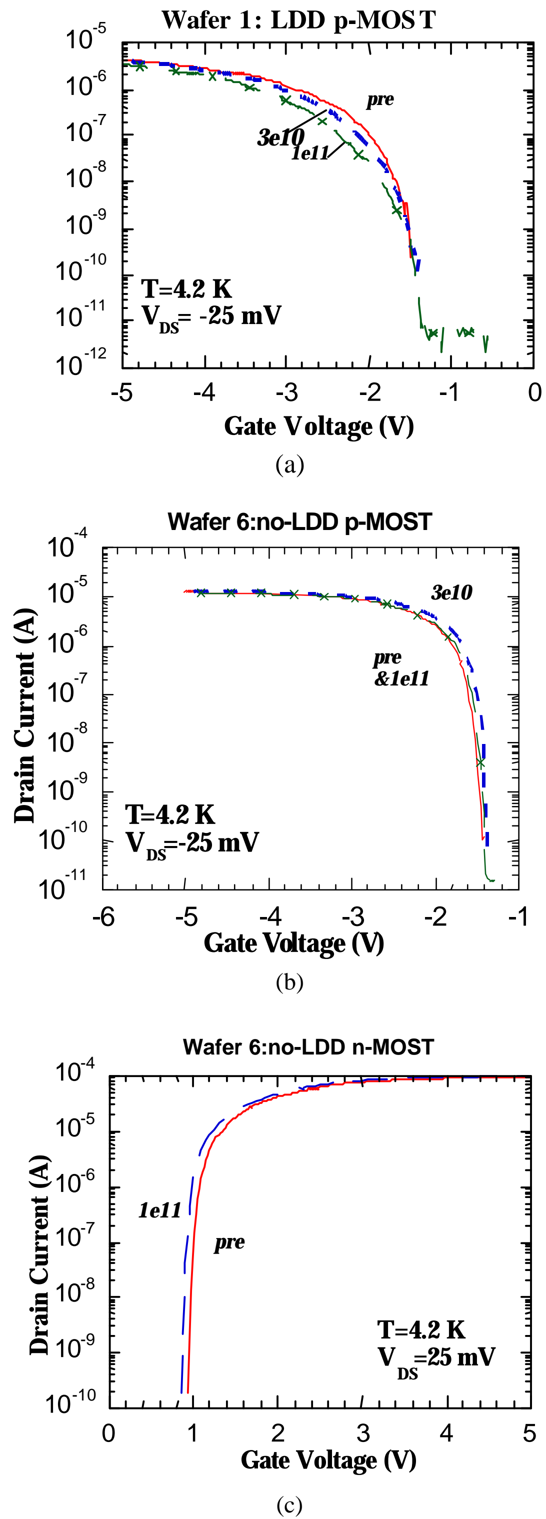


Figure 3. *Input characteristics at 4.2 K of a 10 µmx5 µm proton irradiated p-MOSFET at 4.2 K of split 1 LDD (a) and split 6 no-LDD (b), and of a no-LDD n-MOSFET of split 6 (c).*

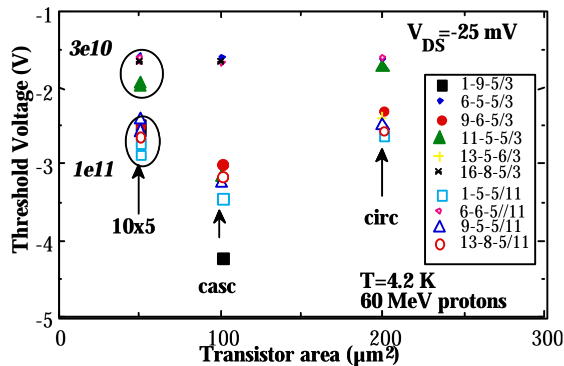


Figure 4. Threshold voltage at -25 mV and 4.2 K for proton irradiated p-MOSFETs, processed according to the different splits outlined in Table. 1.

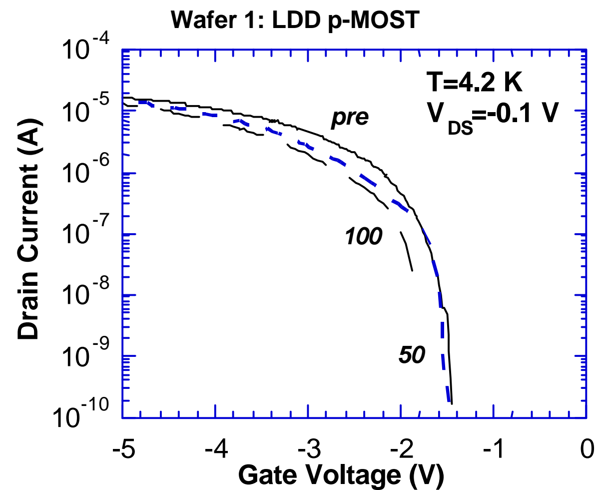
4.2 γ- Irradiations

The radiation performance has also been studied after γ-irradiations up to a total dose of 50 and 100 krad(SiO_2). Typical results are shown in figure 5 for p- and n-channel devices. More or less similar observations are seen as for the proton irradiations, with the exception of the rebound effect. Also in this case the no-LDD devices are the most radiation hard. For the LDD transistors the degradation increases with total dose and results in a reduction of the threshold voltage and a small reduction of the transconductans. However, a special feature is that for LDD devices the pre-irradiation transconductance did not show the peak-shape curve, while this is the case after γ-irradiation (see figure 6). This is true for proton irradiation where for both pre- and post-irradiation no peak-shape curve is seen.

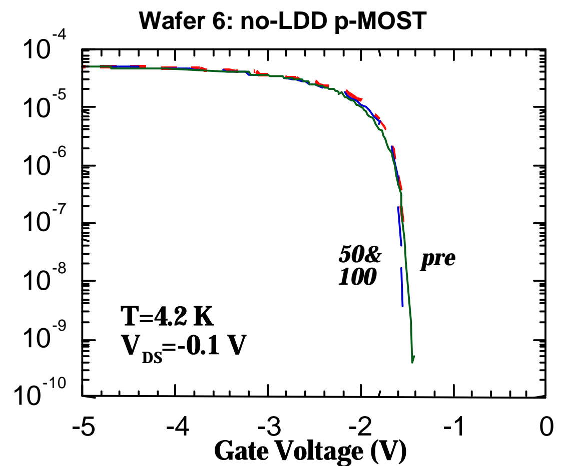
In contrast to proton irradiations, it has been observed for γ-irradiations that a room-temperature anneal occurs for the n-channel devices. This is illustrated in Fig. 6 for the transconductance. As mentioned above, for this process split it is common to see no peak-shape curve before irradiation. Immediately after the exposure the curve changes, and after a few weeks the original curve is nearly found back. A similar behavior is observed for other parameters. The p-channel devices are more in line with the proton irradiations, implying that they are not impacted by a room temperature anneal.

In general, it can be stated that the degradation at 4.2 K after room temperature γ-exposure shows the anticipated trend, i.e., a reduction of the threshold voltage and an increase of the transconductance for the n- and opposite changes for the p-channel devices. This is fully in line with the expected creation of positive charge in the oxide regions. The rebound behavior found for the no-LDD p-MOSFETs after proton irradiation is not found here.

However, a more striking result is the reduction of the kink effect after γ-irradiation, for devices showing a kink before irradiation. This is demonstrated in figure 7 for a 100 krad total dose. A similar reduction of the kink has also been noticed after proton irradiations [Ref. 5]. The physical explanation may be related to an enhancement of the carrier mean free path by the created radiation damage [Ref. 4]. No direct impact on hysteresis effects is observed.



(a)



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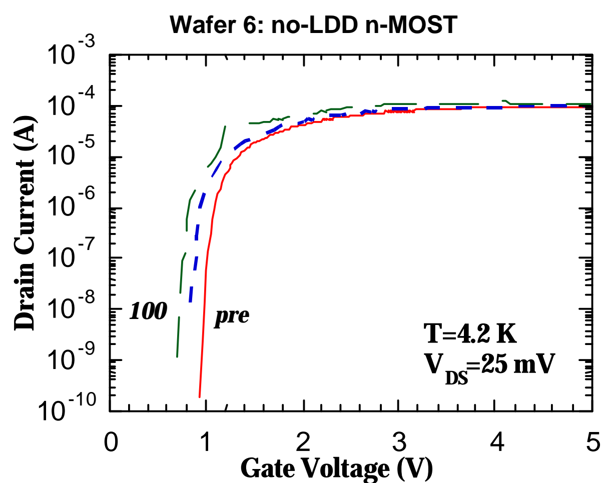

(c)

Figure 5. *Input characteristics at 4.2 K of a 10 μmx5 μm g-irradiated p-MOSFET at 4.2 K of split 1 with LDD (a) and split 6 no-LDD (b), and of a no-LDD n-MOSFET of split 6 (c).*

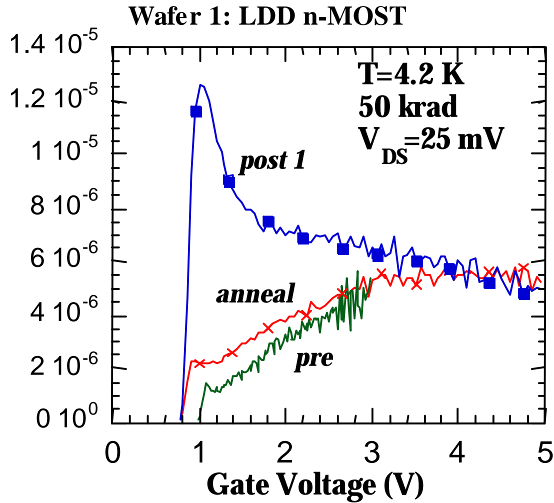

Figure 6. *Impact of room temperature annealing on the linear transconductance of a 10 μmx5 μm n-MOSFET, after a total dose of 50 krad(SiO_2).*

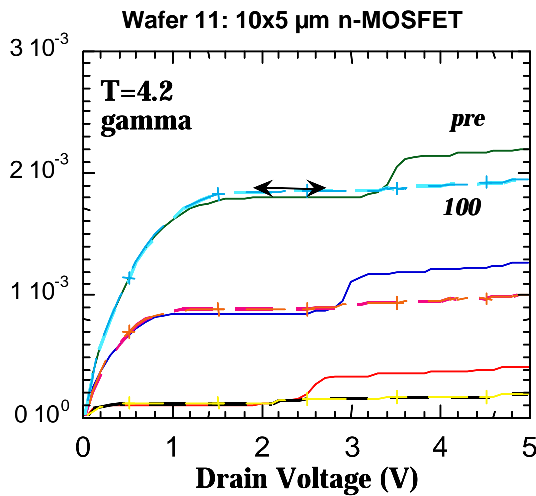

Figure 7: *Output characteristics of an γ-irradiated 10x5 μm n-MOST (process wafer 11) at 4.2 K, corresponding to a dose of 100 krad(SiO_2). Both the Low-High and High-Low curves after γ-exposure are shown.*

In order to further investigate the impact of irradiation on the kink effect, it is useful to study the substrate current (I_B) characteristics as a function of the drain bias, for example [Ref. 5]. The results of figure 8, obtained for a no-well and no-LDD circular n-MOSFET before and after exposure to 50 krad(SiO_2) γ's perfectly illustrates a few interesting features. One can clearly see that for low V_{DS} the substrate current becomes smaller after irradiation, while the opposite is true for higher V_{DS}. This points to a radiation-induced reduction of the carrier multiplication near the drain, on the one hand, and to a lowering of the p-well series resistance, on the other hand, since no levelling off of the I_B characteristic is seen post-irradiation.

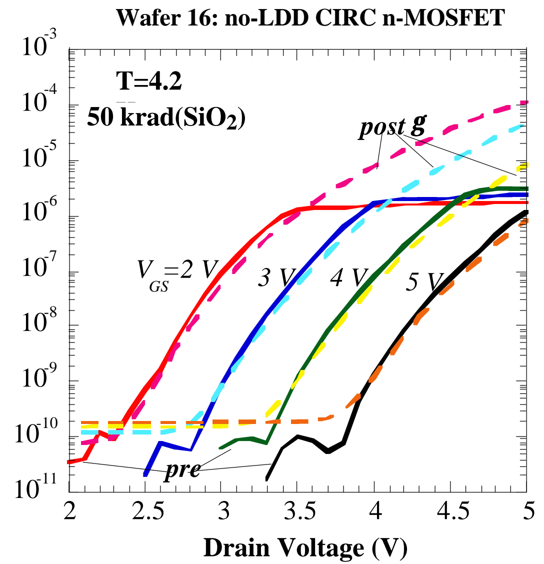

Figure 8. *Substrate current (absolute value) of a circular no-well/no-LDD n-MOSFET before (full lines) and after a 50 krad(SiO_2) irradiation (dashed lines), corresponding with different gate voltages.*

5. TESTING CONSIDERATIONS

It is essential to remark that the reported irradiation investigations have been performed at room temperature. While for displacement damage studies this represents a kind of worst case situation, this is surely not the case for total dose irradiations. Operation at 77 K prevents the trapped holes first of all to move towards the negative interface and secondly to escape (tunnel), to recombine, to annihilate or to be transformed into interface traps. Therefore it is expected that the degradation of the field and eventually also of the gate oxide will be more pronounced during low-temperature irradiations. Although some information can be found in the literature for 77 K irradiations [Refs 16,17], this is hardly the case for irradiations at liquid helium temperatures. Therefore it is very important for the FIRST mission also to have access to cryogenic irradiations. The main problem with the cryogenic irradiations are related to the following aspects:

1) the irradiations have to be performed while the devices are cooled and biased. This may cause some hardware configuration problems. There are not many irradiation facilities offering this option, and
2) the device and circuits have to be kept at cryogenic temperature until the post-irradiation characterization has been completed. This implies that one either needs access to test facilities near the irradiation place or that one has to transport the devices in a cooled Dewar. The latter may cause some problems with the safety regulations.

While cryogenic irradiations are especially needed for total dose effects, the γ-irradiations are also the most affected by room temperature annealing.

In the discussion of the pre-irradiation optimization, the problems related to determine the series resistance were

discussed. However, also other static device parameters are not that straightforward to measure at cryogenic temperatures. Comparing the different popular techniques for the V_T extraction [Ref. 7], it turns out that the so-called double-derivative method [Ref. 18] offers the most robust solution at low temperatures. It can cope with a broad range of device architectures and measurement conditions [Ref. 19]. The technique is furthermore quite insensitive to series resistance effects, which is particularly important for LDD type of devices. In the double derivative method, the second derivative of the drain current I_{DS} is plotted versus the gate bias (linear operation). The threshold voltage is defined as the gate bias where a peak occurs in the second derivative of the drain current I_D.

An important type of measurement is the input or I_D-V_{GS} measurement at a constant drain bias V_{DS}. This enables to extract key device parameters like V_T, the subthreshold slope S or the maximum transconductance g_{mmax}. A first important factor is the choice of V_{DS} in the linear region. In order for the physics and the ohmic equations to be applicable, the device has to be biased for a V_{DS} which is substantially smaller than the saturation value V_{DSAT}. While at room temperature a typical value is 100 mV, this could be at the high (non-linear) side for 77 or 4.2 K operation. As a rule, one should compare the applied V_{DS} with the thermal voltage kT/q (q the elementary charge). Therefore, a value of 10 (maximum 25) mV seems to be more appropriate, for 4.2 K measurements. One drawback of using a small V_{DS} is that the drain current transients become longer that way [Ref. 20], so that it may take some time before the device reaches equilibrium. The occurrence of transient effects can cause a change of V_T with time. One possibility is to cool down a biased device so that the steady-state situation is frozen. However, changing the gate bias inevitably breaks the steady state so that this is not really a solution. In order to average out the transient effects at 4.2 K, one can use a long integration time (parameter analyzer). It is also recommended to repeat the same measurement a few times to check the stability/repeatability of the results. As a compromise, one can use a somewhat higher V_{DS} value compared with what would be ideal for true linear operation at 4.2 K, e.g. 10 or 25 mV.

6. DESIGN CONSIDERATIONS

There are a number of well established design techniques for improving the radiation hardness of CMOS technologies. These include the use of closed geometry devices or of guard rings. It has been demonstrated in the past that these techniques are also successful for low temperature operation [Refs 16-17]. Maybe more specific for cryogenic electronics, is the use of cascode transistors. This is a transistor consisting of two parts in series with a common contact, preferably left floating. It helps in reducing the kink effect. This has for example been shown convincingly for partially depleted (PD) SOI transistors operating in the so-called twin-gate mode [Ref. 21]. Not only the drain current kink is removed, but also the associated low frequency (LF) noise overshoot [Ref. 22]. It has furthermore been demonstrated that the noise margins of SOI inverters improve drastically for twin-gate structures [Ref. 23]. This design concept has a good potential for analogue applications.

7. CONCLUSIONS

In summary, it can be stated that the development, design and characterization of spaceborn cryogenic electronics brings about specific problems, requiring a dedicated approach. For instance, it is crucial to optimise the used test methodology. From a processing viewpoint the cryogenic performance has to be optimised and some built-in hardening should be realised for space applications. Although so far only room temperature irradiation has been studied, it is crucial to perform irradiation and in-situ testing at cryogenic temperature as well. Especially for total dose effects, the cryogenic irradiations are a worst case. Keeping the present limitations into account, some processing guidelines have been formulated, which in our view are recommended for achieving successful 4.2 K circuit development. This implies the use of no-LLD devices, processed in a p-well for the n-MOSFETs and making use of the appropriate threshold voltage adjustment implantation. In some cases irradiation has a beneficial impact on the electrical device performance, including some phenomena which need more in-depth studies in order to come to a physical modeling.

8. ACKNOWLEDGEMENTS

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