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SUBSTRATE CURRENT AND KINK ANALYSIS OF MOSFETs AT LIQUID HELIUM TEMPERATURE

E. Simoen*, C. Claeys*'** and A. Mohammadzadeh***

*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

** also at EE Dept., KU. Leuven, Kard. Mercierlaan 94, B-3001 Leuven, Belgium

***ESTEC-ESA, Keplerlaan 1, NL-2200 AG Noordwijk, The Netherlands

ABSTRACT

A simple method is proposed to analyse the substrate current characteristics of MOSFETs operated at liquid helium temperatures. The key feature is to determine experimentally the saturation drain voltage V_{DSAT}, which is next substituted in the standard model for the multiplication current. The technique is applied and validated on n-MOSFETs fabricated in a dedicated cryogenic 0.7 µm CMOS technology. The impact of certain technology splits and of radiation damage on the substrate-current and kink characteristics is discussed and some guidelines for optimising the cryo-performance of submicron CMOS are formulated.

1. INTRODUCTION

One of the critical issues in cryogenic CMOS intended for operation in the liquid helium temperature (LHT) range is the occurrence of carrier multiplication near the drain, for sufficiently large drain bias V_{DS}. This generates a number of undesired features and artifacts, like the kink effect in the drain current I_D (e.g. figure 1), the flow of the substrate current I_B through the bulk of the device (figure 2), drain current transients and hysteresis and a significant increase in the low-frequency noise (Ref. 1). This implies that a correct analysis and modeling of these phenomena is of strong practical importance. Furthermore, a dedicated approach is required, since standard analysis techniques successful at higher temperatures often fail in the LHT regime. Here, a simple method is proposed to analyse the multiplication-current generation at 4.2 K. The method will be applied to devices fabricated in different processing splits, both before and after irradiation. This enables to study the impact of the device architecture and processing on the kink effect.

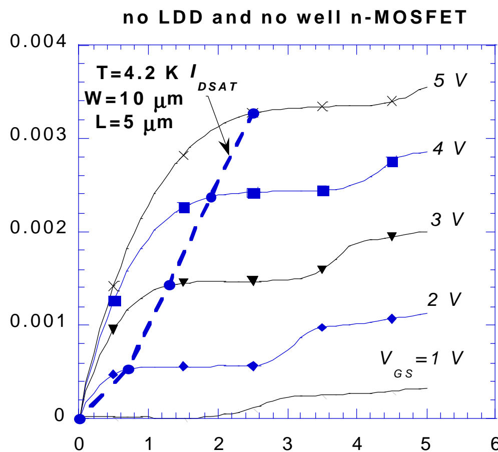

Figure 1. *Output characteristics at 4.2 K of a 10 µmx5 µm no well/no LDD n-MOSFET. Also shown is a dashed line connecting the saturation drain current I_{DSAT} points.*

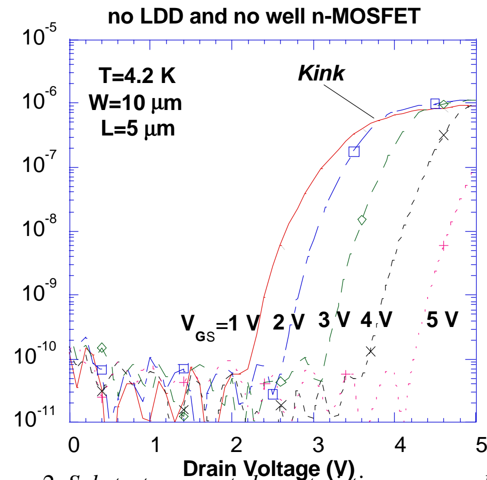

Figure 2. *Substrate current characteristic corresponding to the device of figure. 1. Also indicated is the "kink" in the I_B curves.*

2. EXPERIMENTAL

The devices have been processed in a modified 0.7 µm CMOS technology at ALCATEL-Microelectronics and serve as test structures for the prototype cryogenic read-out electronic circuits for ESA's FIRST mission. The gate oxide thickness is 16 nm and a polysilicon-buffered LOCal Oxidation of Silicon (PBL) is used for device isolation. Beside the standard technology developed for room temperature operation, splits have been fabricated to investigate the role of the presence of the Lowly-Doped Drain (LDD) and of the p-well on the performance at LHT. Here, results will be presented of regular structure W(idth)xL(ength)=10 µmx5 µm n-MOSFETs.

Pre- and post-rad testing has been performed on dual-in-line packaged devices, mounted in a sample-holder which was immersed directly in the liquid helium. Standard input drain current – gate voltage (I_D-V_{GS}) and output drain current – drain voltage (I_D-V_{DS}) characteristics have been recorded. In the latter case, both low-to-high (LH) and high-to-low (HL) sweep directions were applied in order to investigate possible hysteresis/transients in the channel current.

The 61 MeV proton irradiations were performed at the Cyclone facility in Louvain-la-Neuve (Belgium), in the fluence range of $3x10^{10}$ cm^{-2} up to 10^{12} cm^{-2} and a flux of 10^8 $cm^{-2}s^{-1}$. This is certainly more than expected for the entire lifetime of the FIRST mission. A gate bias of +5 V was applied to the gate of the n-MOSFETs while the other terminals (source, drain, p-well) were grounded. The ^{60}Co γ-irradiations were also performed in Louvain-la-Neuve, for total dose of 50 and 100 krad(SiO_2) and the same bias conditions. Post irradiation measurements took place within 24 h of the exposures. The irradiation temperature was 300 K.

3. ANALYSIS METHOD

It has been demonstrated in the past that in first order, the room-temperature model for the multiplication current I_M holds down to liquid helium temperatures (Refs. 1-6). In this model, the multiplication factor $M=-I_B/[I_D+I_B]$ obeys the following semi-empirical law:

$$M/[V_{DS}-V_{DSAT} \quad {}_{DS}-V_{DSAT}$$

with V_{DSAT} the saturation drain voltage, corresponding to the

channel. A and B are semi-empirical multiplication coefficients which will be discussed below. It is assumed $_B$=I . In other words, the measured (collected) substrate current is equal to the multiplication current

demonstrated previously (Ref. 7), this may not be the case at LHT for high V , when the collected substrate current levels off and, hence, shows the kink, indicated in figure 2. In this

swept to the source junction, so that I_B $_M$.

$$1/V_{DSAT} \quad 1/(V_{GS}-V_T) + 1/(E_cL_{eff}) \qquad (2)$$

with V_T the threshold voltage, L_{eff} the effective device length and E_c the critical electric field for velocity saturation. In principle, it is easy to obtain V_{DSAT} from equation (2), once V_T and L_{eff} are known. The critical field is in the order of a few times 10^4 V/cm at 300 K and reduces with temperature (Ref. 4). In practice, however, other methods are used to derive V_{DSAT} from measured output characteristics. One way is based on the substrate current and consists of constructing curves of constant M (Ref. 2). As can be derived from equation (1), the curve running through the origin corresponds with M=0 and $V_{DS}=V_{DSAT}$. While this technique works quite well in the liquid nitrogen temperature range, some problems might occur at 4.2 K, especially for somewhat higher M values. Due to the occurrence of the 'kink' effect in the I_B characteristic erroneous results may be obtained.

The method proposed here is based on the observation that the onset of the drain current kink should equally follow the V_{DSAT} at each V_{GS}, in first instance. This has been noted before (Ref. 9) and can also be inferred from figure 1 for example, where a more or less constant distance is seen between the I_{DSAT} curve and the start of the drain current kink at different gate bias. In order to more clearly define the drain voltage corresponding to the start of the kink, defined as V_{Dkink} here, it is proposed to analyse the output conductance g_D, equal to the derivative of I_D with respect to V_{DS} (I_D/V_{DS}). In fact, a similar type of method, using the output resistance has been proposed before to determine V_{DSAT} in Silicon-on-Insulator MOSFETs (Ref. 10). V_{Dkink} is obtained from the point where g_D starts to increase after the saturation plateau, as shown in figure 3. Note also the hysteresis in the output characteristics, which is present in the ohmic, the initial saturation and the kink region. For high enough V_{DS}, no hysteresis is observed, in agreement with previous reports (Refs. 11-13). Generally, the HL g_D curves are more smooth than the LH ones and allow a more straightforward determination of V_{Dkink}. The latter is represented in figure 4 for different gate biases. The corresponding drain current I_{Dkink} is read from the output curves of figure 1 for example.

In order to derive V_{DSAT} at each V_{GS}, the shift of the I_{Dkink}-V_{Dkink} curve of figure 4 with respect to the origin is determined. This is done by a quadratic fit to the experimental data of figure 4. The crossing point with the x-axis I_{Dkink}=0 defines V_{DS0}. Finally, V_{DSAT} is obtained from:

$$V_{DSAT}(V_{GS}) = V_{Dkink}-V_{DS0} \qquad (3)$$

and I_{DSAT} is the drain current corresponding with each V_{DSAT}.

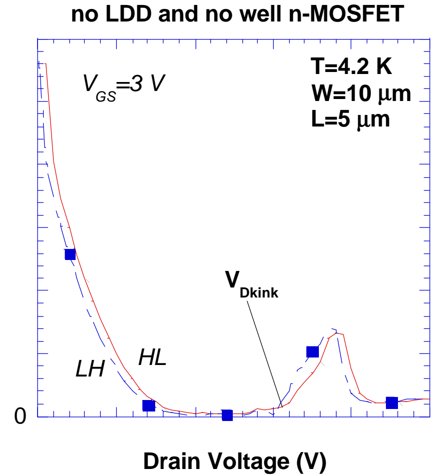

Figure 3. *Channel conductance at V_{GS}=3 V and T=4.2 K of a 10 μmx5 μm n-MOSFET. Both LH and HL curves are shown, representing the hysteresis in the characteristics.*

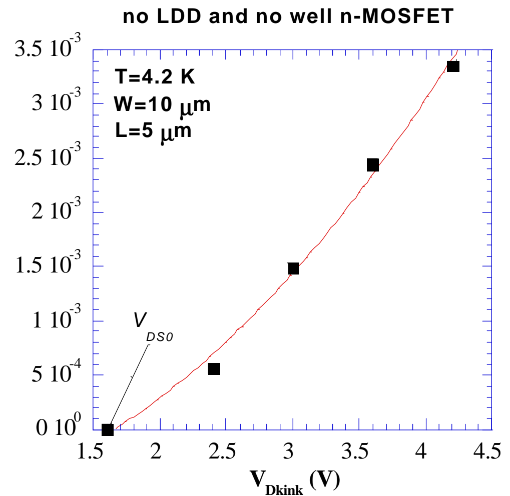

Figure 4. *I_{Dkink}-V_{Dkink} data points corresponding to the characteristics of figure 1. A quadratic fit is used to obtain the kink position at zero gate voltage V_{DS0}.*

From the above, it is clear that for the proposed method to be applicable, it is necessary that M is approximately constant at the onset of the kink. This requires that the gate biase range is not too large. Table I shows that in this particular case, M 2 to $2.5x10^{-7}$. Note that this value is well below the onset of a kink effect in the substrate current (figure 5). Another important point is that the accuracy of V_{Dkink} will be determined by the V_{DS} step used in measuring the output curves. Here it was 0.1 V. However, too small a step will enhance the noise of the measurements, leading to an additional source of errors. It is

believed, therefore, that there exists an optimal measurement procedure to determine V_{DSAT} in this way. The assumption of a quadratic behaviour of equation (1) neglects 3rd and higher order terms in the expansion of the exponential on the right-hand side.

Finally, using the experimental V_{DSAT} of table I, the normalised multiplication factor of the left-hand side of equation (1) can be derived, yielding the result of figure 5. The corresponding A and B coefficients are summarised in table II.

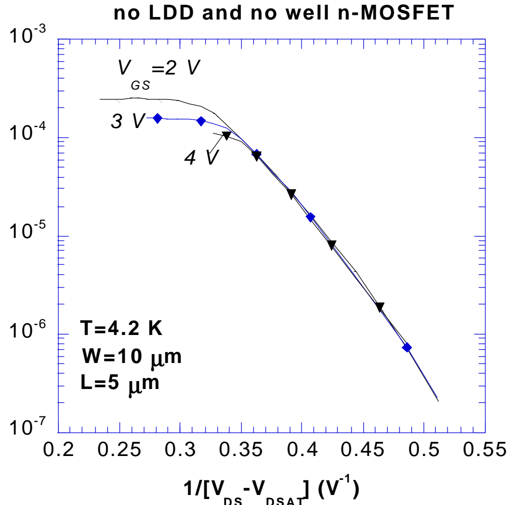

Figure 5. *Multiplication factor divided by V_{DS}-V_{DSAT} for three gate voltages and corresponding to the device of figure 1.*

Table I. *Experimental V_{Dkink}, V_{DSAT} and M values for the 10 mmx5 mm n-MOSFET of figure 1, corresponding with different V_{GS}.*
bd: below detection/noise limit

V_{GS} (V)	V_{Dkink} (V)	V_{DSAT} (V)	M ($x10^{-7}$)
2	2.4	0.74	bd
3	3.0	1.74	bd
4	3.6	1.94	1.8
5	4.2	2.54	2.6

Table II. *A and B coefficients at different V_{GS} for an LDD and a no LDD 10 mmx5 mm n-MOSFET at 4.2 K.*

V_{GS} (V)	A_{no} (V)	B_{no} (V^{-1})	A_{LDD} (V)	B_{LDD} (V^{-1})
2	37.3	67	36.5	5.3
3	37.4	74	37.3	7.6
4	35.8	30	36.2	6.6

4. APPLICATIONS

4.1. Impact of technology

In this section, the impact of the technology splits on the kink and substrate current behaviour at 4.2 K will be reported. As can be seen from table II, the A coefficient for the no well and no LDD n-MOSFET of figure 1 is about 36-37 V for V_{GS}=2 to 4 V, while B is on the order of 30 to 70 V^{-1}. The larger spread in the B values is related to the exponential fitting procedure: a small (i.e. 5 %) change in the slope leads to a drastic change in the experimental intercept.

Figure 6 compares the output curves for a 10 μmx5 μm n-MOSFET with and without LDD. While the transistor without LDD shows a pronounced kink in the drain current, a significant reduction is observed for the device with LDD. This illustrates the reduction of hot-carrier effects at LHT by the presence of the LDD, which aims at lowering the maximal field at the drain-substrate junction. However, as is also clear from figure 6, LDD devices show a lower drive current and a higher series resistance, which is derived from the lower drain current in the ohmic region (Refs. 14-16).

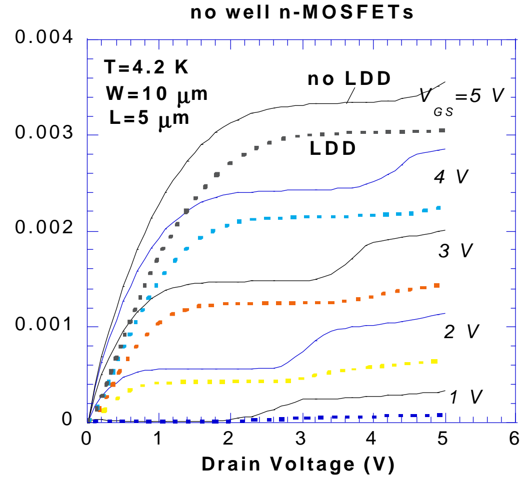

Figure 6. *Output characteristics at 4.2 K of a 10 mmx5 mm n-MOSFET with (dots) and without (full lines) LDD.*

The effect of the presence of a p-well is more complicated, as evidenced by figure 7. There is still a marked kink effect, indicating similar multiplication current. On the one hand, it is expected that M is enhanced for the same operation bias for an n-MOSFET in a well, since the maximum field at the drain junction is higher for a higher substrate doping. However, since the p-well is only moderately doped, freeze-out will occur, cancelling partly this effect. A second factor playing is the series resistance along the path of the substrate current (Ref. 7). For the same collected I_B, the potential drop V_{sub} across R_{series} will be larger, the larger the drain to pwell-contact resistance becomes. This will determine both the onset and the end of the kink region. Initially, the flow of the multiplication-generated holes towards the p-well contact will enhance V_{sub} and lower the threshold voltage V_T. The higher R_{series} is, the sooner the increase of V_{sub} will start to affect the channel current. The rather abrupt end of the kink at LHT is related to the turn-on of the source/p-well diode. Once part of the holes can be collected by the source, the substrate potential will be pinned at about the band-gap energy of 1.17 eV, due to the steep I-V characteristic of a p-n junction at 4.2 K (Refs. 7, 17).

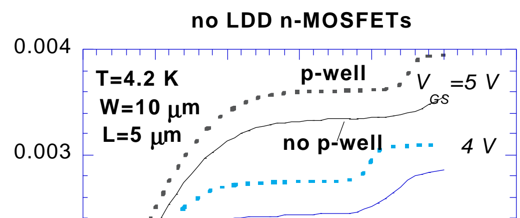

Figure 7. *Output characteristics at 4.2 K of a 10 μmx5 μm n-MOSFET with (dots) and without (full lines) p-well.*

The combined effect of p-well and LDD is shown in figure 8, yielding a marginal kink at all V_{GS}. However, if the characteristics at 1 V would be enlarged, a kink is still discernable. This becomes more clear when plotting the output conductance versus V_{DS}, where still an increase of g_D is seen. It also implies that the method is applicable to cases where only a moderate to weak kink is observed. It should also be remarked that the normalised kink amplitude is generally largest for gate voltages close to V_T. This is at the same time the operation regime of the FIRST amplifier and read-out electronics, so that a control of the kink effect is of crucial importance in order to keep good circuit linearity.

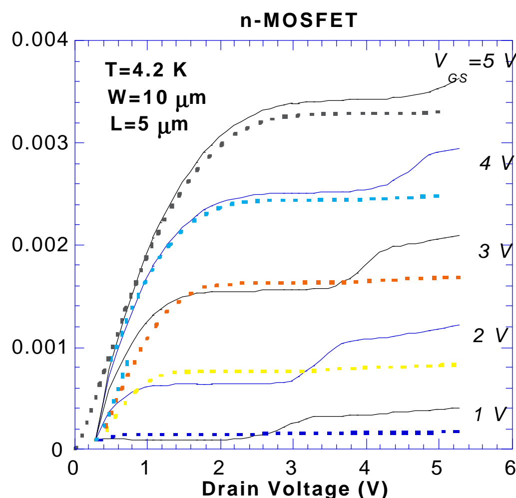

Figure 8. Output characteristics at 4.2 K of a 10 μmx5 μm n-MOSFET with (dots) and without (full lines) LDD and p-well.

Figure 9 summarises the substrate current characteristics at V_{GS}=2 and 3 V for some of the splits studied, while figure 10 shows the reduction of the M factor due to the presence of the LDD region at V_{GS}=2 V. According to the data of table II, it is in first instance the B pre-factor which is reduced and not A. This also follows from the nearly parallel shift of the curves in figure 10. The reduction of the B coefficient seen here is roughly one decade, suggesting a substantial lowering of the maximum field near the drain junction.

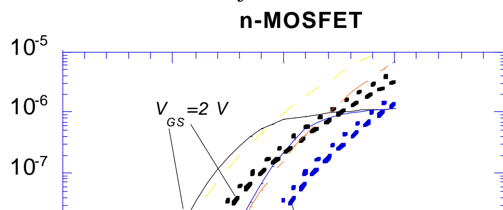

Figure 9. *Substrate current at V_{GS}=2 and 3 V as a function of V_{DS} for the different splits studied.*

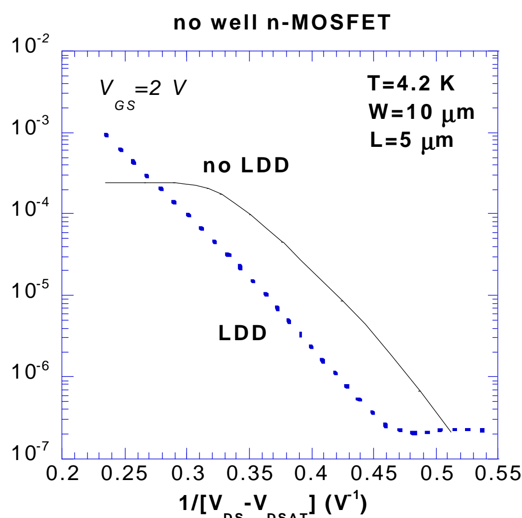

Figure 10. *Normalised multiplication factor versus 1/[V_{DS}-V_{DSAT}] for an LDD and a no LDD n-MOSFET at 4.2 K and V_{GS}=2 V.*

4.2 Impact of irradiation

For cryogenic space applications, the radiation response and hardness is a critical issue. An obvious question is whether exposure to total-dose or high-energy particle irradiation will aggravate the kink performance as well. Fortunately, despite of the change/degradation of the static device parameters like the V_T and the transconductance, it turns out that the kink effect is 'cured' upon irradiation (Refs. 15,18-19). An example of this effect is shown in figures 11 and 12, for a 61 MeV proton and a 100 krad(SiO_2) γ-ray irradiation, respectively. A pronounced reduction of the kink is observed in these figures, even for the LDD-less devices, suffering from severe kink before exposure.

In order to understand this behaviour, one can apply the same analysis as before irradiation (Ref. 18). A typical example of the normalised M factor is represented in figure 13, showing that irradiation results in a lowering of the carrier multiplication for the same 1/[V_{DS}-V_{DSAT}]. Similar as in the case of an LDD MOSFET, this could point to a lowering of

the maximum electric field near the drain junction. However, as illustrated by the data of table III, not only the B prefactor is lowered after irradiation, but also the A coefficient (e.g. compare with the no LDD results of table II). This is particularly pronounced for the proton irradiation. As shown elsewhere, this could be interpreted as resulting from an enhancement of the carrier mean free path due to the creation of radiation damage in the transistors (Ref. 18). More work is ongoing to differentiate between the role of ionisation and displacement damage to this phenomenon. The fact that in figure 13 no leveling off occurs after irradiation, indicates that the R_{series} has been modified for instance by a radiation-induced change in the active dopant density at 4.2 K. In addition, these results should be compared with irradiations at LHT in order to clarify the role of room-temperature damage annealing.

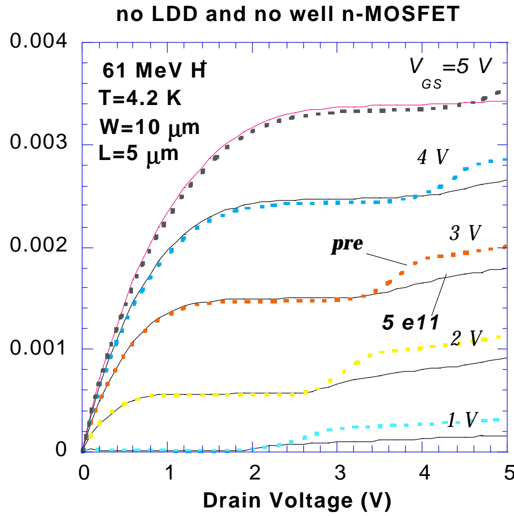

Figure 11. *Output characteristics of a 10 mmx5 mm n-MOSFET at 4.2 K before and after a 61 MeV proton irradiation*

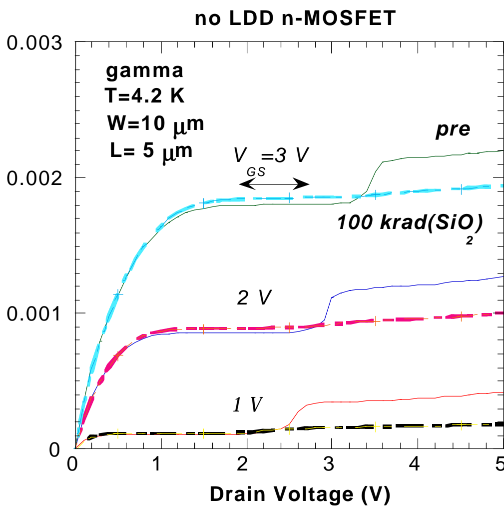

Figure 12. *Output characteristics of a LDD-less 10 mmx5 mm n-MOSFET at 4.2 K before (full lines) and after a 100 krad(SiO_2) g-irradiation.The double arrow indicates HL and LH curves, showing marginal hysteresis.*

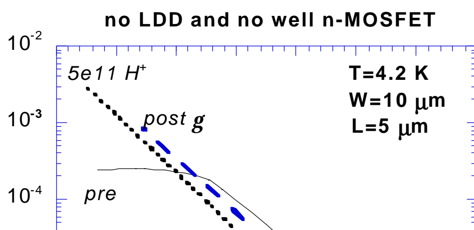

Figure 13. *Impact of high-energy proton or g-irradiation on the multiplication factor of an LDD-less n-MOSFET, at 4.2 K and V_{GS}=2 V.*

Table III. *A and B coefficients for a LDD and well-less 10 mmx5 mm n-MOSFET at 4.2 K and different V_{GS}. The results are for a g-dose of 100 krad(SiO_2) and for a proton fluence of $5x10^{11}$ cm^{-2}.*

V_{GS} (V)	A_γ (V)	B_γ (V^{-1})	A_H (V)	B_H (V^{-1})
2	33.4	7.8	30.7	4.9
3	35.2	13.5	31.2	5.9
4	32.5	8.1	31.7	7.1
5	--	--	33.6	4.4

5. CONCLUSIONS

In summary, a comprehensive and straightforward technique has been proposed to determine V_{DSAT} in the LHT range, based on the kink effect. In fact, as shown above, the technique yields reliable results even for n-MOSFETs without pronounced kink, as long as the output conductance shows an increase with the drain bias. It can for example be extended to the V_{DSAT} analysis of partially depleted SOI MOSFETs.

The method has been applied to a series of different n-MOSFETs corresponding to different processing splits. The role of the LDD in suppressing the kink has been highlighted. At the same time, it was demonstrated that high-energy irradiation typical for a space environment reduces the kink effect. Therefore, it is felt that the presence of an LDD is not strictly necessary to warrant succesful cryogenic operation of space-born cryo-CMOS read-out electronics. This simplifies the processing and reduces the production cost significantly.

6. ACKNOWLEDGEMENTS

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