

Short-channel radiation effect in 60 MeV proton irradiated 0.13 μm CMOS transistors

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Abstract

Introduction. A nice side-effect of CMOS scaling is that the technology becomes harder for every new generation (see e.g. Ref 1 and references therein). This observation is related to the thickness reduction of both the gate and isolation dielectric layers, rendering them less susceptible to ionising damage. The recent COTS approach for space electronics benefits largely from this scaling hardening effect, as it opens the door for the use of standard microelectronic components in the space radiation environment. However, at the current stage of technology development, thin thermal oxide (SiO_2) is running out of steam as a gate dielectric and should, therefore, be replaced by more reliable alternatives like nitrided (NO) or reoxidised nitrided oxides (RNO). At the same time, the classical LOCOS-based isolation is replaced by Shallow Trench Isolation (STI), allowing a further reduction of the device pitch. According to the literature, NO and RNO oxides offer a better resistance against radiation [1-2]. On the other hand, non-optimised STI could show up significant Total-Ionisation Dose (TID) degradation [3-5]. Therefore, a certain amount of radiation testing of state-of-the-art CMOS still seems to be recommended, in order to assess potential problem areas. In this paper, the impact of a 60 MeV proton irradiation on the static characteristics of 0.13 μm CMOS transistors with STI will be reported and discussed in view of previous results obtained on the 0.18 μm generation [6-7]. It will be shown that overall, the 0.13 μm technology is hard in the fluence range studied. However, a length-dependent degradation of the static device parameters has been noted, similar as for the 0.18 μm transistors, whereby the shortest channels suffer the largest changes, both for n- and p-MOSFETs. Some impact of the gate dielectric will also be reported. Finally, the mechanism responsible for the damage will be discussed.

Experimental. The devices studied have been processed in a 0.13 μm CMOS technology with STI. Some of the salient features are summarised in Table I. Both Highly Doped Drains (HDD) and Lowly Doped Drains (LDD) have been implanted, while the wells have a retrograde character. The HALO (or pocket) implantation serves to control the short-channel effects (SCE) [8]. Two wafer splits have been studied: with a 2 nm NO (wafer 7) and RNO (wafer 9) gate oxide. N- and p-channel devices with various polysilicon gate lengths, ranging from $L_{\text{poly}}=0.08$ till 10 μm have been mounted in 24 pins DIL; the width $W=10 \mu\text{m}$.

Biased irradiations were performed at the Cyclone facility in Louvain-la-Neuve; details of the 60 MeV exposures are summarised in Table II. The gate bias V_G was limited to the nominal supply voltage of the technology. The maximum gate and drain bias during pre- and post radiation testing was also limited to 1.5 V (absolute value) in order to avoid stressing of the devices. The threshold voltage V_T and the maximum transconductance G_{max} were derived from the linear input characteristics. The series resistance R_s and ΔL have been derived from a modified Shift and Ratio (S&R) method [9], using a 1 μm reference transistor.

Results. As can be seen from Fig. 1, the normalised threshold voltage of the NO n-MOSFETs increases after proton irradiation, for lengths below 0.2 μm for a fluence of $1 \times 10^{11} \text{ p/cm}^2$ and for all lengths for $5 \times 10^{11} \text{ p/cm}^2$. The maximum relative shift, however, is limited to about 4 % and does not increase with the proton fluence. A more or less similar picture is valid for the maximum transconductance ratio of Fig. 2: G_{max} increases up to 15 % for the shortest n-MOSFETs, for both fluences studied, while a negligible degradation is found for the long channel devices. The simultaneous increase of V_T and of G_{max} for proton-irradiated n-MOSFETs is a rather unusual combination, which points to a degradation mechanism which differs from the classical ionisation damage at the Si-SiO₂ interface.

The RNO n-MOSFETs show a slightly different behaviour, as evidenced by Figs 3 and 4. While the fluence of 10^{11} p/cm^2 seems to have only a marginal effect on the static parameters, a more pronounced degradation is found for the larger fluence. This time, a cross-over behaviour is observed for the V_T , which has been reported before for 0.18 μm n-MOSFETs [6-7]. In other words the V_T increases after irradiation for the shorter devices, while it reduces for the longer ones. Again, this is accompanied by an increase of G_{max} , which amounts to about 20 % for the shortest L (Fig. 4).

The NO p-MOSFETs of Fig. 5 and 6 show a qualitatively similar behaviour as their n-channel counterparts (Figs 1 and 2), although the changes are less pronounced, particularly for G_{max} . A similar conclusion is drawn

for the RNO p-type transistors. It has finally been observed that after proton exposure, the effective length is better aligned to the theoretical expectations than before (Fig. 7), while a reduction of the series resistance has been noted, which is more pronounced for the long channels (Fig. 8). A possible degradation model should thus account for the concurrent increase of G_{\max} and V_T and the reduction of R_s . Of course, a reduction of R_s will normally lead to an increase of G_{\max} , so that both phenomena may be coupled. It should also be remarked that no changes in the gate current, i.e., no Radiation-Induced Leakage Current (RILC) was observed.

Discussion. In order to explain the observations, additional analysis has been performed both on mounted (i.e. biased) and non-mounted (unbiased) irradiated devices. From Fig. 9, it is clear that no degradation is observed in the subthreshold characteristics. This points to the fact that no measurable hole trapping or interface-state formation occurs in the NO or RNO gate dielectric. Further evidence is provided by high-frequency C-V measurements on MOS capacitors and by low-frequency noise spectroscopy showing no changes within the sensitivity of the techniques. Only after some time, an increased gate-induced drain leakage current develops, while the rest of the characteristics remains fairly stable (Fig. 10). Studies on devices with a fixed $L=10\ \mu\text{m}$ and variable width demonstrate that the STI used is radiation hard, so that the degradation of the edge regions can also be ruled out.

So far, the degradation mechanism is obscure, although it is speculated that it could be related to a change in the lateral doping profile. It is known that the dependence of the V_T on the length is a sensitive function of the HALO doping profile. Doping density changes could be produced by e.g. displacement damage (the interaction with created interstitials and vacancies). In favor of this argument is the fact that γ -irradiations do not generate any observable degradation. Device simulations are currently undertaken to substantiate this interpretation. Overall, it is concluded that the $0.13\ \mu\text{m}$ CMOS technology with STI is hard from a viewpoint of space applications.

References

- [1] C. Claeys and E. Simoen, "Radiation Effects in Advanced Semiconductor Materials and Devices", Chapter 6, Springer Verlag (in press, Summer 2002)
- [2] G.J. Dunn, B.J. Gross and C.G. Sodini, "Radiation induced increase in the inversion layer mobility of reoxidized nitrided oxide MOSFETs", *IEEE Trans Electron Devices* **39**, pp. 677-684 (1992).
- [3] M.R. Shaneyfelt, P.E. Dodd, B.L. Draper and R.S. Flores, "Challenges in hardening technologies using shallow-trench isolation", *IEEE Trans. Nucl. Sci.* **45**, pp. 2584-2591 (1998).
- [4] G.U. Youk, P.S. Khare, R.D. Schrimpf, L.W. Massengill and K.F. Galloway, "Radiation-enhanced short channel effects due to multi-dimensional influence from charge at trench isolation oxides", *IEEE Trans Nucl. Sci.* **46**, pp. 1830-1835 (1999).
- [5] F.T. Brady, J.D. Maimon and M.J. Hurt, "A scaleable, radiation hardened shallow trench isolation", *IEEE Trans Nucl. Sci.* **46**, pp. 1836-1840 (1999)
- [6] E. Simoen, J. Hermans, E. Augendre, T. Marescaux, C. Claeys, G. Badenes and A. Mohammadzadeh, "Evidence for short-channel effect in the radiation response of $0.18\ \mu\text{m}$ CMOS transistors", in the *Proc of the RADECS 2000 Workshop*, Louvain-la-Neuve (Belgium), 11-13 Sept. 2000, pp. 25-31
- [7] E. Simoen, J. Hermans, A. Mercha, W. Vereecken, C. Vermoere, C. Claeys, E. Augendre, G. Badenes and A. Mohammadzadeh, "60 MeV proton irradiation effects on NO-annealed and standard-oxide deep submicron MOSFETs", to be published in the *Proc of RADECS 2001*, Grenoble (France), 10-14 Sept. 2001.
- [8] R. Gwoziecki, T. Skotnicki, P. Bouillon and P. Gentil, "Optimization of V_{th} roll off in MOSFETs with advanced channel architecture - retrograde doping and pockets", *IEEE Trans Electron Devices* **46**, pp. 1551-1561 (1999)
- [9] Y. Taur, D.S. Zicherman, D.R. Lombardi, P.J. Restle, C.H. Hsu, H.I. Hanafi, M.R. Wordeman, B. Davari and G.G. Shahidi, "A new "shift and ratio" method for MOSFET channel-length extraction", *IEEE Electron Device Lett* **13**, pp. 267-269 (1992).

Table I. Relevant technological details for the 0.13 μm CMOS technology studied.

Gate oxide thickness:	2 nm
Wafer 7	NO
Wafer 9	RNO
Gate oxidation:	750 $^{\circ}\text{C}$
n- and p-well implantation	
n- and p-LDD and HDD implantation	
n- and p HALO implantation	
Nitride spacer:	80 nm
Silicidation:	Ti/Co (8/12 nm)

Table II. Proton irradiation matrix for the 0.13 μm CMOS components.

Bias:	$V_G=1.5\text{ V}$ All other terminals grounded
Energy:	60 MeV
Flux:	$3 \times 10^8\text{ p/cm}^2\text{ s}$
Fluence:	10^{11} and $5 \times 10^{11}\text{ p/cm}^2$

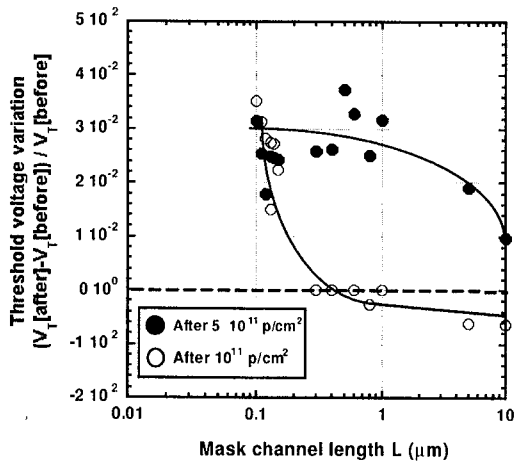


Fig. 1. Normalised threshold voltage versus channel length after a 60 MeV proton irradiation for NO n-MOSFETs.

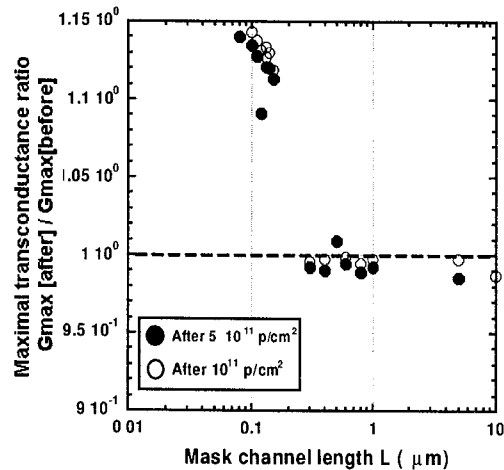


Fig. 2. Maximum transconductance ratio versus channel length after a 60 MeV proton irradiation for NO n-MOSFETs.

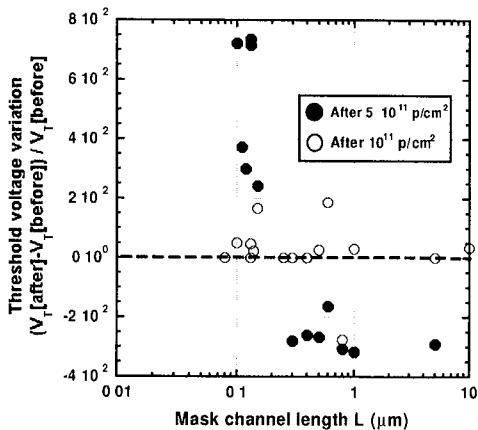


Fig. 3. Normalised threshold voltage versus channel length after a 60 MeV proton irradiation for RNO n-MOSFETs.

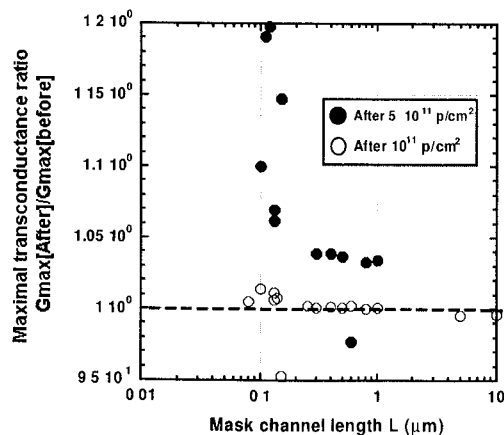


Fig. 4. Maximum transconductance ratio versus channel length after a 60 MeV proton irradiation for RNO n-MOSFETs.

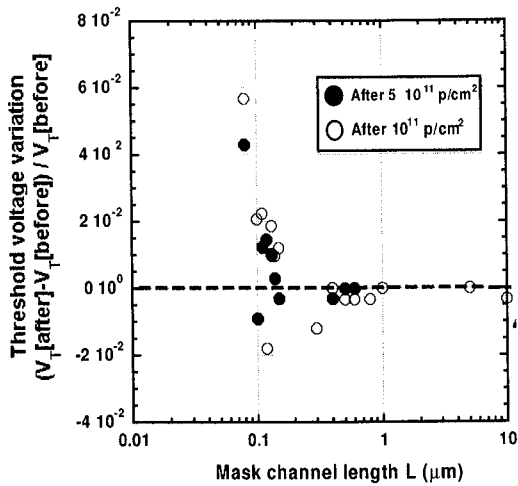


Fig. 5. Normalised threshold voltage versus channel length after a 60 MeV proton irradiation for NO p-MOSFETs.

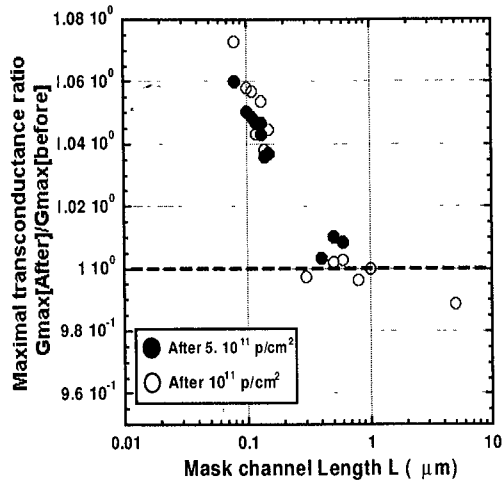


Fig. 6. Maximum transconductance ratio versus channel length after a 60 MeV proton irradiation for NO p-MOSFETs.

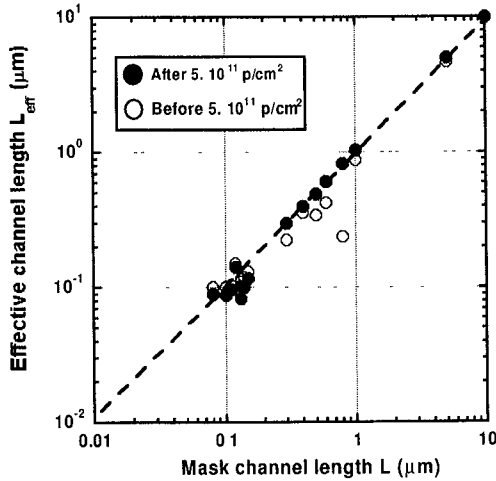


Fig. 7. Effective channel length versus polysilicon gate length after a 60 MeV proton irradiation for NO n-MOSFETs.

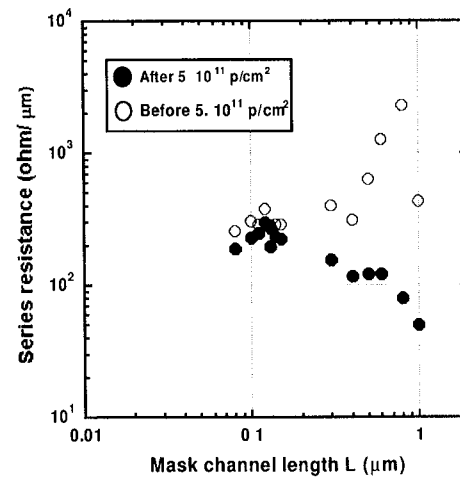


Fig. 8. Series resistance versus channel length after a 60 MeV proton irradiation for NO n-MOSFETs.

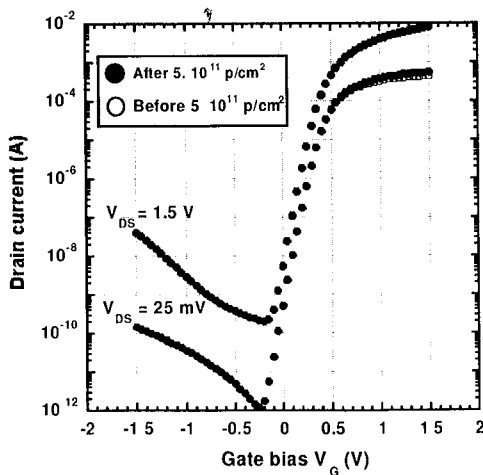


Fig. 9. Variation of the drain current versus the gate bias in linear and saturation regimes for a $L=0.13 \mu\text{m}$ NO n-MOSFET after 60 MeV proton irradiation.

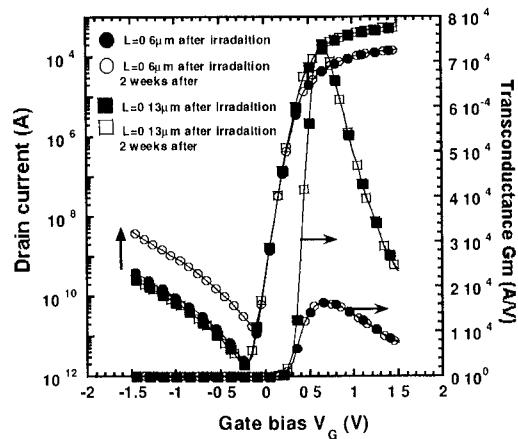


Fig. 10. Variation of the drain current and the transconductance before and after irradiation versus the gate bias in linear regime for an RNO n-MOSFET with $L=0.13 \mu\text{m}$ and $L=0.6 \mu\text{m}$.