Heavy Ion Characterization of SEU Mitigation Methods for the Virtex FPGA

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***Abstract*-- This work presents the results from Heavy Ion tests of Xilinx Virtex FPGA XQVR300 manufactured by Xilinx in a 0.25µm technology. Virtex XQVR300 is an SRAM-based FPGA, which allows for real-time reconfigurable computing. Reprogrammable logic would offer the benefit of on-orbit design changes. Earlier SEU testing [1] on this type of device has reported high sensitivity to heavy ions. Mitigation techniques of single event upsets in Virtex devices as Triple Module Redundancy (TMR) and configuration readback (bitstream repair) have been developed by Xilinx and are tested in this work.**

***Index Terms*—FPGA, Radiation, Xilinx, Virtex, Single Event Upset, Mitigation**

I. Introduction

The Virtex FPGA is an SRAM based device fabricated on thin-epitaxial silicon wafers using the commercial mask set and the Xilinx 0.25µ CMOS process with 5 metal layers. SEU risks dominate in the use of this technology for most applications in radiation environments. In particular, the reprogrammable nature of the device presents a new sensitivity due to the configuration bitstream. The function of the device is determined when the bitstream is loaded into the device. Changing the bitstream changes the design function. While this provides the benefits of adaptability, it also implies a high risk in terms of SEU in a radiation environment. A device configuration upset may result in a functional upset. User logic can also upset in the same fashion as seen in fixed logic devices. These two upset domains are referred to as configuration upsets and user-logic upsets. Two features of the Virtex architecture can help overcome upset problems. The first is that the configuration bitstream can be read back from the part while in operation, allowing continuous monitoring for an upset in the configuration and the part supports partial reconfiguration, which allows for real-time SEU correction.

Secondly, the high density and rich architecture allow resource redundancy to be economically implemented in order to filter out SEU effects.

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II. Experimental

A. Test Vehicle

Heavy Ion tests were performed on two Xilinx Virtex XQVR300 prototype devices, delivered by Xilinx in a 240 pin plastic flat package. The samples were exposed by etching the plastic from the topside down to the chip. Two different designs, named non-TMR and TMR, have been tested in one device each.

1) Non-TMR Design

The non-TMR design, shown in Fig. 1, implements into the Device Under Test (DUT) 14 pipelined shift register each 144 bit long and a small self-test circuit. Individual register bits are build up of the D-type flip-flop inside the CLB module of the Virtex architecture [2]. All together, 32% of the available CLB flip-flop resources in the Virtex device have been used.

The principle of the self test circuit, shown in Fig. 2, is that data are compared with themselves and any mismatch is reported to an output (Error flag). Data consists of 6-bit words taking two different paths in the design before comparison. One path goes through 6 I/O modules of the device and then back to the comparator. The other path goes directly to the comparator. The data are generated by feed back flip-flops register from an external clock signal.

The non-TMR design is a standard design practice without any redundancies or circuits for SEU mitigation.

2) TMR Design

The TMR design, shown in Fig. 3, implements a functionally equivalent circuitry as the non-TMR design but with full internal Triple Module Redundancy (TMR). 95% of available flip-flop resources are used. The outputs of the TMR design use triple tri-state drivers to filter data errors from the output.

The TMR version uses the triple module redundancy design techniques that Xilinx recommends for use with the Virtex FPGA. It uses the same design rules as have been used in SEU tests performed at the Los Alamos National Laboratory [3].

B. Test Methods

At Saab Ericsson Space special test equipment has been developed for SEU testing of FPGAs. The general concept is to load data into the DUT, pause for a pre-set time and thereafter read data and check for errors. New data are loaded into the DUT at the same time as the old data are read out. All this is repeated continuously during irradiation. The DUT is tested in static operation using a long time pause and in dynamic operation by setting the time pause to zero.

A flow chart of the test sequence is given in Fig. 4. Any detected errors will be stored in FIFOs, and the DUT will be loaded with new data again. The cycle will then be repeated. Failing read/write operations from/to the DUT will determine the functionality. The clock speed is variable up to 5 MHz. Error Data are serially transferred from the FIFO to a PC where data are analysed. For each DUT, errors can be traced down to logic module, logic value and position.

1) Test Boards

The test system consist of two boards, one Controller board managing the test sequence and the serial interface to the PC and one DUT-board housing two Devices Under Test (DUT). A schematic drawing is given in Fig. 5.

The Controller board tests one DUT at a time using a "virtual golden chip" test method. The principle of the test technique is to compare each output from the DUT with the correct data stored in SRAM's, the "virtual golden chip". The DUT is continually cycled while the outputs of the selected 14 shift registers are compared with the "virtual golden chip". When an error is detected (when outputs do not match), the state of all outputs and position in cycle of the failing shift register will be temporarily stored in FIFOs. Data in the FIFOs is continually sent to a PC through a RS232 serial interface. After each test run the data are analysed and stored in a database by the controlling PC.

The configuration controller chip on the DUT-board is controlling the PROM and configuration ports of the DUT. A program command can be sent to the DUT, which clears its configuration memory and starts an automatic re-configuration of the DUT from the PROM. During the test of the DUT the configuration controller is continuously scrubbing the DUT configuration memory with new configuration data from the PROM's.

All data from the PROM's to the DUT is transferred through the parallel SelectMAP interface, which supports the partial configuration feature making it possible to continuously scrub the device with new configuration data during operation.

2) Classification of SEU Errors

Detected errors out from the DUT could originate from SEU in registers (user-logic flip-flop) of the device, in the configuration data causing functional errors in parts of the device and in control registers of the device causing global functional errors. The analysed data errors are separated into three different domains, SEU in registers, SEU in configuration data, and SEU in device control registers.

a) User-Logic Upsets

SEU in the user logic registers are corrected with new data loaded into the registers in connection with each read cycle. The data are analysed for single bit errors and categorised into the following error types:

FF(0-1) Read '1' from flip-flop registers when '0' is expected.

FF(1-0) Read '0' from flip-flop registers when '1' is expected.

FF Total sum of all FF errors (above) read from the shift registers.

DataSwap This error showed up as two bit errors in registers next to each other. First a '0' was read when '1' was expected and in the next register a '1' is read when a '0' was expected. It is only observed in this order. The error was not persistent in the next test cycle. No explanation has been found for this error signature.

b) Configuration Upsets

SEU in the configuration data will remain until the configuration data are corrected with new configuration data. Errors that are caused by SEU in the configuration are quantified by observing the following signatures in the test data:

Routing An SEU in the configuration logic (routing bits and lookup tables) may cause errors in the configured function of the operational device. This gives errors from the shift registers that are permanent until next time the device is scrubbed with new configuration data.

Persistent A persistent error is a permanent error that can not be corrected with new configuration data. The device needs to be reset and completely reinitialised. This is the result of SEU in "weak keeper" circuits used in the Virtex architecture when logical constants are implied in the configured design such as unused clock enable signals for registers.

SelfTest SelfTest errors are of the same kind as the routing error, but instead of interrupting a shift register it interrupts the function of the SelfTest module. This will be detected on the "Error flag" of the SeltTest module.

c) SEU in Device Control Registers

SEFI error With a SEFI error the function of the whole device is interrupted in one hit and all shift register data are lost. The device requires a reset and complete reconfiguration for correction.

Xilinx believe this to be SEU in the POR register in the control registers of the architecture. An upset in one specific bit in the POR register may start a re-initialisation of the whole device.

3) Other Test Considerations

The test system is optimised for SEU testing of the user-logic. Data are clocked in and out and then paused for a pre-set time, giving the radiation time to upset the registers, before reading out the data. Every upset in the tested registers (FF, DataSwap) will be detected. The test frequency is comparative low, which means that user logic is tested in a static manner. A dynamic test at higher frequencies would be needed to detect possible transients propagating in the internal logic.

An SEU in configuration data causing a functional error is corrected when new configuration data are written to the DUT. To be able to detect all of these errors the DUT must be continuously tested. Since the DUT is paused in our tests we will not see all of these errors (Routing, SelfTest). Therefore we have estimated the fraction of errors detected. (Detection factor). Two different pause times (time where DUT is not clocked between read/write of data) are used during the tests, 223ms and 4ms. The time to scrub the DUT with configuration data was 10,38ms. For the longer pause time only $10{,}38ms/223ms \approx 0{,}05$ of all scrub cycles are tested. 50% of the errors in these scrub cycles will be detected. This gives a detection factor of 0,025. For the shorter pause time, all scrub cycles are tested but still $50\% of (4ms/10{,}38ms) \approx 0{,}2$ of all upsets will be corrected before they are detected. The detection factor will be $(1-0{,}2) = 0{,}8$. Testing the non-TMR design mostly used the long pause time since the flow of error data otherwise became too high for the system to handle.

III. Results

Two test samples with the two designs were irradiated with a variety of atomic species covering effective LET values from 2.97 MeV·cm^2/mg to 34 MeV·cm^2/mg.

Each test run was performed up to a fluence of 10^6 ions/cm^2, or until either all 14 shift registers were permanently disabled by the "Persistent" errors or eliminated by the "SEFI" error. With this error in a shift register no data came out and the registers couldn't be tested. The device required to be re-initialised before starting a new test run.

A. Non-TMR Design

1) Configuration Upsets

At a LET of 2.97 MeV·cm^2/mg each type of configuration error was observed. Cross-sections are presented in Fig. 6. The presented data for all configuration errors are correlated with the estimated "detection factor" (see paragraph II-B-3).

The cross section is specific for this design. To predict cross section for a 100% utilised device you must multiply these cross sections with the utilisation factor for this design (about 32% for the routing errors and maybe 5% for the SelfTest module).

2) User-Logic Upsets

At a LET of 2.97 MeV·cm^2/mg only two errors were recorded after two test runs. Both errors were of the FF(0-1) type. Dataswap and all FF errors were observed at a LET greater than 2.97 MeV·cm^2/mg with a saturation cross-section of about 10^6 cm^2. The results are presented in Fig. 7.

The Dataswap error stands for 25% of all user logic register errors.

B. TMR Design

1) Configuration Upsets

With the exception of one test run, the SEFI error was the only observable error. The SEFI was observed from a LET of 5.85 MeV·cm^2/mg. This demonstrated that the TMR design method effectively eliminated all non-SEFI configuration induced errors.

The SEFI error is believed to be an SEU in the POR control register, clearing the whole device from configuration data. All I/Os are 3-stated in this state and this was detected at the read out data, which slowly went from read high state to read low state after some test cycles.

In one test run the "Routing" error was observed. The flux was ~1333 ions/cm^2/s and the device were scrubbed with new configuration data every 10,38ms. This gives a flux/scrub-cycle ratio of 13,8 ions/cm^2/scrub. With a too high flux/scrub-cycle ratio we have an increased risk to have errors in two modules at the same time, which could give error in the majority voting circuit. From the tests on the Non-TMR data we know the cross-section for a "Routing" error in one module and can calculate the mean number of errors/scrub-cycle for the test run. With the assumption that the errors are randomly spread in time, the Poisson distribution may be used to predict the probability to have two "Routing" errors within the same scrub-cycle. The probability that these two errors in the TMR design shall occur in the same tripled shift register, is $1/14 * 2/3$. With this statistics, we would detect 1,8 errors in this specific test run, we detected one. Therefore, the observed "routing" error is most likely an artifact of the flux/scrub-cycle ratio. With a 10 times lower flux/scrub-cycle ratio the same statistics predicts that 100 times less errors would be detected.

2) User-Logic Upsets

Only one FF error was observed at a LET of 14.1 MeV·cm^2/mg with an estimated cross section of ~$5 \cdot 10^{-10}$ cm^2. No other FF errors were recorded in absence of a SEFI error. The FF error was recorded in the same test run as the "Routing" error was recorded and it is considered that this error is the result of the flux/scrub-cycle ratio as previously mentioned.

IV. Conclusion

The SRAM based cells are sensitive to SEUs down to low LET values. With a module redundant design in combination with fast correction of configuration data, the majority of all observed errors could be corrected. Errors in the control registers of the device cannot be corrected. The experimental data for upsets in control register part of the Virtex devices are summarised in Fig. 10. It is expected that with the recommended SEU mitigation methods, the SEFI error rate represent the complete error rate for the Virtex device in orbit. Since the control registers are identical in each Virtex family member, this SEFI error rate applies to any Virtex device size without dependency on resource utilisation by the configured design.

References

[1] E. Fuller, M. Caffrey, P. Blain, C. Carmichael, N. Khalsa and A. Salazar, “Radiation test results of the Virtex FPGA and ZBT SRAM for space based reconfigurable computing.,” MAPLD 1999 Proceedings, C2, Sep. 1999.

[2] Xilinx Product Specification, *Virtex™ 2.5 V field programmable gate arrays*, DS003-2 (v2.6), Jul. 2001

[3] E. Fuller, M. Caffrey, A. Salazar, C. Carmichael and J. Fabula, “Radiation characterization, and SEU mitigation, of the Virtex FPGA for space based reconfigurable computing,” presemted at NSREC 2000 conference, Oct 2000.

[4] C. Carmichael, E. Fuller, P. Blain and M. Caffrey, “SEU mitigation techniques for Virtex FPGAs in space applications,” MAPLD 1999 Proceedings, B2A, Sep. 1999.

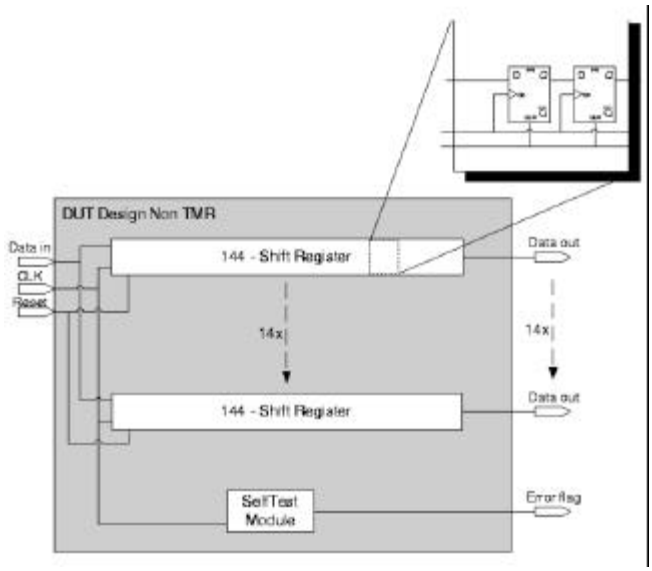

Fig. 1 Schematic drawing of part used for functional test in the Non-TMR DUT design.

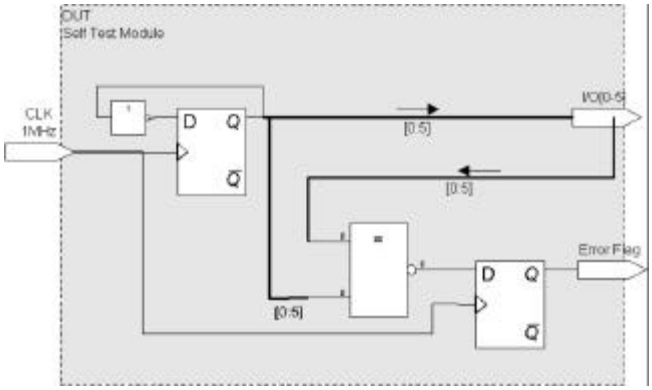

Fig. 2 Schematic drawing of SelfTest module

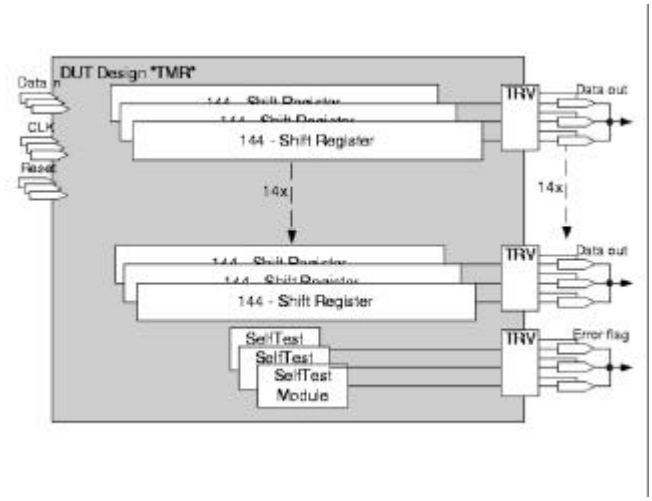

Fig. 3 Schematic drawing of TMR DUT design

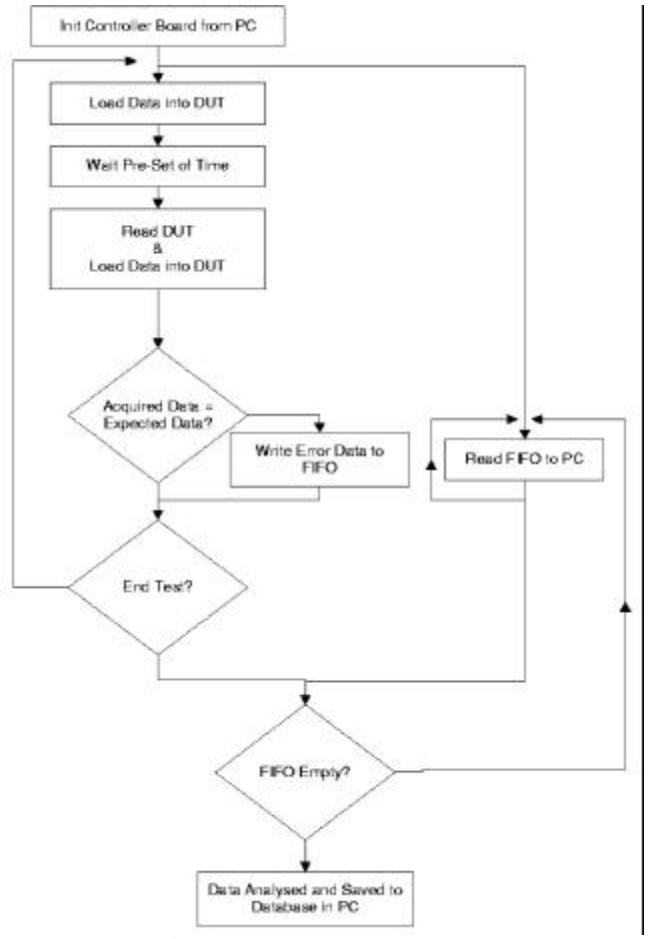

Fig. 4 Flow chart of the test sequence.

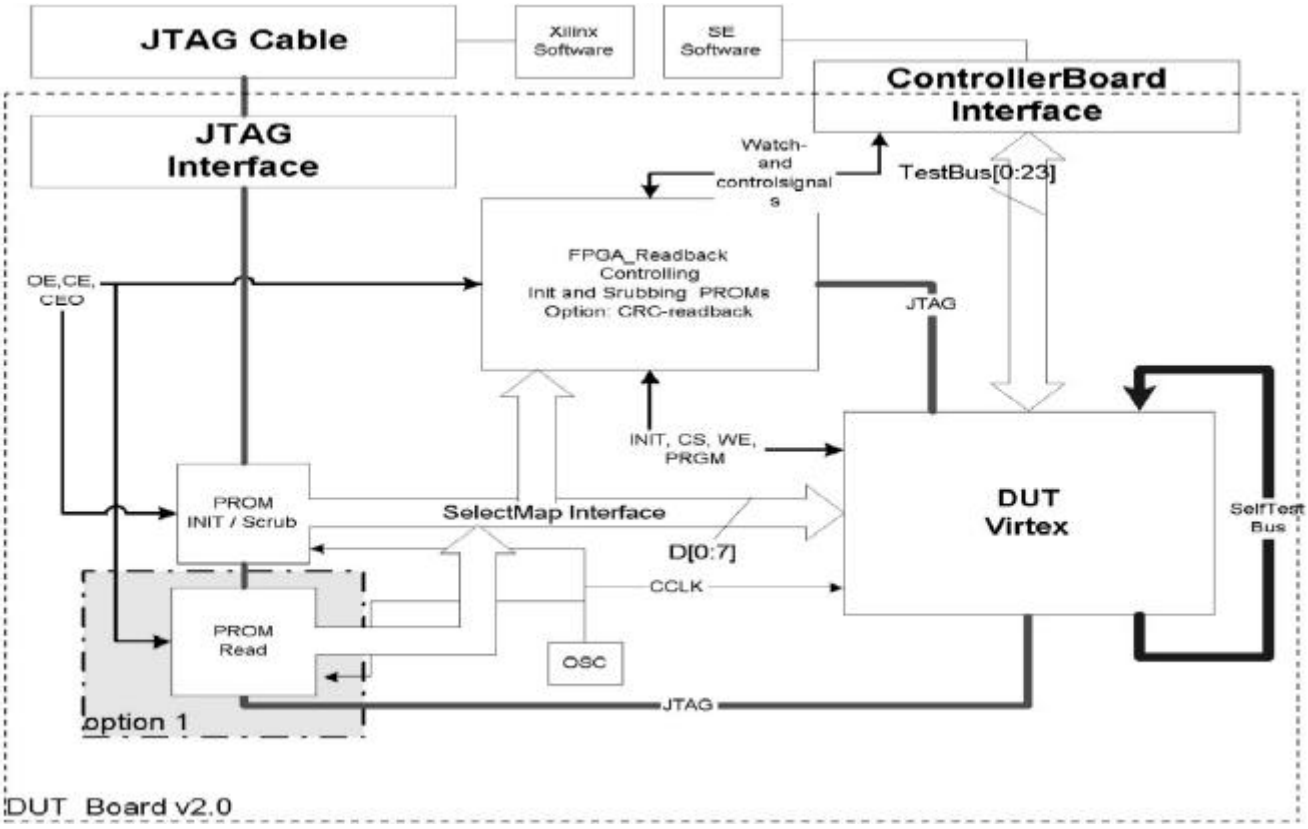

Fig. 5 Schematic drawing of DUT board with configuration interface for the Virtex device.

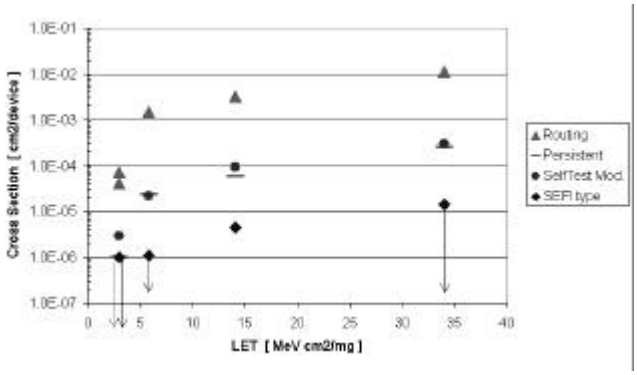

Fig. 6 Configuration errors for non-TMR Design. The cross sections are per device and are specific for this design. For the non-TMR design only one SEFI error was recorded, at a LET of 14.1 MeV·cm^2/mg. Arrows indicate test without any upsets.

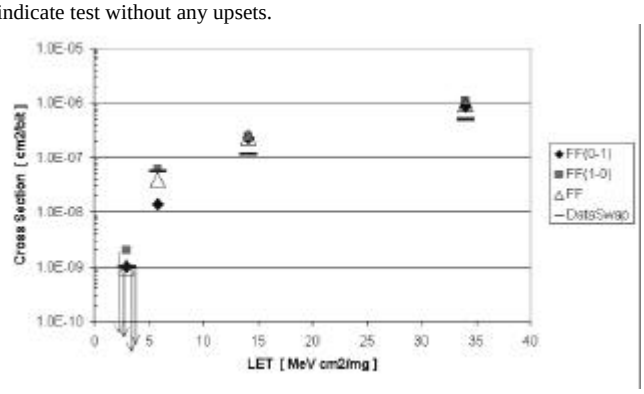

Fig. 7 User-logic errors for non-TMR Design. Arrows indicate test without any upsets.

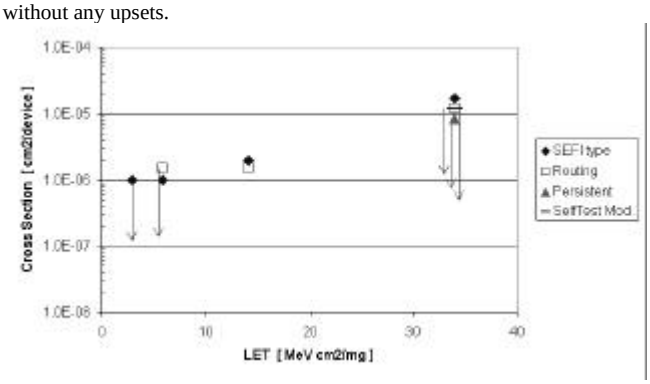

Fig. 8 Configuration errors for TMR Design. Except for SEFI errors only one "routing" error was recorded at a LET of 14.1 MeV·cm^2/mg. Arrows indicate test without any upsets.

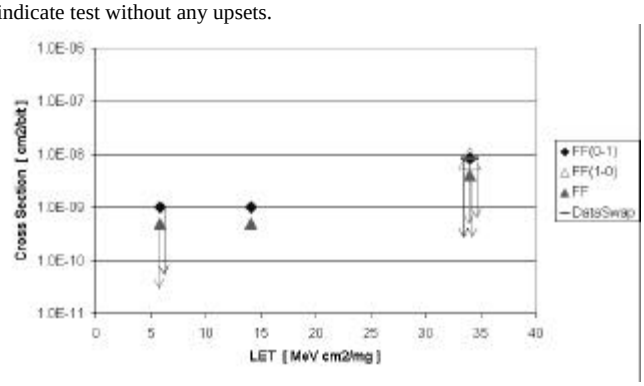

Fig. 9 User-logic errors of TMR Design. The only recorded error was a FF(0-1) error at a LET of 14.1 MeV·cm^2/mg. Arrows indicate test without any upsets.

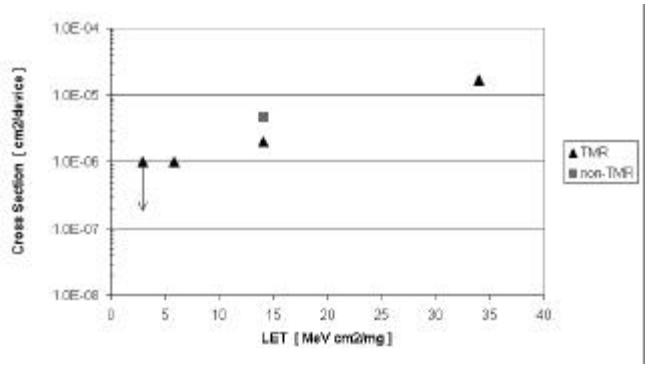

Fig. 10 SEFI errors for non-TMR and TMR design. The non-TMR tests were performed to less fluence than the TMR, therefor less SEFI errors have been observed for non-TMR design. In principal the SEFI error cross section should be the same for the two designs. With the assumption that the control registers have the same heavy ion sensitivity as the user registers (Fig. 6), the number of fatal failure control bits of the device seem to be around ten.