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# MODELLING CMOS RADIATION TOLERANCE IN THE HIGH-DOSE RANGE (MODELISATION DE LA TOLERANCE DE COMPOSANTS CMOS POUR LES FORTES DOSES)

Andrew Holmes-Siedle, *Centre for Radiation Damage Studies, Brunel University of West London*

Palle Christensen, *Risø National Labs, Roskilde, Denmark*

Leonard Adams, *European Space Agency, ESTEC, The Netherlands*

Claudia-Christina Seifert, *Siemens KWU, Offenbach, Germany*

## ABSTRACT

This paper refines a "four-lane" physical model for CMOS devices, first published in 1994. The growth of threshold voltage as a function of radiation dose in a very wide range of Complementary Metal-Oxide-Semiconductor (CMOS) devices, all the way from low (kilorad) to very high (gigarad) doses. The parameters of four **LANE-LIKE OR CORRIDOR-LIKE REGIONS** on the growth curve diagram are extracted. The resulting **FOUR-LANE CLASSIFICATION** is useful in selecting CMOS technologies and offers a new terminology for describing the radiation tolerance of ICs and could form the basis of a "league table", used to assess the performance of "hardening laboratories" around the world

## 1. INTRODUCTION

Engineers need to know the way in which the threshold voltage of MOS devices grows with dose and anneals with time, especially in the case of complex integrated devices of the complementary type (CMOS). Because of new mission requirements in the nuclear industry and high-energy physics, this need now extends into in the megarad to megagray dose range. Reference 1 (hereafter referred to as "the 1994 publication") was a preliminary classification and physical model for charge buildup and anneal and was an attempt to assist engineers in adapting CMOS technology to circuit and system design the high-dose range. A growing database of measurements on devices in this range has allowed us to build on and refine this model, further classifying devices by such parameters as A, the "hardness" of the oxide, $D_{ro}$ and $V_{ro}$, the point for departure from linear growth of threshold shift etc. The data can be organized so that an engineering model of threshold voltage versus dose can be made from a set of parameters (see e.g. ref. 2). This simple type of model is recommended as a format for classifying a manufacturer's technology and reporting radiation data in future workshops of the IEEE and RADECS.

## 2. PREDICTION MODELS

Prediction models have been developed to deal with threshold voltage shift in MOS devices as a function of dose and electrical stress applied during irradiation. An example of an early simple analysis is reference 3. The user specifies the thickness of the oxide and the location of the trap sheet within it and the electrical field value applied during irradiation. The early model employed a linear dependence of oxide trapped charge density on dose at low dose values, making a transition to a saturated condition at high doses. The result was an analytical method suitable for codifying the behaviour of commercial MOS devices such as simple CMOS logic elements without field oxides (CD4000 series and successors) under laboratory radiation test and the use of this data to predict degradation with time in a radiation environment **at low dose values (1 - 100 krad)**. The 1994 publication added a sublinear buildup of charged interface states to the above and also contained expressions for late or post-irradiation effects, in general following earlier work (e.g. Ref. 4). The result was a model which could be applied over a wider dose range, even up to 100 Mrad, which is now attainable with some ultra-hard technologies (see e.g. Refs 5-7). Although not explicit in the diagrams, the mathematical formulae included in Reference 1 allow dose-rate effects and annealing to be considered. The models all assume that an electric field is present in the oxide (say 1 MV $cm^{-1}$); a method of handling the zero-bias case, is discussed in reference 3, but is not yet included.

Independently, a UC Berkeley group adopted many of the same basic models from the literature in order to construct AGERAD, an adaptation of an ageing/reliability programme named AGE [8]. Since the SPICE programme and time dependence of radiation damage are incorporated in this suite, AGERAD has potential for predicting the performance of complex circuits under given operating conditions and dose rates not covered in test programmes. The

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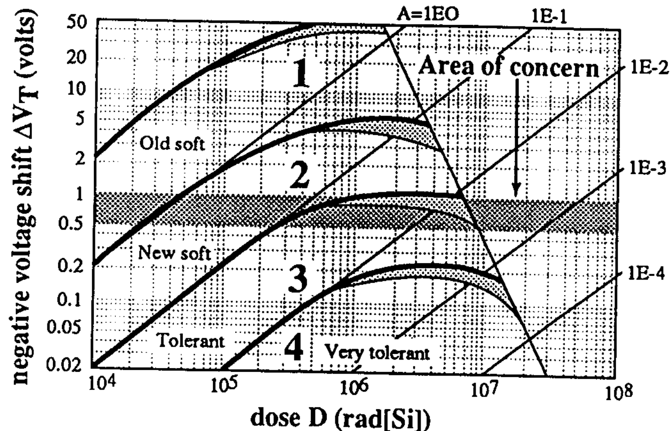


Fig. 1. The FOUR-LANE classification of threshold voltage shifts of **n-channel MOSFETs** into categories of radiation tolerance. Devices are under positive bias during irradiation. Four lane-like or corridor-like regions of radiation sensitivity are shown. The "area of concern" indicates the values at which serious quiescent leakage may occur. The curves exhibit "turnaround" i.e. reversal of direction of shift at high values of dose. The region with hatching bears some uncertainty. The straight guide lines are for oxide charge growth at an oxide thickness of 32 nm with hole trapping probability values, A, ranging from 1 to 1E-4.

four-lane system described here is different, being a classification of technology which uses the same principles. It attempts to make broader statements than AGERAD, which mainly tabulates test data; the four-lane system will, for example, classify a manufacturer's oxide technology in terms of trapping probability, as well as supplying intuitive terms such as "rolloff"(ro) and "turnover"(to).

## 3. THE 4-LANE CHARTS

### 3.1 n-channel MIS structure

Fig. 1 is a "four-lane" $\Delta V_T$ vs D growth chart for n-channel MOSFETs and other MIS structures. The theory behind this model will be found in (1). Four ranges of nMOS technology are defined with respect to radiation tolerance in $\Delta V_T$ vs D space. The oxide fields were defined in (1). To illustrate the simple mathematical analysis, we extract parameters for the curves forming the boundaries of the lanes. The boundary curve between lane 1 and 2 is named "boundary 1&2". For parameterization, we arbitrarily set an oxide thickness of 32 nm, which is convenient mathematically and not untypical of technology of the present era. The responsivity (RA) of a "new soft" oxide is set at $2x10^{-3}$ mV/rad. This is the slope of the curve in its early (i.e. low-dose) part and repesents the trapping, near the $Si/SiO_2$ interface, of every hole generated by the radiation, representing a trapping probability value, A, of unity. This is the ultimate in "softness", not uncommon in commercial oxides. The three other boundary curves represent three decades of improvement in hardness, namely trapping probability values of 0.1, 0.01 and 0.001. The last of these is, probably, the most that can ever be expected from even the most sophisticated oxide process, being the trapping of only one hole in a thousand created. The Lane 1 lies above the line A=1 because the chart must accomodate data from older devices with oxide thickness well above 32 nm (for early CMOS devices, $t_{ox}$ > 100 nm). These are the "Old Soft" group.

### 3.2 p-channel MIS structures

Figure 2 is for p-channel devices irradiated under a negative gate bias, the condition experienced by the pMOS device in a CMOS inverter in a logic "0" state. The shapes of the boundaries are strongly influenced by the tendency of p-channel devices to continue an increase of threshold voltage shift to megagray values (see e.g. 8). The pMOS device is not involved in quiescent leakage so, unlike the case of the nMOS device, an "area of concern" associated with leakage does not appear on the chart. On the other hand, the reduction of switching speed or negative threshold shifts greater than 1V can cause other malfunctions. However, because such malfunctions vary widely with the circuit configuration, we cannot easily state an

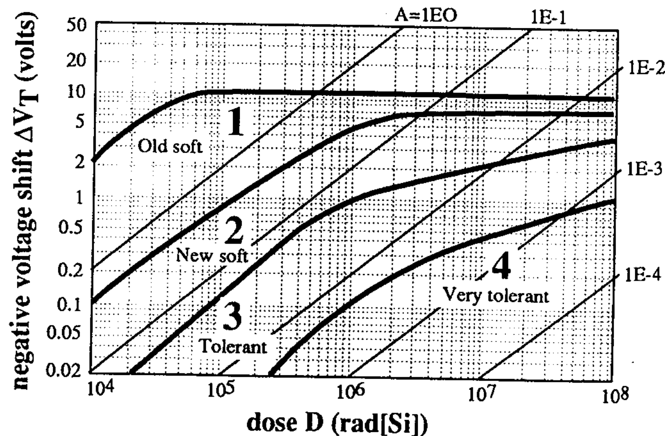


Fig. 2. The FOUR-LANE classification of threshold voltage shifts of **p-channel MOSFETs** into categories of radiation tolerance. Devices are under negative bias during irradiation. Four lanes or corridors of radiation sensitivity are shown. The straight guide lines are explained above

TABLE 1. PARAMETERS OF CURVES FOR n-CHANNEL MIS STRUCTURES IN THE 4-LANE CHART

| name of curve | oxide thickness tox (nm) | response constant RA (mV/rad) | trapping probability (A) | threshold voltage shift at 10 krad (ΔV 10K) | rolloff dose Dro (rad SiO2) | turnover dose Dto (rad SiO2) | rolloff voltage ΔVro (V) | turnover voltage ΔVto (V) | balance dose D bl (rad SiO2) |
|---|---|---|---|---|---|---|---|---|---|
| upper limit | up to 100 | 2.00E-1 | not applicable | 2.0 | 3.0E+4 | 1.0E+6 | 10 | 50 | unknown |
| boundary 1&2 | 32 | 2.00E-2 | 1 | 0.2 | 1.0E+5 | 1.5E+6 | 2.0 | 5.0 | 3.0E7 |
| boundary 2&3 | 32 | 2.00E-3 | 0,1 | 0.02 | 3.0E+5 | 2.5E+6 | 0.5 | 1.2 | 2.5E7 |
| boundary 3&4 | 32 | 2.00E-4 | 0,01 | 0.002 | 1.0E+6 | 4.0E+6 | 0.1 | 0.2 | 1.5E7 |

"area of concern" for the pMOS device. In most circuits, it is the voltage shifts of the nMOS device which are of greatest concern.

### 3.3 Key dose and voltage points

In Figure 3, we see a number of key points on the curves of Fig. 1, using the curve forming the lane boundary between lane 1 and 2 ("bound 1&2"). We indicate the "10 krad point", "rolloff (ro)", "turnover"(to) and "balance (bal)". These are working features which are of intuitive use to engineers in assessing devices for use. In Table 1, we list the co-ordinates of these points for the four boundary curves which divide up the space of the growth chart. Mathematical symbols are defined in Section 6.

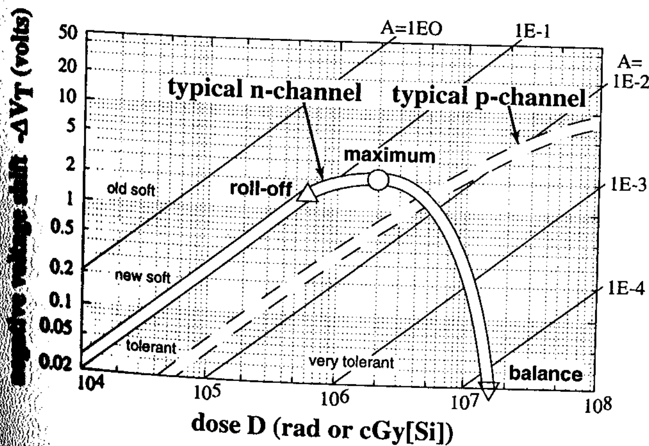


Fig. 3. Comparison of typical n-channel and p-channel FETs with the same oxide trapping properties, respectively biassed negative and positive during irradiation. The straight guide lines are explained above.

The 10-krad voltage value is simply 10,000 times the tabulated responsivity RA. At this dose, the threshold voltage of most positively biassed, new-technology MOSFETs is still responding linearly. The number provides a useful intuitive value for device hardness. At some dose value after this point, the effect of internal fields in the oxide begins to produce recombination of electron-hole pairs, so that the growth curve becomes non-linear, or "rolls off" the straight line on which it began. In Table 2, we tabulate the point at which 5 percent rolloff occurs. These points are seen to be in the 100 krad range for new technologies, implying that we can use simple linear prediction curves up to this point (a useful economy

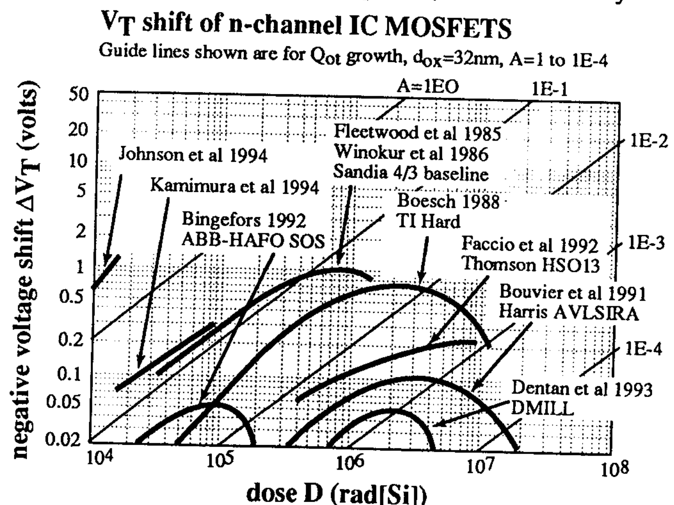


Fig. 4 Experimental growth curves of threshold voltages for n-channel MOSFETs as a function of dose; positive irradiation bias on the gate during irradiation.

TABLE 2. EXPERIMENTAL PARAMETERS OF NMOS ELEMENTS IN CMOS DEVICES

| Process | Ref. | oxide thick ness tox (nm) | RA product RA (mV/rad) | oxide trapping probability A | threshold shift at 10 krad ΔVT (mV) | rolloff dose Dro (rad) | turnover dose Dto (rad) | rolloff voltage ΔVro (V) | turnover voltage ΔVto (V) | balance dose D(bl) (rad) |
|---|---|---|---|---|---|---|---|---|---|---|
| Sandia baseline | 9 | 32 | 3.0E-3 | 0.145 | 28 | 2.0E5 | 7.0E5 | 0.60 | 0.93 | unknown |
| Texas Instrum. | 11 | 32 | 7.0E-4 | 0.027 | 7 | 9.0E5 | 2.0E6 | 0.90 | 0.7 | 1.8E7 |
| Harris AVLSIRA | 7 | 24 | 7.5E-5 | 0.0032 | 0.75 | 1.3E6 | 3.0E6 | 0.09 | 0.124 | 1.8E7 |
| ABB-HAFO | 10 | 32 | 9.0E-4 | 0.0398 | 9 | 4.0E4 | 9.0E4 | 0.03 | 0.052 | 2.0E5 |
| Thomson HSOI3 | 5 | 24 | 1.5E-4 | 0.0068 | 1.5 | 7.0E5 | unknown | 0.12 | 0.255 | unknown |
| D-MILL | 6 | 24 | 3.5E-5 | 0.0016 | 0.35 | 1.5E6 | 2.0E6 | 0.05 | 0.045 | 4.5E6 |

for many space projects). The voltage at which rolloff occurs in the four cases is greatly different and the theoretical significance of this empirical rule (with respect to oxide recombination kinetics etc) has yet to be assessed.

The internal field in the oxide falls continually as the oxide trapped charge builds up. The logical end to this process is that the field disappears, leading to complete recombination of all radiation-induced hole-electron pairs and, as a result, the saturation of the radiation-induced charge $Q_{ot}$ and the resulting shift, $\Delta V_{ot}$. The tabulated points $\Delta V_{to}$ are linked to this physical event but the dose values do not correspond exactly to its occurrence because, alongside the development of $Q_{ot}$ is the development of oppositely-charged interface trapped charge, $Q_{it}$. The presence of this charge offsets the maximum slightly on the dose and voltage scales.

The value of $\Delta V_T$ starts falling after turnover because, although oxide charge growth has saturated, the buildup of interface states has not. The latter, hitherto not very significant, begins to control the growth curve. Within as little as a decade of dose, the device has returned to its original value of threshold voltage. We call this the "balance point" because the quantities $Q_{ot}$ and $Q_{it}$ are roughly in balance. In the definition, we choose a point slightly before perfect balance, since zero does not appear on a logarithmic voltage scale.

An important point to notice is that, in the "boundary 3&4" curves, the maximum occurs at a voltage value well below the as-processed threshold voltage values for nMOS transistors used in ICs. This represents the "secret of hardness" of some CMOS processes. The threshold voltage value never reaches the "area of concern" at which severe quiescent leakage occurs. That is, such a technology is "hard" to this form of failure up to an infinite value of dose. The "secret" lies in the ability to produce the correct relative amounts of $Q_{ot}$ and $Q_{it}$ at key points on the dose scale. This can be done by trial and error, once the process engineers understands the requirement.

3.4 Analytical treatment and predictions

The physics of effects involved in the model - the buildup of oxide trapped charge and interface trapped charge - lead us to choose a fitting equation containing two terms:

$$\Delta V_T = L[1 - \exp(-MD)] - ND^{2/3}$$

The first expression saturates as the oxide trapped charge should do and the second is sublinear, as the interface state growth is often found to be. The value of the exponent of 2/3 is an assumption which may be allowed to change from 0.5 to 1 in certain cases. The constant M may be altered to fit oxide thickness, bias and time dependence. Table 3 lists the constants L, M and N for the four

TABLE 3. ANALYSIS OF THE CURVES IN THE 4-LANE CHART (N-CHANNEL) USING THE FORMULA $\Delta V_T = L[1 - \exp(MD)] - ND^{0.67}$

| curve number | L | M | N |
|---|---|---|---|
| upper limit | 60 | 4.0E-3 | 1.3E-2 |
| boundary 1&2 | 5.0 | 4.0E-4 | 1.4E-3 |
| boundary 2&3 | 1.3 | 4.0E-4 | 1.3E-4 |
| boundary 3&4 | 0.75 | 4.0E-4 | 1.0E-5 |

boundary curves in Figure 1. We have explained that, in n-channel oxides the second term, negative interface trapped charge, eventually overtakes the first term,leading to the characteristic turnover and balance points in the curves. Table 1 lists the values for the above parameters as extracted from the four curves of Figure 1. The values of rolloff and turnover dose are seen to rise with the degree of tolerance of the oxide, while the value of the corresponding voltages decreases. These parameters are useful quantitative expressions of the radiation tolerance of real devices in the high-dose region.

In the analytical expressions given in Appendix A, we include the time dependence terms for oxide trapped charge and late interface trapped charge. In the treatment above, these are set to zero (i.e. annealing is not considered).

In Fig. 4, we show growth curves for n-channel devices [5-7] [9-11]. These range from soft to very hard technologies. The parameters L, M and N for these curves are given in Table 4.

All curves except that for the data of Bingefors follow the "lane discipline" of our model. The reason for the deviation of the Bingefors curve is reflected in the small value of the constant L (related to oxide charge growth) relative to N, which is related to interface charge growth. It appears that, in this Swedish process, the oxide charge growth is extremely small, rather than the interface state response is untypically large. It is found that the terms L and RA bear a smooth relation, implying that a high rate of charge trapping also leads to a high saturation value. This, in turn gives rise to the lane-like structures of Figures 1 and 2.

3.6 PSPICE parameters

A pragmatic approximation for most integrated-circuit n-channel and p-channel MOSFETs is the following:

$\Delta V_T$ = RAD for $0 < D < D_{ro}$

$\Delta V_T = \Delta V_{To}\,[1 - \exp(-RAD)/\Delta V_{To})]$,

for $D_{ro} < D < D_{to}$

$\Delta V_T = \Delta V_{To}$ - (+)$k2D^{2/3}$

for $D > D_{max}$ (+ sign for p-channel)

In earlier work, the authors simulated the degradation of simple analogue and digital circuits with the PSPICE programme and created approximate equations for logic switching voltages as a function of dose as found in the 4-lane chart. This form of simulation is also performed in the work of Pavan et al [8]. The present authors used the rough approximation for PSPICE simulation:

$$\Delta V_T = \Delta V_{To}[1-\exp(-RAD)/\Delta V_{To})] - (+)\,k2D^{2/3}$$

3.7 Limitations and reservations

The charts constitute
(i) a graphical method of classifying n-and p-channel MOS devices
(ii) a graphical form for assessing test results.

Their novelty arises as follows :

(a) they are suitable for the higher dose ranges, where saturation and interface effects are strong.

TABLE 4. PARAMETERS L,M AND N FOR THE CURVES IN FIG. 4

| | OXIDE CHARGE PARAMETERS | | | INTERFACE CHARGE |
|---|---|---|---|---|
| | RA | L | M | N |
| Fleetwood [9] | 3E-3 | 0.93 | 3.96 | 3.0 |
| Boesch [11] | 7E-4 | 0.7 | 6.91 | 4.64 |
| Bouvier [7] | 7.5E-5 | 0.124 | 3.48 | 7.66 |
| Bingefors [10] | 9E-4 | 0.052 | 7.48 | 5.12 |
| Faccio [5] | 1.5E-4 | 0.26 | 1.31 | - |
| Dentan [6] | 3.5E-5 | 0.047 | 2.54 | 2.55 |

(b) they define a technology range by drawing a "corridor" or lane of values for the growth curve; the corridor rules are rarely violated by members of that class (e.g. "new soft").

(c) key points on the graph possess a combination of intuitive and scientific meaning

The limitations of both the four-lane charts shown here include the following:

(1) the results included are for gamma ray test procedures in which the dose rate is high and the electrical measurements are made immediately after exposure (as in MIL STD or ESA SCC testing). It is well known that a variety of "postirradiation effects" may produce further threshold voltage shifts, either increases or decreases. This often leads to dose rate effects, which are not explicit in the charts, although they are dealt with in the mathematical model in [1], by the use of two time-dependent terms, which give the desired "late" effects; the terms are defined in Section 6.

(2) the assumption is that the bias values are applied to the gates are the worst cases likely in the use of CMOS devices in logic circuits (positive voltage for nMOS, negative for pMOS). The model does not allow for other possible values of bias, although the mathematical model (1) allows for variation of the damage constants, K; the bias dependence of these constants can often be extracted from published radiation test data. Thus, if the time constants are known, the charts can be re-drawn for any other time or bias value.

A less tractable limitation is the fact that, in many ICs, effects in thick "field oxides" often give leakage-induced failure modes not covered by the above model. Another effect not yet included in the model is the degradation of the effective mobility of carriers in the channels. This affects switching speed. Expressions for mobility and derived switching speed values can be added to the models and tabulations but cannot be accomodated in the graphical presentations so far used.

## 4. CONCLUSIONS

We conclude that the classification of CMOS devices presented here is useful as a demonstration of a format which should be widely used to compare MOSFET oxides fabricated by different manufacturers and laboratories. Among the key properties exhibited are (a) a figure for the basic gate oxide "hardness" at a fundamental level (i.e.divorced from oxide thickness and bias fields) (b) analytical expressions have been used to construct, over a very wide dose range prediction curves for the behaviour of a MOS technology, even when given only a few test data points and technology details (c) the ability to predict whether "turnover" will suppress the onset of severe quiescent leakage even at very high doses (d) the effective balance in the nMOS system between positive oxide charge and negative interface charge at very high dose is expressed as a number. These features are expressed in intuitively easy parameters termed rolloff, turnover and balance points. Item

(c) eases some critical choices in CMOS technology (e.g. choice of silicon foundry for an application requiring extremely high doses We recommend that the radiation effects community use a "league table" system based on these intuitive and analytical parameters, to assess the performance of "hardening laboratories" around the world. Now that some processes, previously exclusive to the military, are being released for use in civil high-energy and nuclear energy fields, this sort of open-access league rating is even more desirable than when first mooted by one of the authors over 15 years ago [3]. We also note that the analytical parameters given be inserted in SPICE predictions of circuit performance.

## 5. ACKNOWLEDGEMENTS

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## 6.LIST OF SYMBOLS USED

q is the charge on the electron
$\epsilon_{ox}$ is the dielectric constant of the oxide
g is the hole generation coefficient of value 7.9E12 cm-3 rad-1 for silicon dioxide (using 18 eV/electron-hole pair)
$x_1$ is the distance of the sheet of traps from the silicon
$x_2$ is the distance of the sheet of traps from the gate electrode
$x_c$ is the thicknesss of the charge collection region, which may be x(1) or x(2) depending on polarity
f(E) is the field - dependent fraction of holes generated which are then freed (i.e. escape recombination)
$t_{ota}$, $t_{lit}$ are characteristic times expressing the time-dependence of charge buildup and decay in oxide films
A is the probability of trapping of holes passing through the postulated sheet of traps
$t_{ox}$ is the thickness of the oxide film
$Q_{ot}$ is the oxide trapped charge density
$Q_{it}$ is the interface trapped charge density
$Q_s$ is the density of the image charge in the semiconductor,
D is the radiation dose
$\Delta V_{ot}$ is the shift of the threshold voltage of the transistor due to the radiation-induced charge, $Q_{ot}$
$\Delta V_{ota}$ is the annealing or relaxation of the threshold voltage due to the relaxation of charge $Q_{ot}$ by amount $Q_{ota}$
$\Delta V_{pit}$ is the shift of the threshold voltage due to the prompt buildup of interface charge $Q_{pit}$
$\Delta V_{lit}$ is the shift of the threshold voltage due to the late, or time-dependent buildup of interface charge $Q_{lit}$
K1 to K4 are responsivity constants for the four $\Delta V$ terms listed above.
F is a multiplier for late interface trapped charge, $Q_{lit}$ being a fully matured growth of the new centres.
R is a combination of some of the above terms which remain constant for a given MOSFET design under a given irradiation bias. Typically:

$$R = q\, g\, x_2\, x_c\, f(E) / \epsilon_{ox}$$

L is the main growth constant for oxide trapped charge, used in the PSPIC analysis.
M is the pre-exponential term in the saturating characteristic for oxide trapped charge.
N is the growth constant for interface states.
$D_{ro}$ is the dose value at which linearity of the growth curve rolls off by 5 percent
$D_{to}$ is the dose value at which the growth curve reaches a maximum and turns over
$D_{bl}$ is the dose value at which balance of $Q_{ot}$ and $Q_{it}$ is achieved (the actual point used is $-\Delta V_T = 0.1V$)
$\Delta V_{ro}$ is the voltage shift value corresponding to $D_{ro}$
$\Delta V_{to}$ is the voltage shift value corresponding to $D_{to}$

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