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RADIATION TESTING OF FLIGHT LOTS FOR MARS-94 COVERING - SEMICONDUCTOR TYPES AS 4 M-BIT DRAM, 256 K-BIT SRAM, 256 K-BIT EEPROM AND A 53C90 SCSI CONTROLLER.

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Abstract

The MARS-94 Mass Memory Unit (MMU) uses many new and advanced digital semiconductor components for which there is no radiation data available. This paper reports on a radiation programme covering total ionising dose (TID) and single event effects (SEE) testing of devices from flight and back-up lots. Expected in-orbit upset rates, based on these ground tests and the CREME suite of programs, are calculated for this mission.

INTRODUCTION

The MARS-94 mission is a scientific mission to be launched October 1994 to the planet Mars. The MMU on-board this flight consist of a semiconductor data store of 2 Gigabit based on 4 Mbit Dynamic Random Access Memories. The radiation environment to be encountered by the MMU is primarily interplanetary, thus solar flare protons and galactic cosmic rays only (one pass through the trapped radiation belts of the earth).

Several of the key components to be used in this semiconductor MMU were processed using the latest technology. Having no or very little radiation information on components coming from these manufacturing lines, a number of component types were identified as requiring radiation testing. The types to be tested were Micron 4Mx1 DRAM and 32Kx8 SRAM, Seeq 32Kx8 EEPROM and the NCR 53C90 SCSI controller. Seeing large variations in earlier reported radiation data on similar types, it was decided to radiation assess components from the flight lots. We present the results of these tests which cover TID and heavy ion testing. The ESTEC Co-60 facility was used for the TID and the ESTEC "CASE" single event upset (SEU) facility for the initial upset data. Further heavy ion testing was carried out at Brookhaven National Laboratory using the Tandem van der Graaff, over a Linear Energy Transfer (LET) range of 1 to 120 MeV/(mg/cm^2). Finally, we provide calculations of the MARS-94 expected in-orbit upset rate based on these ground data.

Additionally, for comparison and as a back-up, radiation data obtained on the shrunk 1Mx4 DRAM from Micron, on the Texas Instrument shrunk 4Mx1 DRAM, on the Hitachi 32Kx8 EEPROM, on the commercially available Seeq 32Kx8 EEPROM (only TID) and on commercially available NCR 53C90 SCSI controller, are also presented.

II. DEVICES TESTED

Eight devices from each of the flight lots (six for the NCR controller) for MARS-94 and up to ten devices from each of the back-up lots were available for radiation testing. Device type, manufacturer, marking, die information, die size and process information (if available) for these lots can be found in Table 1. Additional technology details, if available, and comments are given in the following per device group. The last column in Table 1 gives the number of devices actually exposed to each test.

4MBIT DRAMs

The Micron 4Mx1 DRAM is a CMOS silicon gate process with a line width of 0.8 µm. The same process was previously tested in 1991 by ESTEC [1]. The shrunk 1Mx4 also tested here (process D15B) has a line width of 0.6 µm. The T.I. DRAM is a EPIC CMOS double level metal process rev.B. S2.1 having a line width of 0.75 µm.

32Kx8 SRAMs

The Micron 32Kx8 SRAM is a CMOS high speed low power process using a 4-transistor memory cell with a line width of 0.9 µm. Process details of the previously tested type are not known, but die information can be found in Table 1.

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DEVICE FUNCTION	MANUF-ACTURER	PACKAGE MARKING	DATE CODE	DIE - MARKING & SIZE	mm²	PRO-CESS	Co-60	H.ION CASE	PROT.
MARS-94 FLIGHT DEVICES									
32Kx8 SRAM	MICRON	JM38510/29308 BYA USA GY440	2C9231	MT5C2568 S06 REVA '90	36.3	S06A	4 2	4	1
4Mx1 DRAM	MICRON	5962-9062202MTA USA	2C9236C	MT4C4001 D02 REVA '90	74.7	D02A	4 2	2	-
32Kx8 EEPROM	SEEQ	5962-8852506XA C	9223B	57C53B-5001 SEEQ 1989	39.8	P512	3 2	2	-
50C90 SCSI	NCR	CQ12444 609 53C90HR-68CQFP	8923P	NCR 1987 W701 263X220	36.9	2µm	3 2	1	-
BACK-UP DEVICES									
32Kx8 SRAM	MICRON	5C2568C-25 883C USA	0C9028	MT5C2568 1987	46.1		4 2	2	-
1Mx4 DRAM	MICRON	4C4001JC-00E ENG.SAMPLE	9244	MT4C1004 REV D15B '92	55.8	D15B	4 2	2	-
4Mx1 DRAM	TEX.I.	SMX44100-80HLM 2ABH	9218 B	1990TI 44100B	70.6	S2.1	4 2	2	-
32Kx8 EEPROM	HITACHI	HN58C256P-20 R3102340 JAPAN	9232	58C256R HITACHI	33.1		4 2	1	-
50C90 SCSI	NCR	53C90A 609-3400640 CF47271	9217N	NCR 1989 WC43-73	45.8		3 3	-	-

Table 1. Device type, manufacturer marking, die identification, process and number of devices exposed to each tests.

32Kx8 EEPROM

The Seeq 32Kx8 EEPROM is a CMOS non EPI process with a line width of 1.0 µm. The Hitachi EEPROM process is not known, but die identification can be found in Table 1.

50C90 SCSI CONTROLLER

The NCR 53C90 Enhanced SCSI Processor (ESP) is a high performance CMOS device which implements the ANSI X3.131-1986 SCSI standard.

The MARS-94 50C90 SCSI lot is a CMOS non EPI 2 µm process. We have no process data on the commercial type, but both types can be further identified via die details in Table 1.

III. TEST SYSTEMS

SRAM/DRAM/EEPROM

Two dedicated memory test systems, one for TID testing (old tester) and one for SEE testing (new tester), were used [1][2]. Testing was carried out using the MOVI 50/50 test pattern [3], checking for functionality errors and monitoring the current. Testing of SRAMs and DRAMs followed the standard technique whereas EEPROM testing required a new test approach.

For SEU testing of EEPROMs in read mode, following programming, normal read cycles (checking the memory content) can be carried out. In write mode, we used a test cycle as follows: first a write (1) followed by 3 read cycles then a write (0) followed by 3 read cycles. The three read cycles allow us to separate errors into read errors (one SEU in one of the three read cycles) and in write errors (the same SEU in all three cycles). For TID testing, following programming (1), the test cycle was changed to read for 30 minutes then re-programming (write with 0), 30 minutes read, then re-programming (write with 1), 30 minutes read, and so on.

50C90 SCSI CONTROLLER

In order to SEU test the 50C90 a dedicated test system was developed. A test board carrying the Device Under Test (DUT) and a PC interface card was built. The DUT board (8 x 10 cm) was built with two sockets, one for 68 pin flat-pack devices (MARS-94) and one for 68 pin PLCC devices. The DUT board was placed in the vacuum chamber (radiation environment) with only communication and power lines brought out. The PC, via the interface card, allowed remote control of all commands and collection of test data.

The test software was written in FORTH. This language allows an easy and interactive development. The application is developed by creating so-called FORTH words using the language primitives. The new word becomes then part of the dictionary and can be used as any other primitive. FORTH operates on a data stack instead of a variables as for common languages. This concept leads to very compact and fast coding. Finally, FORTH has a nice documentation feature. For each block of code, a so-called shadow documentation block allows comments which makes the

software almost self-explanatory.

The test technique is basically a loop which writes defined values into the various registers and compares these values every second. This test set-up allowed us to test the Configuration Register 8 bits, the XFER Counter 16 bits, the TFER Counter 16 bits and the FIFO 128 bits, a total of 168 bits. For each test, a dedicated test file is generated which contains all DUT data and general information. From this file, an SEU summary display can be created. The format of such a summary sheet can be seen in Figure 1. The upper part gives test details and conditions, the middle part provides a bit map showing the number and location of upsets, the lower part shows the number, location and content of multiple SEU's.

```
NCR53C90 SCSI controller SEU testing: 20 NOV 1992  - 16:22

 Test number : 52   Part F01   Source IV   Height  3cm.

Pattern in the input byte of the FIFO :

         0    1    0    1    1    0    1    0

        MSB   6    5    4    3    2    1   LSB      TOTAL

CONF     0    1    0    3    0    3    0    4        11
XFER H   5    1    1    1    1    2    1    3        15
XFER L   5    1    4    1    1    5    1    5        23
TFER H   0    0    0    5    0    0    0    0         5
TFER L   0    0    0    5    0    0    0    0         5
FIFO 0   3    0    2    0    0    1    1    2         9
  :      0    1    1    0    3    0    2    2         9
  :      0    0    1    0    0    4    0    2         7
  :      0    1    1    2    1    0    3    0         8
  :      4    0    2    1    0    0    0    2         9
  :      0    2    0    2    2    0    2    0         8
  :      0    0    4    0    0    1    0    0         5
  :      2    2    0    3    1    0    2    0        10
  :      1    1    1    0    0    0    0    1         4
  :      0    1    0    2    1    0    0    0         4
  :      1    0    0    0    0    0    0    0         1
  :      0    3    1    3    2    0    2    0        11
  :      5    0    0    0    0    1    1    0         7
  :      2    0    0    1    0    0    4    0         7
  :      0    0    1    0    0    3    0    1         5
FIFO I   1    1    1    0    0    1    0    0         4

TOTAL   29   15   20   29   12   21   19   22       167

Modified with :       2 x 3 SEU in CONF   :   58
                      6 x 2 SEU in TFER   : 0300
                      4 x 2 SEU in TFER   : 0003
                      1 x 4 SEU in FIFO I :   5A
                     _______________________________
                     13  30 SEU removed out of 197
```

Figure 1. SEU summary display output.

IV. TEST CONDITIONS AND TEST FACILITIES

All results presented here were obtained with VDD = 5.0 V, using MOVI or "55"/"AA" test patterns and monitoring the current. DRAMs and SRAMs were tested in the standard way whereas three different SEU tests were performed on the EEPROMs, read mode, write mode and unbiased mode testing.

ESTEC source IV, 1.38 microcuries of CF-252, was used during all Californium-252 Assessment of Single-event Effects ("CASE") tests. Fission fragment fluxes ranging from 240 to 1600 ions/cm²/min. were used. The average LET of Cf-252 is 43.0 MeV/(mg/cm²), a value which has been used for presentation of test data.

SEU heavy ion testing was carried out at the twin Tandem Van de Graaff accelerator at Brookhaven National Laboratory, Long Island, USA. The dedicated SEU test facility at beam line 55° East in target room 4, was used [4]. Testing was carried out with the incident ion beams normal to the die surface as given in Table 2, and having the DUTs tilted at 45° and 60°.

TID testing was carried out using the ESTEC GAMMABEAM 150C Co-60 facility (original activity 2040 Curies) at dose rates ranging from 0.9 to 4.0 Krads(Si)/hour.

ION	ENERGY (MeV)	TILT	LET in Si MeV/(mg/cm²)	RANGE in Si (um)
12-C	95	0°	1.5	173.0
19-F	135	0°	3.5	114.0
35-Cl	205	0°	11.6	61.6
58-Ni	265	0°	26.6	42.2
127-I	321	0°	59.7	31.0

Table 2. BNL ion beam characteristics.

V. RADIATION TEST RESULTS

"CASE" RESULTS

DRAM and SRAM "CASE" results for the various tests are given as Cf-252 points in the heavy ion graphs (see Figures 2(a), 2(b), 2(c) and 2(d). As can be seen for most of these reference points, their actual LET value depends on the dead layer but in general would be somewhere between 15 and 20 MeV/(mg/cm²).

The EEPROMs were tested in an unbiased mode checking their functionality and memory content after irradiation, in the normal read mode and in the write mode as

MANU.	TEST CONDITION	FLUENCE p. cm²	ERRORS SEU/SEL	CROSS SECTION cm² DEVICE	PER BIT
SEEQ	UNBIASED	1393218	0/0	<7.2E-07	<2.7E-12
SEEQ	READ	484428	0/0	<2.1E-06	<7.9E-12
SEEQ	WRITE	1529605	*48/0	3.1E-05	1.2E-10
HITA.	UNBIASED	717315	0/0	<1.4E-06	<5.3E-12
HITA.	READ	1378080	0/0	<7.3E-07	<2.8E-12
HITA.	WRITE	180235	*11/0	6.1E-05	2.3E-10

* Re-programming failure

Table 3. EEPROM "CASE" summary results.

previously described. The results for these tests have been summarised in Table 3. As can be seen, only the write mode testing showed SEUs. Analysis of these SEUs identified the Seeq errors to be 42 byte failures, 5 page failures and 1 block failure (3/4 of the memory). One of the two devices tested failed totally, re-programming of the memory was not possible. After 9 byte and 2 page failures, the Hitachi write mode tested device also failed re-programming.

The 53C90 "CASE" results for the MARS-94 SCSI controller are given in a summary format in Table 4 and for the commercial type in Table 5. These tables present the total number of measured SEUs with their single and multiple error distributions as observed in the different registers and FIFO. The s/n tested, the test pattern used, the fluence in fission particles per cm² and multiple error details, are also given. Finally, "CASE" cross section values per cm² have been calculated for the "device" and "per bit". As can be seen from these two tables, large variations exist in their SEU sensitivity. The MARS-94 is less sensitive, has fewer multiple errors, fewer bits changed in a multiple error event, and smaller cross section. However, due to Cf-252 particle penetration (about 15 micron in Si) and LET reduction limitations, these results should be further assessed against

S/N PATT.	FLUENCE p. cm²	ERRORS SEU/SEL	ERROR DISTRIBUTION/MULTIPLE CONF.	XFER.	TFER.	FIFO
F1 A5A5	2620862	69/0	5/1	11/1	1/2	48/0
F1 5A5A	6069586	180/0	11/2	38/0	10/10	108/1
F2 5A5A	3876504	106/0	1/0	12/0	7/3	83/0
F2 A5A5	8546204	181/0	21/1	27/0	9/6	117/0
	21113156	536/0	38/4	88/1	27/21	361/1

MULTIPLE ERRORS ; A5A5 | 5A5A

A5A5	5A5A
2 x 2-bit SEU in CONF: A0	2 x 3-bit SEU in CONF: 58
1 x 9-bit SEU in XFER: 000B	6 x 2-bit SEU in TFER: -3--
3 x 2-bit SEU in TFER: 3---	7 x 2-bit SEU in TFER: ---3
5 x 2-bit SEU in TFER: --3-	1 x 4-bit SEU in FIFO: --5A

"CASE" CROSS SECTION ;

AVERAGE PER DEVICE (168 bits)	-	**2.5E-05 cm²**
AVERAGE PER BIT	-	**1.5E-07 cm²**
or CONFIGUR. BITS	-	2.5E-07 cm²
TRANSFER BITS	-	2.7E-07 cm²
XFER COU. BITS	-	1.4E-07 cm²
FIFO	-	1.3E-07 cm²
DEVICE LATCH-UP	-	**<4.7E-08 cm²**

Table 4. MARS-94 NCR 53C90 SCSI controller "CASE" results.

S/N PATT.	FLUENCE p. cm²	ERRORS SEU/SEL	ERROR DISTRIBUTION/MULTIPLE CONF.	XFER.	TFER.	FIFO
#1 5A5A	3667157	152/0	25/0	14/0	10/6	95/2
#1 A5A5	32535362	1129/0	137/0	176/6	82/32	676/20
#2 A5A5	47512644	1771/0	192/0	252/6	127/62	1094/38
#3 A5A5	13160096	514/0	40/0	57/2	30/22	353/10
#3 5A5A	9070608	394/0	34/0	50/4	41/12	251/2
	105945867	3960/0	428/0	549/18	290/134	2469/72

MULTIPLE ERRORS ; A5A5 | 5A5A

A5A5	5A5A
14 x 9-bit SEU in XFER: 000B	9 x 2-bit SEU in TFER: -3--
62 x 2-bit SEU in TFER: 3---	9 x 2-bit SEU in TFER: ---3
54 x 2-bit SEU in TFER: --3-	1 x 4-bit SEU in FIFO: --00
1 x 4-bit SEU in FIFO: --00	2 x 10-bit SEU in XFER: 0005
51 x 68-bit SEU in F+CO: 0000	3 x 68-bit SEU in F+CO: 0000
4 x 66-bit SEU in F+XT: 0000	2 x 14-bit SEU in XF+F: 005A
12 x 10-bit SEU in F+XF: 0000	

"CASE" CROSS SECTION ;

AVERAGE PER DEVICE (168 bits)	-	**3.7E-05 cm²**
AVERAGE PER BIT	-	**2.2E-07 cm²**
or CONFIGUR. BITS	-	5.1E-07 cm²
TRANSFER BITS	-	3.4E-07 cm²
XFER COU. BITS	-	2.5E-07 cm²
FIFO	-	1.9E-07 cm²
DEVICE LATCH-UP	-	**<9.4E-09 cm²**

Table 5. Commercial NCR 53C90 SCSI controller "CASE" results.

Heavy Ion Induced SEU Characteristic

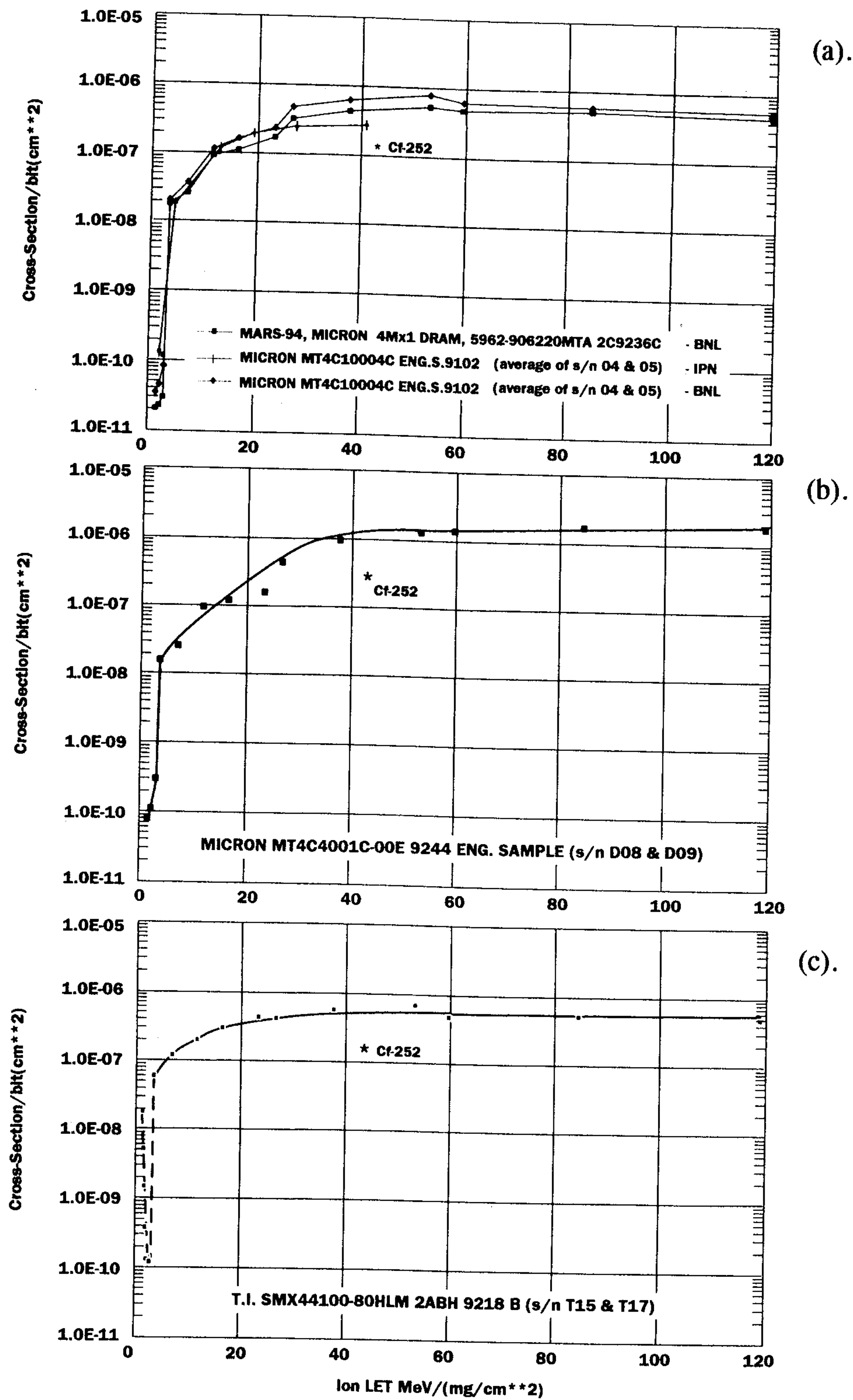

Figure 2. Heavy ion Single Event Upset test results for 4 M-Bit DRAM memories : (a) Micron process D02A, (b) Micron process D15B and (c) T.I. process S2.1.

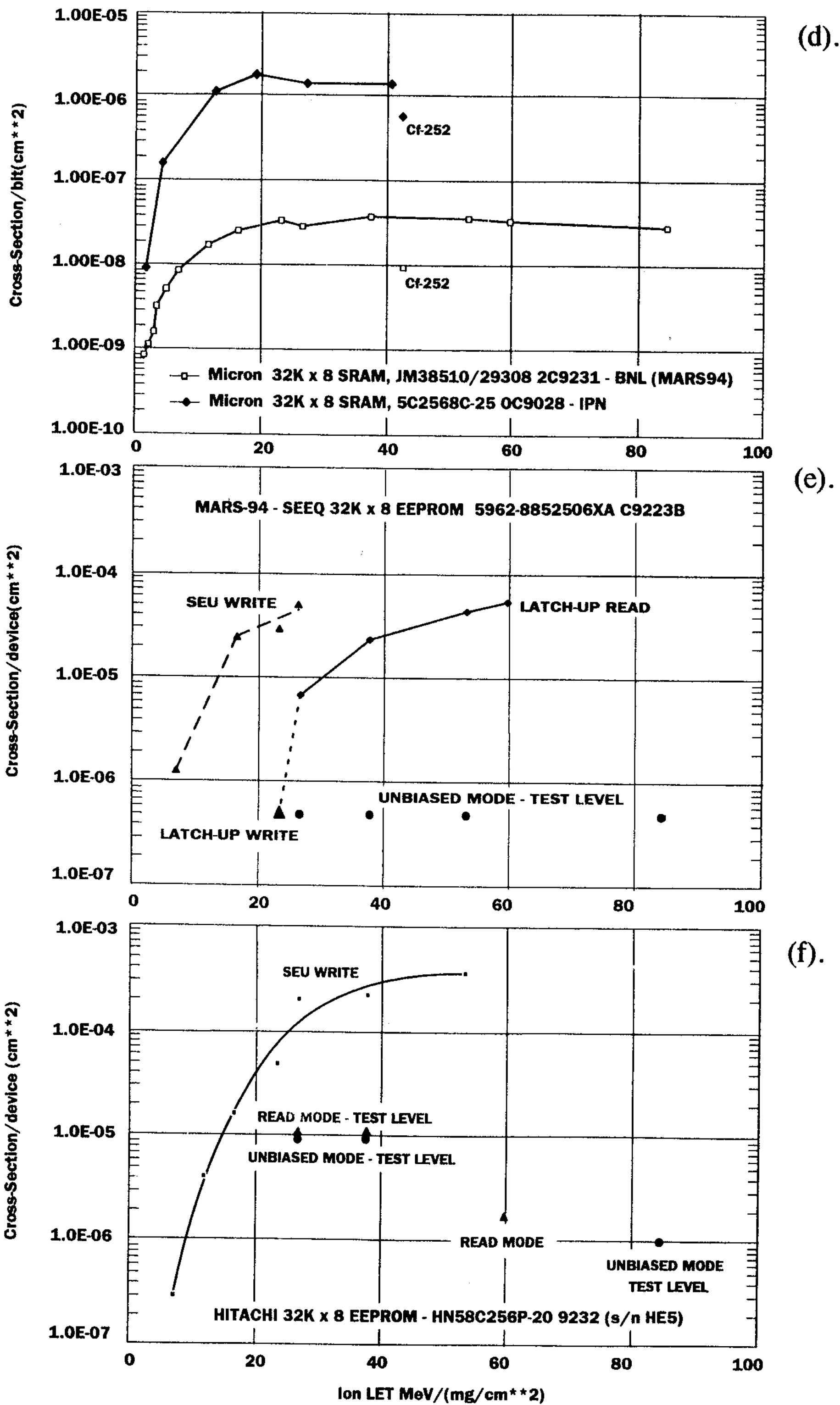

Figure 2. /cont. Heavy ion Single Event Upset and Latch-up test results for :
(d) Micron 32K x 8 SRAMs, (e) Seeq 32K x 8 EEPROM and (f) Hitachi 32K x 8 EEPROM.

device technology information. These details will be available in the beginning of 1994 when National Microelectronic Research Centre (NMRC) completes the MARS-94 reverse engineering work. Note that no latch-ups were observed in any of the "CASE" tests, this may also be due to particle penetration limitations.

HEAVY ION SEU RESULTS

Heavy ion SEU test results for all SRAMs, DRAMs and EEPROMs can be found in graphical form in Figures 2(a), 2(b), 2(c), 2(d), 2(e) and 2(f). These graphs show, as a function of LET, the upset cross section "per bit" or "per device" per cm^2. All data points shown correspond to an average value derived from all tests at that particular LET. For several of the EEPROM tests where no errors were observed, test levels (1/fluence), are given.

The three upset curves presented in Figure 2(a) show the SEU results for the Micron 4Mx1 DRAMs. These curves cover the MARS-94 lot (ref. ■) tested at BNL, engineering devices having d/c 9102 (ref. ♦) tested at BNL and the same engineering devices tested at IPN (ref. +). As can be seen from these curves, threshold LET levels, curve slopes and saturated values come quite close confirming previously published data [1]. Fairly good inter-facility consistency was observed on these tests. The upset curve for the new Micron 1Mx4 DRAM as presented in Figure 2(b), shows higher saturated cross section values whereas slope and threshold behaviour come close to the old type.

The upset curve for the T.I. 4Mx1 DRAM (rev. "B") as presented in Figure 2(c) show a similar curve slope and saturated value as the old Micron, however, the LET threshold level appears to be lower. The fall in the curve (as indicated with the dotted line) comes from testing with Carbon-ions and having the DUT tilted between 30° and 60°. This somewhat strange behaviour at low LET is probably due to a combination of using a light ion type and the 4Mx1 DRAM technology. The DRAM memory cells have trench capacitors with a depth of about 5 μm and a diameter of about 1 μm. With these dimensions, the length of the ion track through the sensitive volume will be reduced at tilt angles and result in a deposited charge lower than the critical charge required for upsets.

The two upset curves presented in Figure 2(d) show the SEU results for the Micron 32Kx8 SRAM. The lower curve covers the MARS-94 flight lot (ref.■) tested at BNL whereas the upper curve gives the result for the previous technology (ref. ♦) tested at IPN. As can be seen from these results, large SEU sensitivity differences exist between these two technologies. Fortunately for MARS-94, the new S06A process is by far the best.

The heavy ion results for the Seeq 32Kx8 EEPROM are presented in Figure 2(e). Results for the three test modes are shown, however, as can be seen the latch-up behaviour dominated the testing. No SEUs were observed in the unbiased mode of testing up to a LET of 84.5 MeV/(mg/cm^2) and in the read mode of testing up to a LET of 59.7 MeV/(mg/cm^2). The write mode gave errors as shown in the graph with a LET threshold value around 6.9 MeV/(mg/cm^2). No reliable test data could be obtained at LETs higher than 26 MeV/(mg/cm^2) due to latch-up.

The results for the Hitachi 32Kx8 EEPROM are presented in Figure 2(f). Again, results for the three test modes are given. No SEUs were observed in the unbiased and read mode of testing whereas the write mode showed a similar behaviour as the Seeq with a threshold value around 6.9 MeV/(mg/cm^2). The SEU write curve approach some sort of saturated level at a LET of 53.2 MeV/(mg/cm^2), the highest LET tested.

Unfortunately, latch-up in the first tested 53C90 controller, when tested with Ni-ions at a LET of 26.6 MeV/(mg/cm^2), limited the SEU characterisation of the MARS-94 lot. At this LET, the latch-up rate was measured to be in the order of 7.7E-6 cm^2/device, a level which interfered strongly with the recording of SEUs. As no SEUs or latch-ups were recorded when testing with Cl-ions at a LET of 15.1 MeV/(mg/cm^2), and not having the possibility of tilting the DUT, thus changing the effective LET, we had to stop the testing. Reliable test data can only be recorded with the add of a latch-up protection circuit. So today we can only conclude, the MARS-94 controller to have a SEU and latch-up threshold somewhere between these two test levels. The BNL test arrangement did not allow for testing of the commercial 53C90 lot (different package).

Co-60 TID RESULTS

Total ionising dose data are presented in a summary format in Table 6. This table show all devices tested and results obtained. Device function, serial number, dose rate in rad(Si)/hour, functional failure levels for the first bit error and for 1Kbit errors when testing have been stopped, initial and final standby (ICCSB) and operating (ICCOP) current and annealing behaviour, are given. However, the functional failure levels should always be seen in relation to current behaviour as given in the last column "Remarks". The annealing results, "Fail" or "Work", are given as measured after one week unbiased and at room temperature.

For the MARS-94 lots, the Micron 32Kx8 SRAM failed at a surprisingly low level around 5 Krad(Si) whereas the 4Mx1 DRAM behaved better than expected. The Seeq 32Kx8 EEPROM also showed good TID behaviour $\geq$ 22 Krad(Si), especially when compared with commercial devices also tested at the same time. These devices failed at levels around 6.0 Krad(Si). Three unbiased MARS-94 devices, tested at a dose rate of 8.0 Krad(Si)/hour, showed parametric failures between 40 and 50 Krad(Si). The NCR MARS-94 controller showed acceptable behaviour with a better than level of 15 Krad(Si), however, the commercial type showed even better performance. Finally, quite acceptable TID levels were also found for several of the other back-up lots as can be seen in the table.

DEVICE FUNCTION	S/N	D.RATE rad/hr	FUNC. FAILURE Krad(Si)	ICCSB INITIAL mA	ICCOP INITIAL mA	ICCSB FINAL	ICCOP FINAL	ANNEA-LING	REMARKS
M A R S - 9 4 F L I G H T D E V I C E S									
MICRON 32Kx8 SRAM	#01	3000	5.8 5.8	0.17	1.10	28.4	7.17	FAIL	ICC increase from 5 Krad
	#02	3000	5.7 5.7	0.17	1.10	28.4	7.22	FAIL	
	#03	3000	6.3 6.3	0.17	1.10	28.4	7.22	FAIL	
	#04	3000	5.0 5.0	0.17	1.05	28.4	-	FAIL	
MICRON 4Mx1 DRAM	#01	1200	>30.4 >30.4	0.56	1.70	1.87	3.09	WORK	ICC increase from 15 Krad
	#02	1200	>30.4 >30.4	0.56	1.70	1.87	3.09	WORK	
	#03	1200	21.7*>30.4	0.56	1.70	1.87	3.09	FAIL*	*S/N 3, Stuck bit
	#04	1200	>30.4 >30.4	0.56	1.70	1.87	3.09	WORK	
SEEQ 32Kx8 EEPROM	#01	900	>22.1 >22.1	0.11	0.85	0.11	0.89	WORK	*S/N 2, Error dis-appeared during reprogramming.
	#02	900	21.5*>22.1	0.11	0.89	0.11	0.89	WORK	
	#03	900	>22.1 >22.1	0.11	0.85	0.11	0.89	WORK	
NCR 50C90 SCSI CONTROLLER	F03	2700	16.2 -	-	3.3	-	3.3	N.M.	ICCOP as measured in the test set-up used.
	F04	4000	19.4 -	-	3.4	-	3.4	N.M.	
	F05	4000	15.0 -	-	4.3	-	4.3	N.M.	
B A C K - U P D E V I C E S									
MICRON 32Kx8 SRAM	#03	2000	17.7 >72.4	-	-	-	-	WORK	ICC increase from 12 Krad
	#06	2000	13.9 38.8	-	-	-	-	WORK	
	#07	2000	26.3 42.7	-	-	-	-	FAIL	
	#08	2000	14.8 29.7	-	-	-	-	WORK	
MICRON 1Mx4 DRAM	#03	1800	20.3 20.9	0.46	1.68	37.00	23.24	WORK	ICC increase from 8 Krad, out of test range at 12 Krad.
	#04	1800	20.3 21.1	0.46	1.63	37.00	23.73	WORK	
	#05	1800	21.5 22.1	0.46	1.63	37.00	23.34	WORK	
	#06	1800	21.0 21.9	0.46	1.63	37.00	23.39	WORK	
T.I. 4Mx1 DRAM	TI1	3000	24.6 26.7	0.57	1.62	28.50	32.23	WORK	ICC increase from 9 Krad
	TI2	3000	26.9 31.4	0.57	1.62	28.50	32.23	WORK	
	TI3	3000	21.2 23.5	0.57	1.62	28.50	32.23	WORK	
	TI4	3000	26.1 27.2	0.57	1.62	28.50	32.23	WORK	
HITACHI 32Kx8 EEPROM	HE5	3000	24.0 24.2	0.05	0.20	0.05	0.24	WORK	
	HE6	3000	25.4 25.5	0.05	0.20	0.05	0.27	WORK	
	HE7	3000	24.0 24.2	0.05	0.15	0.05	0.24	WORK	
	HE8	3000	24.0 24.2	0.05	0.15	0.05	0.24	WORK	
NCR 50C90 SCSI CONTROLLER	C11	2700	>20.6 -	-	4.6	-	4.6	N.M.	ICCOP as measured in the test set-up used.
	C13	4000	>26.4 -	-	4.0	-	4.2	N.M.	
	C14	4000	>36.2 -	-	4.0	-	4.3	N.M.	

Table 6. Summary of total ionising dose results.

VI. MARS-94 ORBITAL PREDICTION

Using the MARS-94 SRAM and DRAM heavy ion SEU results together with the CREME suite of programs [5], the expected mission upset rates have been calculated for the Micron devices. Predictions are made for Galactic Cosmic Ray (GCR) index 1, at solar min., 10 % worst case and ordinary flare. The upset rates are computed from the experimentally determined cross section versus LET curves [6] and using standard sensitive regions of 1 μm and 2 μm. Table 7 gives the various upset rate predictions in bits per day.

MARS94	GALACTIC COSMIC RAYs					
MICRON RAMs	MIN. 1 μm	MIN. 2 μm	10 % WC 1 μm	10 % WC 2 μm	ORD. FLARE 1 μm	ORD. FLARE 2 μm
32Kx8	1.6E-7	9.0E-8	2.6E-7	1.5E-7	3.3E-7	2.1E-6
4Mx1	8.2E-7	6.0E-7	1.4E-6	1.0E-6	1.9E-5	1.4E-5

Table 7. MARS-94 upset rate (bit/day) predictions.

VII. CONCLUSIONS

A number of advanced semiconductor technologies have been radiation characterised via this programme. Unexpected results were experienced in several of the MARS-94 lots. The most significant findings can be summarised to be the very low TID margin of the 32Kx8 SRAM and exceptionally low SEU susceptibility to heavy ions. The 4Mx1 DRAM showed TID performance and SEU behaviour as expected. The EEPROM showed unexpected sensitivity to latch-up and to SEU (write mode). The 53C90 SCSI controller also showed unexpected latch-up behaviour in the heavy ion environment and its number of single and multiple SEUs. Finally it should be noted, that the project has taken several precautions in order to minimise these possible threats. Latch-up protection switches, software changes, position of devices and their use, are some of the steps taken in ensuring the MMU mission success.

VIII. REFERENCES

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