RADIATION CHARACTERISATION OF COMMERCIALLY AVAILABLE 1Mbit/4Mbit SRAMs FOR SPACE APPLICATIONS

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Abstract

This paper presents the radiation results of a ground test program carried out on seven commercially available 1Mbit / 4Mbit SRAMs. Heavy ion and proton single event effect (SEE) results together with Co60 total ionizing dose performance are presented for these spacecraft candidate types.

I. Introduction

Spacecraft designers utilize increasing number of commercial devices. The objective of this study was to provide them complete radiation data on seven commercially available SRAM devices which have been selected for their performances (speed, power consumption) and their availability.

This work was performed in the frame of an ESA/ESTEC contract.

II. Presentation of the tested devices

Three 1M and four 4M SRAM device types were tested. References of tested devices are presented in Table 2. They were all the latest version available on the market at the end of the year 1997. All tested devices are 5V devices.

Two parts per device type were tested during heavy ion experiments, two parts per device type were tested during proton experiments and three parts per device type were tested during total dose experiments. Parts submitted to heavy ion testing were delidded.

III. Test conditions

A. Irradiation Facilities

Heavy ion testing was performed at the HIF (Heavy Ion Facility) CYCLONE, Louvain-La-Neuve, Belgium [1] over the LET range 1.7 to 68 MeV/(mg/cm^2). The ion species used for this characterization are described in Table 1. In all cases the total accumulated dose on the two heavy ion irradiated parts is lower than 2 krad(Si).

Table 1 : characteristics of ions used

Ion	Energy [MeV]	Range (Si) [µm]	LET (Si) [MeV/(mg/cm^2)]
^{84}Kr	316	43	34
^{40}Ar	150	42	14.1
^{20}Ne	78	45	5.85
^{10}B	41	80	1.7
^{132}Xe	459	43	55.9

Low energy proton SEE testing, 64.5 to 8.4 MeV, was carried out at OPTIS (therapy beam line), PSI, Villigen. In all cases the total accumulated dose on the two proton irradiated parts is lower than 6 krad(Si).

Total dose testing was performed at ESA ESTEC Co60 facility at a dose rate of 400 rad(Si)/hour.

B. Test conditions

All tests were performed at room temperature, and devices biased at the nominal supply voltage of 5V.

SEE tests were performed in dynamic mode : the device under test is tested with the logical checkerboard pattern and in case of error within one byte word, the correct byte is rewritten during the irradiation. After each irradiation run the devices were also tested with the complementary pattern in order to detect stuck bits induced by microdose effects [2].

Functionality and power consumption (standby current) of each device was checked in situ during total dose irradiation. Parts are biased in the standby mode with a « all 0 » pattern during irradiation when they are not under test. The standby power supply current of each device is measured every 3 hours and functionality is checked every 6 hours. The test pattern used for the functional test is the MOVI pattern.

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Table 2 : reference of tested devices.

Manufacturer	Size	Package Marking	datecode	Die Marking	Technology	Package
Sony	1M (128Kx8)	Sony CXK581000BP-10LL 709 03 VK		CXK581000B, Sony 1996		DIP 32 600 mils
ISSI	1M (128Kx8)	*top* ISSI IS61C1024-20M C1204900S6 9621 *back* 8072AT1VA TAIWAN,C1204800S6	9621	C8072AT 01 SEP 1995 M ISSI	CMOS 0.5 µm	DIP 32 400 mils
Hitachi	1M (128Kx8)	HITACHI JAPAN 9713 HM628128BLP-7 00002330	9713	HM628128B, HITACHI	Hi CMOS 0.8µm mask rev. B	DIP32 600 mils
Hitachi	4M (512Kx8)	HITACHI JAPAN 9705 HM628512ALP-7 00002330	9705	HM628512A (M) HITACHI	HiCMOS 0.5 µm mask rev. A	DIP32 600 mils
Austin	4M (512Kx8)	*top* ASI 0EU86 XT AS5C4008CW-35E AUSTIN 7B9731 USA *back* AS5C4008CWPE E58532.4HB 9731 USA	9731	E70J C 1993 M, MOTOROLA MCM62-46--	CMOS EPI 0.5 µm	CERDIP32 600 mils
Motorola	4M (512Kx8)	*top* MCM6246WJ20 MOTOROLA FIQGA9602 *back* KOREA NXKEI5	9602	E70J © 1993 (M) MCM62-46--	CMOS EPI 0.5 µm mask rev. W51	SOJ36 400 mils
Samsung	4M (512Kx8)	*top* SEC KOREA 731 KM684002AJ-17 SDCE23EC *back* KOREA1		Samsung Electronics 1995.9 KM684002A	CMOS EPI 0.5µm mask rev. A	SOJ36 400 mils

IV. Single Event test results

A. Single Event Upset (SEU)

Heavy ion and proton SEU cross section curves are presented in figures 1(a) to 1(n). As can be seen in the cross section curves, a quite different SEU sensitivity (about three orders of magnitude on cross sections at highest LET) could be observed among the different tested device types. The 4Mbit devices do not appear much sensitive than 1Mbit devices.

Most devices show an equivalent number of 0 to 1 and 1 to 0 SEU transitions. On HITACHI 1M&4M and on MOTOROLA 4M devices, the 0 to 1 SEU transitions are slightly higher for heavy ions tests at LET values greater than 14 MeV(mg/cm^2).

The heavy ion cross section per bit values at saturation are generally greater than the cell area (about 1E-7 cm^2). Heavy ion with a sufficient LET (>14 MeV/(mg/cm^2)) can cause multiple bit upsets. Anyway, on most devices there is no multiple upset within a single byte word (SONY 1M and SAMSUNG 4M) or this number is very low (AUSTIN 4M : 2 events on one run and HITACHI 1M : 1 event on one run) compared with the total number of errors per test run. In that case it is expected that these multiple upsets within a single byte word are certainly caused only by random hitting of two bits within a word by two separate ions.

On MOTOROLA 4M devices the number of multiple upsets within a single byte word is significantly higher down to a LET of 14 MeV(mg/cm^2) but stays low compared with the total number of errors per test runs (less than 1%). On ISSI 1M and HITACHI 4M devices the number of multiple upsets within a single word is comparable to the number of single bit errors within a byte word. For these three devices it is not possible to conclude as the physical mapping of these memories is not known.

No multiple error within a single byte word was observed on all devices but the HITACHI 4M device during proton experiments. On this device two multiple errors (2 bits) were found on SN2 at 44 MeV and one multiple error at 64 MeV plus one multiple error at 44 MeV on SN1.

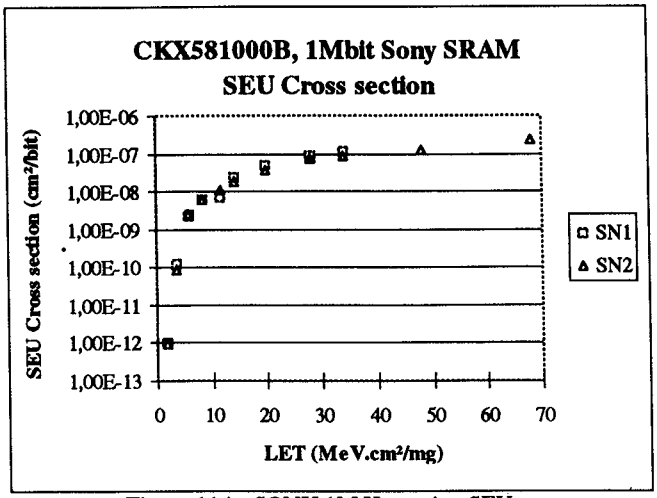

Figure 1(a) : SONY 1M Heavy ion SEU cross section curve

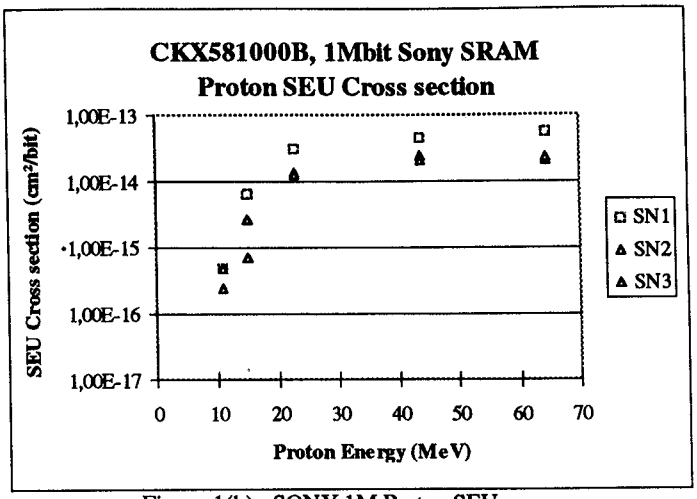

Figure 1(b) : SONY 1M Proton SEU cross section curve

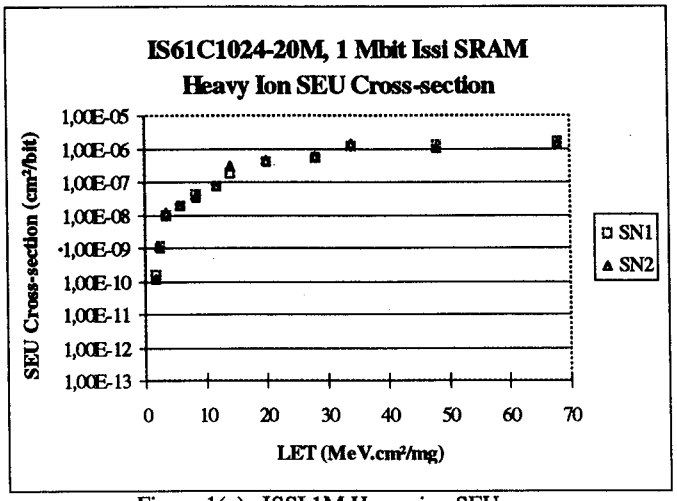

Figure 1(c) : ISSI 1M Heavy ion SEU cross section curve

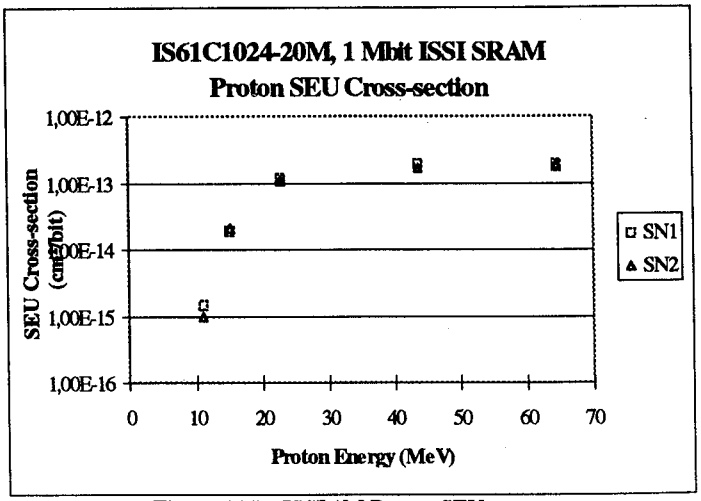

Figure 1(d) : ISSI 1M Proton SEU cross section curve

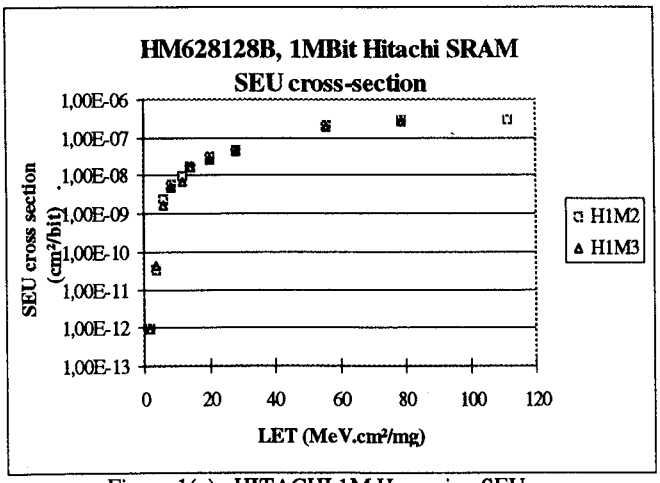

Figure 1(e) : HITACHI 1M Heavy ion SEU cross section curve

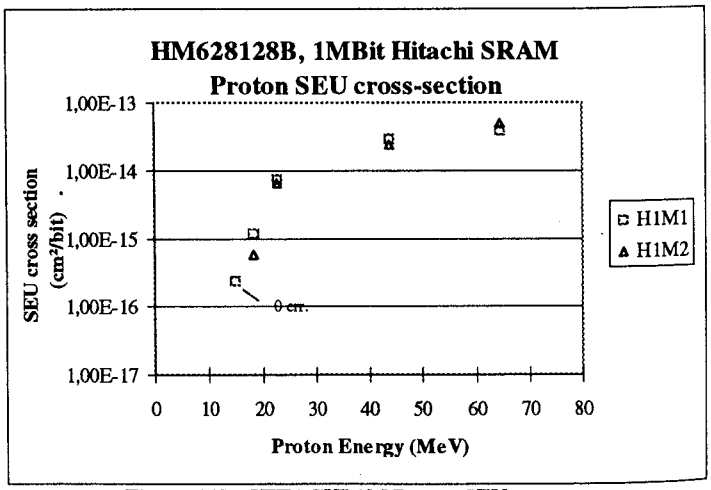

Figure 1(f) : HITACHI 1M Proton SEU cross section curve

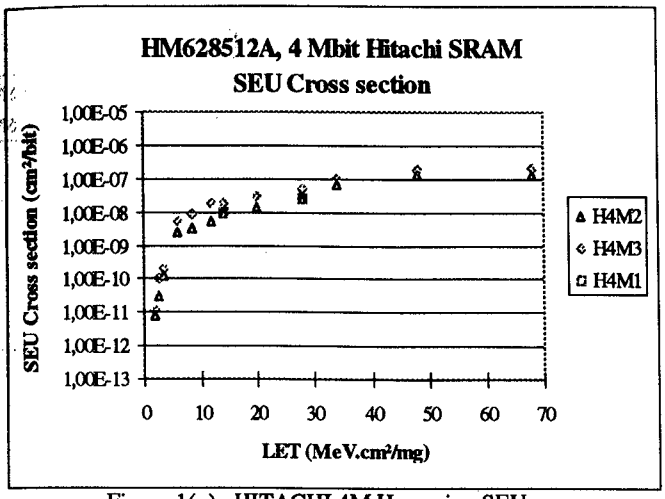

Figure 1(g) : HITACHI 4M Heavy ion SEU cross section curve

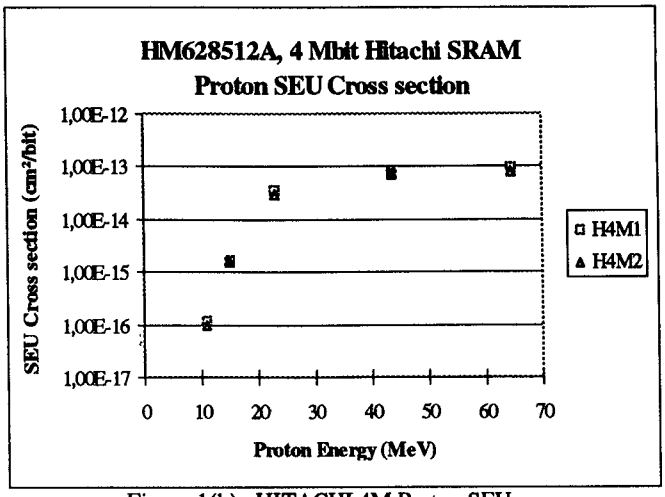

Figure 1(h) : HITACHI 4M Proton SEU cross section curve

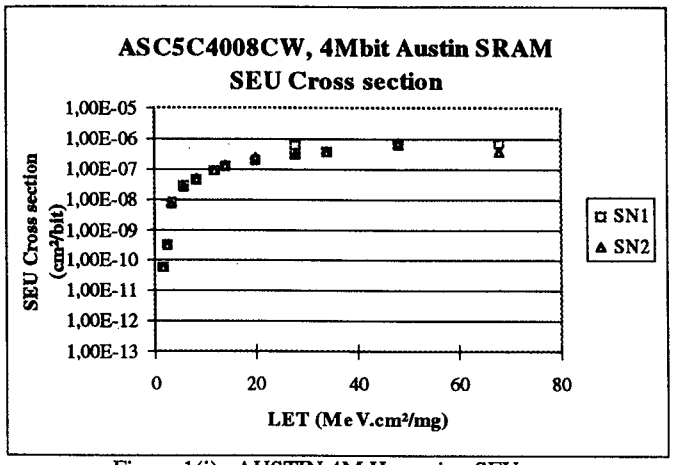

Figure 1(i) : AUSTIN 4M Heavy ion SEU cross section curve

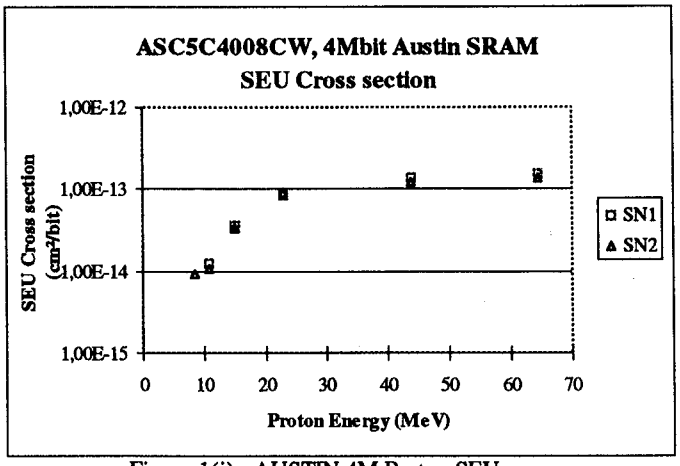

Figure 1(j) : AUSTIN 4M Proton SEU cross section curve

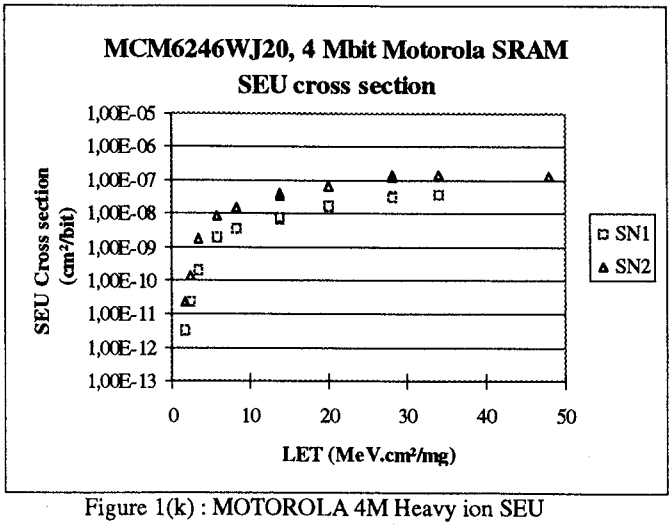

Figure 1(k) : MOTOROLA 4M Heavy ion SEU cross section curve

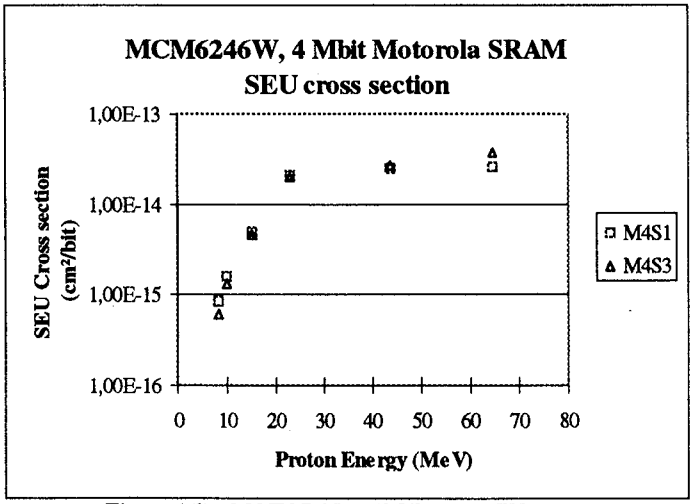

Figure 1(l) : MOTOROLA 4M Proton SEU cross section curve

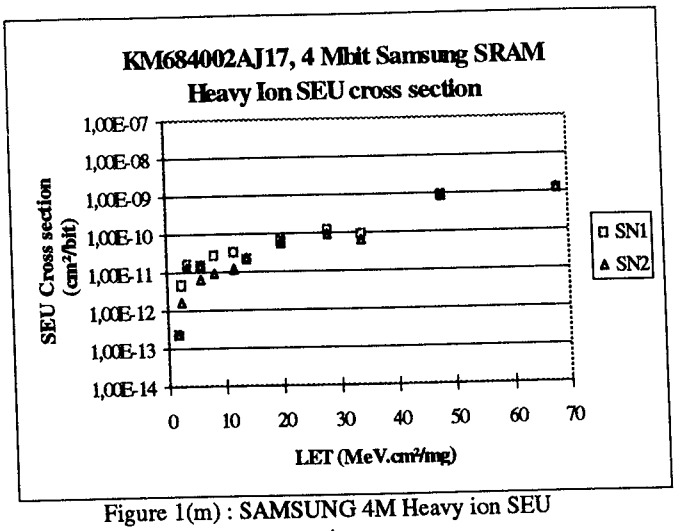

Figure 1(m) : SAMSUNG 4M Heavy ion SEU cross section curve

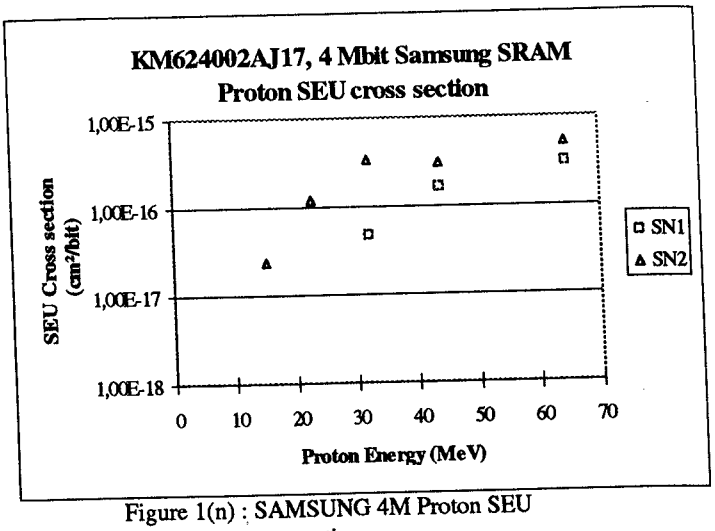

Figure 1(n) : SAMSUNG 4M Proton SEU cross section curve

B. Single Hard Errors (SHE)

SHE are induced by microdose deposition of one (or two) single ions in the gate oxide of the memory cell transistor which is in the ON state [2]. The effect is to stuck the bit in its current state. First generations of 1M SRAMs have been found to have such total dose failures from single ions [3].

No heavy ion induced SHE has been found on three out of the seven tested device types (SONY 1M, ISSI 1M, SAMSUNG 4M). On AUSTIN 4M two SHE were found after the last heavy ion run at 68 MeV/(mg/cm^2) on one part. On HITACHI 1M device one SHE was found after the 55 MeV/(mg/cm^2) run and one other after the 79 MeV/(mg/cm^2) run on the same part. On HITACHI 4M device, two SHE on one part and one SHE on the other part were found after the 68 MeV/(mg/cm^2) run. On MOTOROLA 4M device three SHE on one part and two SHE on the other one were found after the 34 MeV/(mg/cm^2) run.

No SHE was found during proton SEE tests.

C. Single Event Latchup (SEL)

No SEL was detected up to the highest tested LET on all devices but MOTOROLA 4M device. On this device two SEL were observed at the highest LET value of 48 MeV/(mg/cm2). The corresponding cross section value is 1.75E-3 cm^2/device.

V. Total dose test results

Total dose results are presented in table 3. It shows the dose level at the first stuck memory cell, at 1024 stuck memory cells (taken as failure) and at 20% increase of the standby current. It also gives the initial standby current and its value at failure or end of test.

As for SEE results, the total dose sensitivity is quite different for all tested device types. Most sensitive device (HITACHI 1M) shows functional failures at 8 krad(Si) and best device (SAMSUNG 4M) does not show any functional failure and any significant standby supply current increase after about 40 krad(Si).

For all devices but SONY 1M device, after the first stuck cell the number of stuck cells increases very quickly and the failure criteria (1024 stuck cells) is reached a few krad after the accumulated dose at the first error.

On ISSI 1M, HITACHI 4M, AUSTIN 4M and MOTOROLA 4M devices a significant standby current increase appears only after the apparition of the first stuck cells. On the contrary on SONY 1M and HITACHI 1M devices no significant current increase is exhibited even after failure.

VI. Discussion

Based on manufacturer information most of tested devices are made with 4 transistor memory cells (no information is known for HITACHI and SONY devices). These devices are found to have microdose failures from single ions and total dose failures due to the same mechanism (gate oxide effects) [4]. The leakage current does not increase until long after the circuit has failed and a significant variation from chip to chip is observable for the failure level. The shape of the number of bad bits as a function of dose maps the distribution of transistors threshold voltages on a single chip and for different chips we obtain different curves which indicate the chip to chip variation. 4T SRAM are also known to be very sensitive to SEU. Test results obtained are very consistent with this 4T SRAM behavior. The three most sensitive devices to ionizing dose are also sensitive to SHE.

SEL sensitivity is low, but due to the low LET values (maximum LET value = 68 MeV/(mg/cm^2)) and low fluences of experiments at these LET values, no definitive statement could be drawn about non latchup sensitivity.

Table 3 : Total dose results

Type	ID	1st. Error [krad(Si)]	1024 errors [krad(Si)]	Icc standby		
				120% [krad(Si)]	initial [mA]	failure or end of test [mA]
SONY 1M	1	18.23	31.51	---	0	0
	2	22.46	> 37.15			
	3	18.62	30.39			
ISSI 1M	1	14.43	20.97	4.61	0.05	37.43
	2	19.75	25.03			
	3	17.46	22.04			
HITACHI 1M	1	7.99	12.71	---	0	0
	2	8.24	13.68			
	3	9.19	14.08			
HITACHI 4M	1	32.02	> 38.11	3.79	0.05	0.2
	2	32.89	> 38.11			
	3	31.19	> 38.11			
AUSTIN 4M	1	13.6	16.77	14.43	1.77	6.7
	2	12.41	16.92			
	3	13.27	17.15			
MOTOROLA 4M	1	14.18	18.68	18.85	1.95	4.98
	2	17.09	21.50			
	3	13.63	19.31			
SAMSUNG 4M	1	> 39.95	> 39.95	---	4.72	4.93
	2	> 39.95	> 39.95			
	3	> 39.95	> 39.95			

VII. Conclusion

As the 4T SRAM designs are still dominant, the latest SRAM available on the market show about the same radiation behavior than the previous generations, but the radiation sensitivity levels (both for Single Event Effects and Total ionizing dose) are significantly more spread. On some devices SEU sensitivity and/or total dose sensitivity could be very high. Some devices show an unexpected high number of multiple errors within one single byte word. Some devices are sensitive to SHE at LET as low as 34 MeV/(mg/cm^2). Due to the generalization of lightly doped epitaxial layer on a heavily doped substrate, SEL sensitivity is low.

Next generation of SRAM is expected to be dominated by the thin film P channel transistor (TFT) in a 6T cell design. This type of design will reduce the gate oxide sensitivity of transistor cells and then improve SHE behavior. The SEU behavior will also be improved. Total dose failure mechanisms will then be dominated by field transistor leakage [5].

References

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