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RADIATION TEST REPORT

Heavy Ions Testing of
AD565
12-Bit D/A Converter
from Analog Devices

ESA Purchase Order No 171720 dated 22/07/97

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

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This test report has been prepared by:

Name	Function	Date	Signatures
H Constans/ C Tizon	Development Engineers	29/09/97	
FX Guerre	Study Manager	29/09/97	

ESTEC Technical Officer:

R. Harboe Sorensen

HIREX Engineering - 117, rue de la Providence - 31500 Toulouse, France
Tél. (0)5 61 80 64 89 - Fax : (0)5 61 80 65 66 - E-mail : HirexEngineering@compuserve.com
S.A. au capital de 250.000 F - RCS Toulouse B 389 715 525

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1. INTRODUCTION

This report presents the results of a heavy ion Single Event Effects (SEEs) test program carried out for the XMM project on Analog Devices AD565 12-bit D/A Converter. Flight lot devices were tested at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.
The main aims of these tests were to assess the AD565's susceptibility to Single Event Upsets (SEUs) and Single Event Latch-ups (SELs) by heavy ion. Tests were performed in such a way that the SEU cross sections can be plotted over a wide LET range in order to allow computation of the SEU rates in XMM orbit.

This work was performed for ESA/ESTEC under P.O. No 171720 dated 20/07/97.

2. APPLICABLE DOCUMENTS

The following documents are applicable:

- XMM SOW QCA/RHS-XMM.DOC July 97 (fax dated 11 July, 97),
- Test Set-up Specification for heavy ion testing of XMM devices - Hirex Doc No HRX/97.2598 Issue 1 Rev. A dated 7 August 1997 -

2.1 REFERENCE DOCUMENTS

- Analog Devices, AD565 data sheet.
- Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
- The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

3. ORGANIZATION OF ACTIVITIES

The different tasks performed during this evaluation have been conducted in the order shown in Table 1 by the relevant company.

Table 1 - Organization of activities

Para. 5.1	Procurement of Test Samples (Hi-rel serialized devices)	ESA / IGG
Para. 5.2	Preparation of Test Samples (mounting and delidding)	Hirex
Para. 5.3	Preparation of Test Hardware and Test Program	Hirex
Para. 5.4	Samples Check out	Hirex
Para. 5.5	Accelerator Test	Hirex
	Heavy Ion Test Report	Hirex

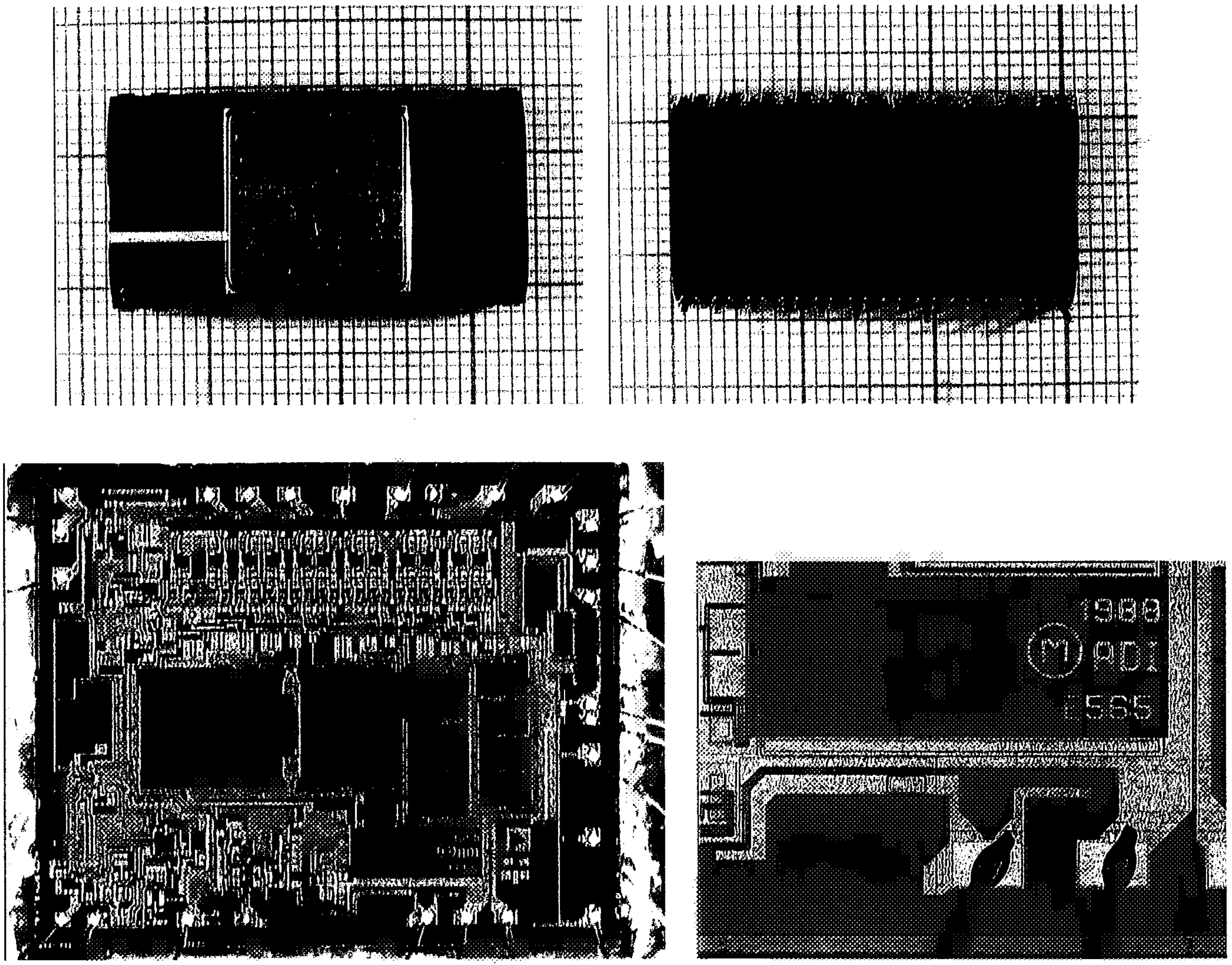
4. DEVICE AND MANUFACTURER INFORMATION

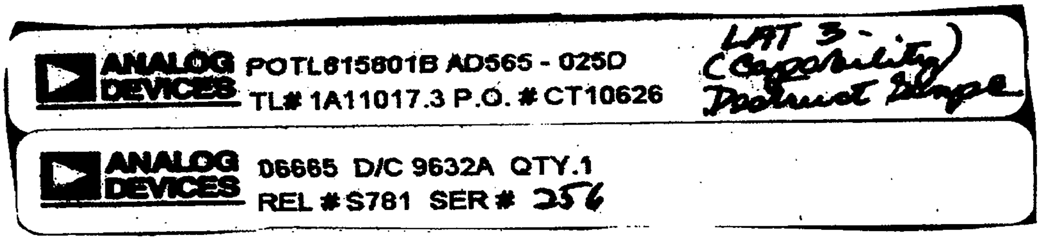
Description of the devices is as follows:

Part type :	AD565
Manufacturer :	Analog Devices
Package :	Side brazed 24-Pin DIL
Quality Level :	SCC B
Date Code :	9624A
Serial Number :	#254, #256, #257
Die Technology :	Bipolar
Die Size :	3.7 mm x 3.1 mm approximately
Die Marking :	ADI E565 1988
Tested samples :	2 (#254, #256)

External and Internal Photos are shown in Figure 1.

Figure 1 - External and Internal Photos





ANALOG DEVICES POTL615601B AD565 - 025D
TL# 1A11017.3 P.O. # CT10626

LAT 3 - (Capability) Destruct Sample

ANALOG DEVICES 06665 D/C 9632A QTY.1
REL # S781 SER # 256

5. TASK DESCRIPTION

5.1 PROCUREMENT OF TEST SAMPLES

3 hi-rel samples have been procured by ESA, and provided to HIREX.

5.2 PREPARATION OF SAMPLES

The 3 devices with the following serialized numbers #254, #256, #257, have been delidded by HIREX lab.
No sample has been mechanically damaged during this operation.

5.3 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and an application specific test board.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

The detailed principle of the test is described in §7, while an overall description of the in-house test equipment and interface board is given in appendix 1.

5.4 SAMPLES CHECK OUT

A functional test sequence has been performed on delidded samples to check that devices have not been degraded by the delidding operation.

5.5 ACCELERATOR TEST

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la neuve (Belgium) under HIREX Engineering responsibility.
2 delidded samples were irradiated, while #257 was kept as reference.

6. DESCRIPTION OF TEST FACILITIES

6.1 CYCLOTRON ACCELERATOR

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.

CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$$110\ Q^2/M$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

7. TEST PATTERN DEFINITION FOR HEAVY ION TEST

7.1 DEVICE DESCRIPTION

High Speed 12-Bit Monolithic D/A Converter
On Board High-Stability Reference
250ns max. Settling Time

7.2 TEST CONFIGURATION

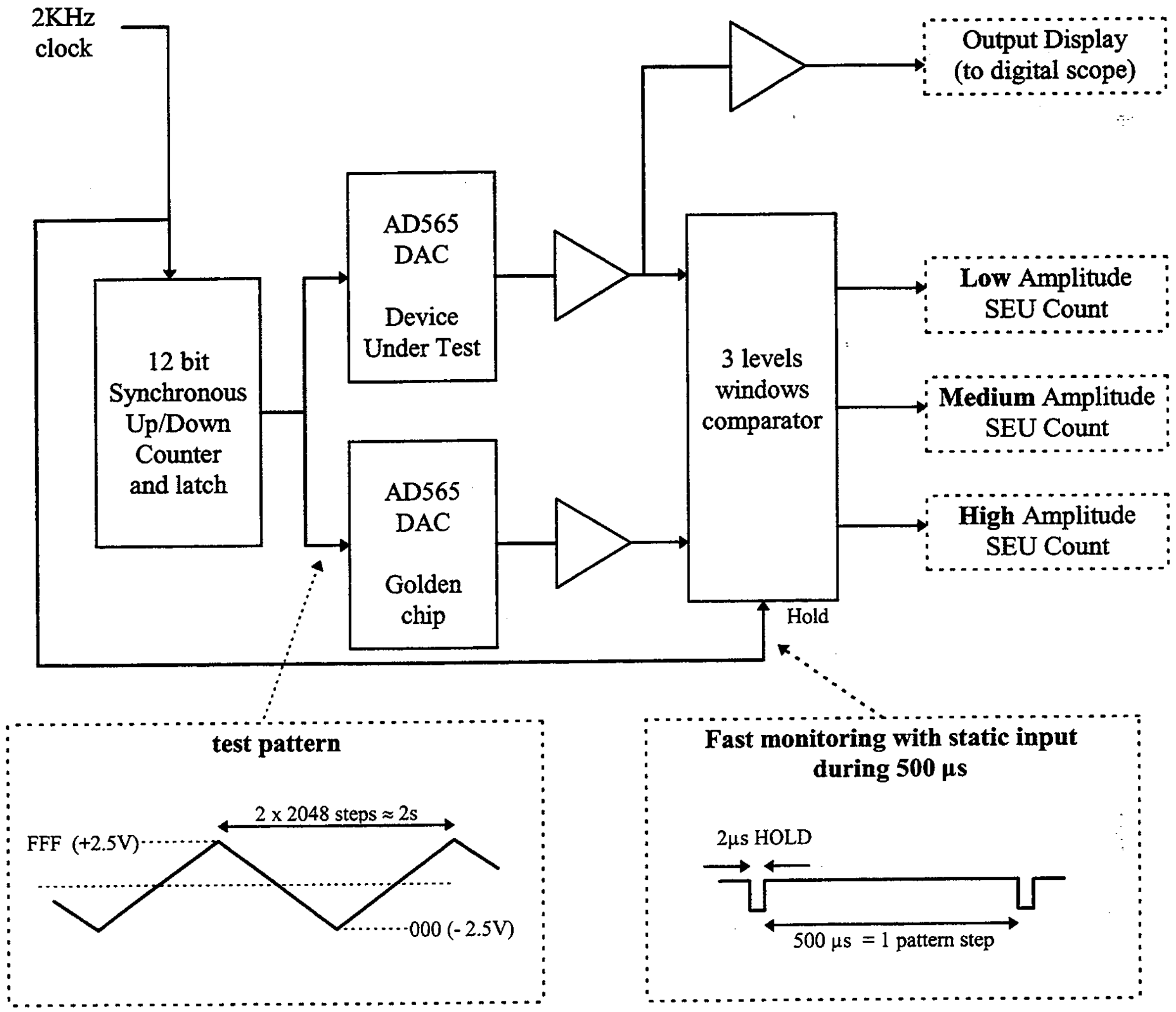
The AD565 12 bit digital to analog converter is tested with the 3 windows comparison method and slow working point variation described in appendix 1.The rationale for the pre-defined windows thresholds, is also explained.
The use of such a device allows to quantify at run time, the number of errors per amplitude range.
A second AD565 (golden chip) is used to deliver the reference signal.
Both DAC current outputs are converted into a bipolar output voltage with two external amplifiers AD847.
Full scale is fixed to ±2.5V. Slow variation of the working point is performed within the full scale limits. Both DUT and Golden chip use their own internal reference. Manual trimming procedure for both device gain and offset allows for a precise observation of 11 bits of the DAC.
The output signal is monitored with respect to the 3 window threshold levels:

"Small" amplitude = 4 / 4096 pts (5mV)
"Medium" amplitude = 64 / 4096 pts (78mV)
"Large" amplitude = 1024 4096 pts (1.25V)

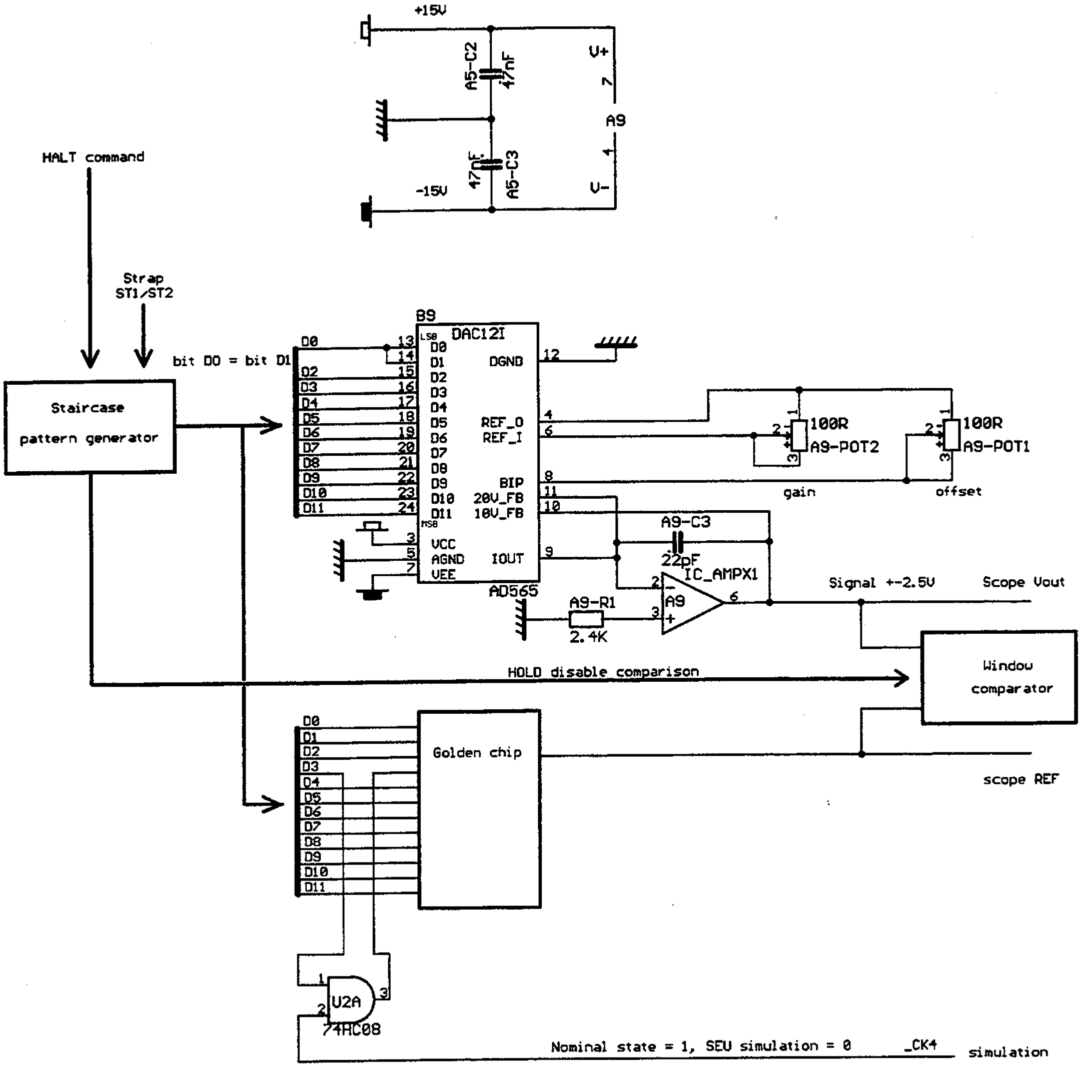
Input digital data change rate is 2KHz. An on board up/down counter produces a saw tooth digital input pattern.
The total pattern period is 2s = 2 slops x 2048 steps x 500µs
(The two LSBs D0 and D1 are connected together)
Each time the staircase input changes (every 500µs), the HOLD function produce a delayed pulse which inhibit the output comparison during 2µs. It prevent ,thus, erroneous counting during DAC & amplifier settling time (nominal delay to 0.01% is 1µs).

Figure 2 - 12-Bit D/A Converter Test Principle

AD565 12 bit D/A converter SEU test functional diagram



7.3 DEVICE CONNECTION DIAGRAM



Details on both motherboard and DUT board are provided in HRX/97.2829 document "Specific Hardware and Software Definition".

7.4 DEVICE TEST SET UP

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_Δ	function
V_L	8	+5V	10mA	18mA	5mA	5mA	Vcc control circuit
V_{A+}	9	+15V	60mA	40mA	20mA	5mA	V+ DUT & REF
V_{A-}	10	-15V	100mA	60mA	40mA	5mA	V- DUT & REF

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4			not used
CK2	4	500µs	50%	pattern generator
CK3	5	static		**HALT** mode for calibration
CK4	6	25µs	1.7s	simulation
HOLD		500µs	2µs	disable event counters during pattern transition time

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	50ns	20µs	windows analog comparator SMALL absolute amplitude > 5mV = 4/4096
CT2	18	50ns	20µs	windows analog comparator MEDIUM absolute amplitude > 48mV = 64/4096
CT3	20	50ns	20µs	windows analog comparator LARGE absolute amplitude > 1.25V = 1024/4096
CT4	22			not used

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref	5MHz	REF output (Golden chip)	(½) **±1.25V** ⇔ **±2.5V**	saw tooth pattern **±2.5V @ 0.2Hz**
Vout	50MHz	DUT output	(½) **±1.25V** ⇔ **±2.5V**	saw tooth pattern **±2.5V @ 0.2Hz**

Check test

nominal state check	HALT = 0 ⇒ saw tooth pattern **±2.5V @ 0.2Hz** HALT = 1 & STRAP ST1 ⇒ static level **+2.5V (Useful for gain calibration)** HALT = 1 & STRAP ST0 ⇒ static level **-2.5V (Useful for offset calibration)** **on board trimmers allow DUT & REF calibration within 1LSB**
upset detection check	CK4 periodically shuts down input data bit D3 (only on Golden chip) . This produces a 10 mV pulse at the output and increments only SMALL counter @ 0.6Hz

Test board

Ref. : IL043-08	**Dim. :** 141mm x 50m	**slot :** DUT 4	

8. EXPERIMENTAL TEST SET-UP

8.1 ION BEAM SELECTION

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.

Table 2 provides the ions which were used to determine the LET threshold and the asymptotic cross section within the LET range for this heavy ion characterization. In addition this table includes the ion energy, the LET, the range and the tilt angle if any.

8.2 FLUX RANGE

Particle flux was comprised between 1. x10E3 and 4. x10E4 ions/cm²/sec under normal operations (tilt 0°).

8.3 PARTICLE FLUENCE LEVELS

Fluence level was comprised between 1 x10E5 and 5 x10E5 ions/cm² under normal operations (tilt 0°).

8.4 DOSIMETRY

The current UCL Cyclotron dosimetry system and procedures were used.

8.5 ACCUMULATED TOTAL DOSE

The equivalent total dose (rad(Si)) received by each device under test is given in Table 2.

8.6 TEST TEMPERATURE RANGE

All the tests performed were conducted at ambient temperature.

9. RESULTS

Heavy ion SEE results are given in Table 2 and plotted as SEU cross section (cm²/device) versus LET for the total number of errors, in Figure 3.

From Figure 3 a), it can be seen that LET threshold has not been reached and is lower than 1,7 MeV/mg/cm². Asymptotic cross-section is found to be around 2 E-2 cm²/device.

Figure 3 b) shows the relative weight of the different errors when sorted by amplitude range. No "large" (> 1,25V) errors have been observed below 28 MeV/mg/cm², and no "medium" (78 mV - 1,25 V) errors below 5,8 MeV/mg/cm².

In Figure 4, typical waveforms of positive and negative events are provided as well as the envelop of events recorded for a set of representative runs. It can be noted that different waveform shapes have been observed.

All tested samples have received an equivalent dose (TID) below 1.0 krad.

No SEL has been detected during the different runs performed on the two samples.

Table 2 - Heavy ions tests results

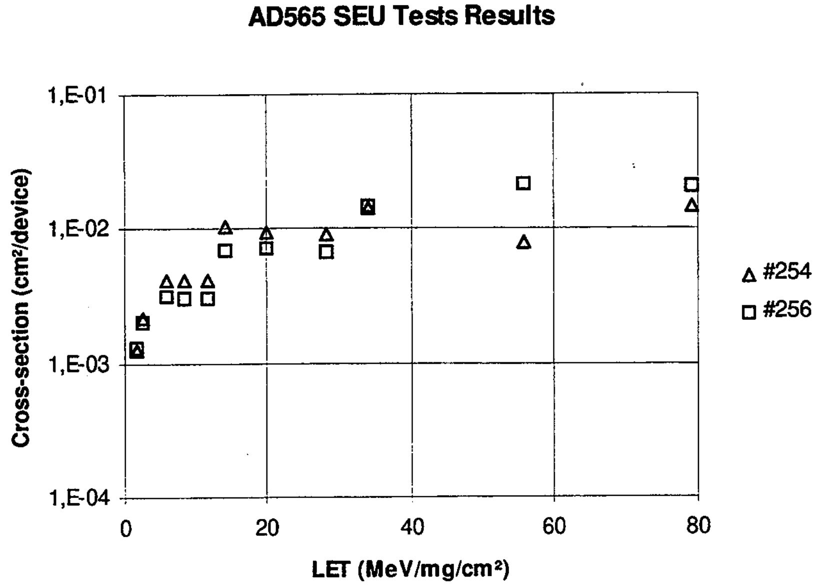
Run #	Type	S/N	Ion	Energy	LET	Tilt Angle	Range Effective	LET Effective	Time	Flux	Fluence	SEU's Error type (*)				SEU's Total	Cross Section	Dose /run	Cumulative dose /SN	Comments
				MeV	Mev/mg/cm²	°	µm (Si)	Mev/mg/cm²	s	p/cm²/s	p/cm²	1	2	3	4		cm²	rads(Si)	rads(Si)	
20	AD565	256	Xe	459	55,9	45	30,4	79,05	380	7,91E+02	100079	1832	251	15		2098	2,10E-02	1,27E+02	2,49E+02	
21	AD565	256	Xe	459	55,9	0	43,0	55,90	220	1,12E+03	100214	1879	220	21		2120	2,12E-02	8,96E+01	3,39E+02	
150	AD565	256	Kr	316	34	0	43,0	34,00	219	1,84E+03	200741	2641	272	8		2921	1,46E-02	1,09E+02	5,31E+02	
12	AD565	256	Ar	150	14,1	60	21,0	28,20	210	2,22E+03	100229	636	28	0		664	6,62E-03	4,52E+01	1,23E+02	
11	AD565	256	Ar	150	14,1	45	29,7	19,94	134	3,13E+03	100639	698	22	0		720	7,15E-03	3,21E+01	7,74E+01	
9	AD565	256	Ar	150	14,1	0	42,0	14,10	160	4,43E+03	100090	673	18	0		691	6,90E-03	2,26E+01	2,26E+01	
10	AD565	256	Ar	150	14,1	0	42,0	14,10	130	4,43E+03	100662	693	18	0		711	7,06E-03	2,27E+01	4,53E+01	
144	AD565	256	Ne	78	5,85	60	22,5	11,70	146	5,34E+03	200399	609	5	0		614	3,06E-03	3,75E+01	4,22E+02	
142	AD565	256	Ne	78	5,85	45	31,8	8,27	109	7,56E+03	201774	624	3	0		627	3,11E-03	2,67E+01	3,66E+02	
143	AD565	256	Ne	78	5,85	0	45,0	5,85	79	1,07E+04	200428	627	0	0		627	3,13E-03	1,88E+01	3,84E+02	
190	AD565	256	B	41	1,7	45	56,6	2,40	126	2,60E+04	503874	1027	0	0		1027	2,04E-03	1,93E+01	5,50E+02	
191	AD565	256	B	41	1,7	0	80,0	1,70	77	3,68E+04	504924	652	0	0		652	1,29E-03	1,37E+01	5,64E+02	
36	AD565	254	Xe	459	55,9	45	30,4	79,05	196	7,91E+02	101112	1331	173	10		1514	1,50E-02	1,28E+02	2,18E+02	
35	AD565	254	Xe	459	55,9	0	43,0	55,90	203	1,12E+03	100318	706	95	5		806	8,03E-03	8,97E+01	8,97E+01	
152	AD565	254	Kr	316	34	0	43,0	34,00	276	1,84E+03	200371	2603	231	3		2837	1,42E-02	1,09E+02	6,10E+02	
133	AD565	254	Ar	150	14,1	60	21,0	28,20	223	2,22E+03	200321	1759	65	1		1825	9,11E-03	9,04E+01	4,18E+02	
132	AD565	254	Ar	150	14,1	45	29,7	19,94	152	3,13E+03	201751	1880	46	0		1926	9,55E-03	6,44E+01	3,27E+02	
131	AD565	254	Ar	150	14,1	0	42,0	14,10	113	4,43E+03	201693	2091	56	0		2147	1,06E-02	4,55E+01	2,63E+02	
134	AD565	254	Ne	78	5,85	60	22,5	11,70	84	5,34E+03	201190	841	5	0		846	4,20E-03	3,77E+01	4,56E+02	
135	AD565	254	Ne	78	5,85	45	31,8	8,27	62	7,56E+03	200540	836	4	0		840	4,19E-03	2,65E+01	4,82E+02	
136	AD565	254	Ne	78	5,85	0	45,0	5,85	43	1,07E+04	204879	846	3	0		849	4,14E-03	1,92E+01	5,01E+02	
186	AD565	254	B	41	1,7	45	56,6	2,40	93	2,60E+04	503937	1092	0	0		1092	2,17E-03	1,94E+01	6,30E+02	
187	AD565	254	B	41	1,7	0	80,0	1,70	81	3,68E+04	503325	624	0	0		624	1,24E-03	1,37E+01	6,43E+02	

*Error types:

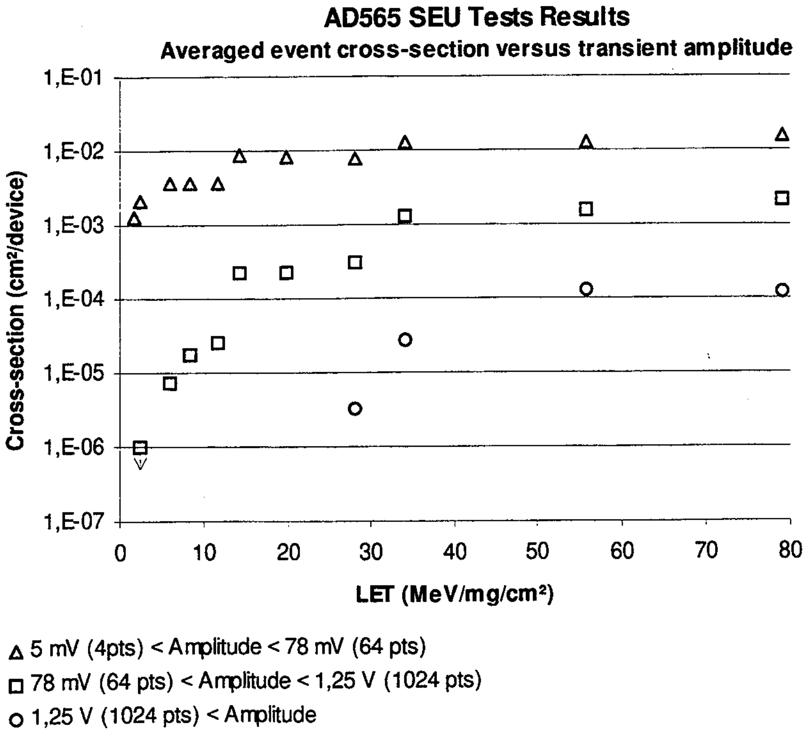
1	5 mV (4 pts)	< Error amplitude <	78 mV (64 pts)
2	78 mV (64 pts)	< Error amplitude <	1,25 V (1024 pts)
3	1,25 V (1024 pts)	< Error amplitude	
4	Not used		

Figure 3 - AD565 SEU Test Results

a) Total SEU error number per irradiated sample



b) Average SEU error number per transient amplitude range



10. CONCLUSION

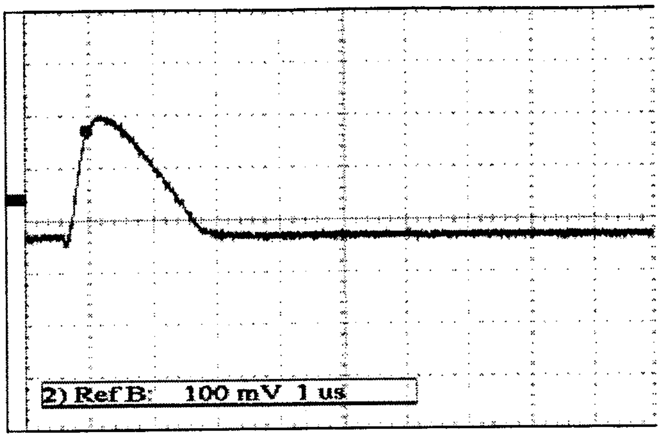
SEU test have been conducted on AD565 12-Bit D/A Converter from Analog Devices, using the heavy ions available at the University of Louvain facility.

SEU susceptibility was obtained through the cross section versus LET curve for the three different transient amplitude ranges (small, medium and large, respectively 5 mV-78 mV, 78 mV-1,25 V, and >1,25 V).

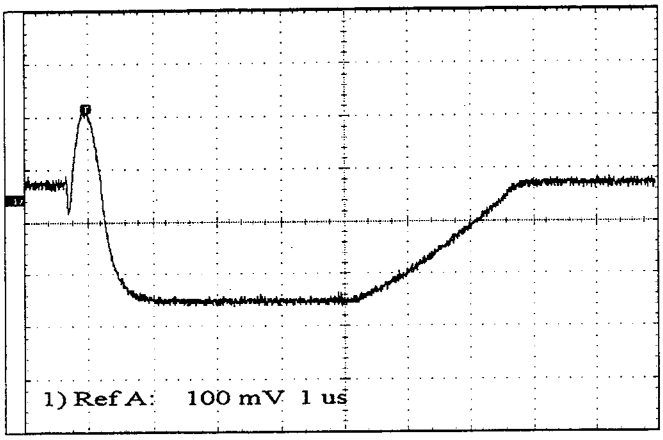
With these results upset predictions on XMM orbit, can be performed for each error amplitude range

In Figure 4, from run 152 - see Table 2 for run details -., it can be seen that both positive and negative errors are as high as ±2,5V (MSB), but are not symmetrical and each pulse width corresponds to few microseconds.

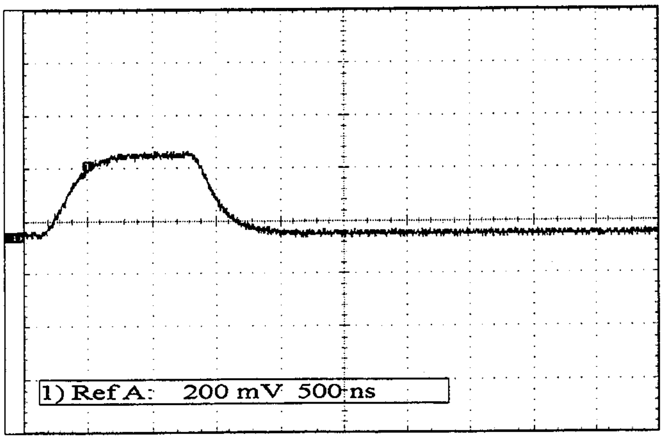
Lastly, no SEL has been detected during the different runs performed on the two samples.



Typical event waveform



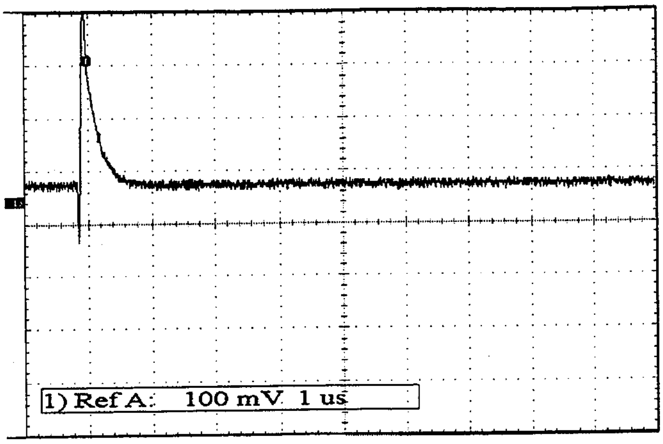
Typical event waveform



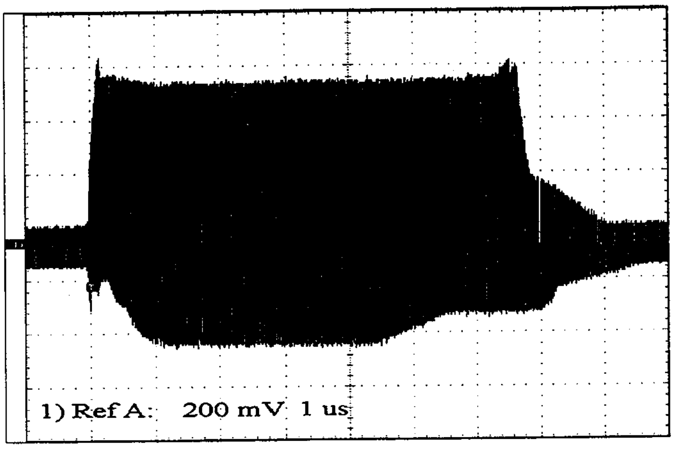
Typical event waveform

(Observed signal to be multiplied by a factor of 2 to obtain the actual amplitude)

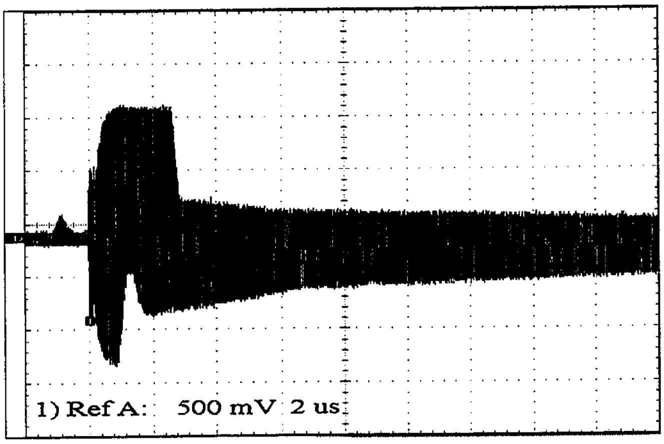
Figure 4 - Scope observation of SEUs



Typical event waveform



Run150 Envelop



Run 152 Envelop

(Observed signal to be multiplied by a factor of 2 to obtain the actual amplitude)

Each different run number corresponds to a given run listed in Table 2

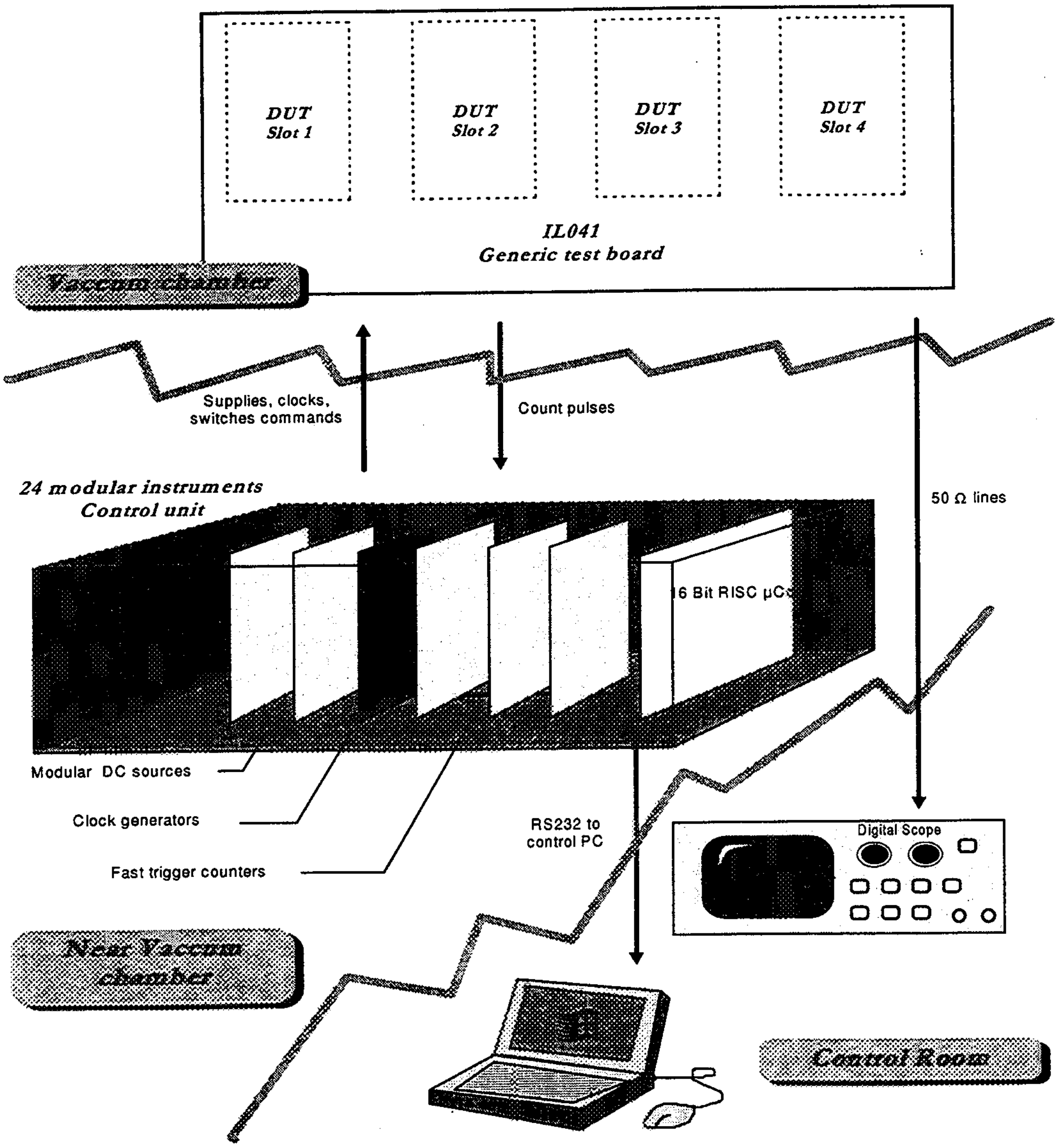
Figure 4 - Scope observation of SEUs (cont'd)

Appendix 1

Test set-up

The complete test equipment is constituted of:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 4 devices
- A digital oscilloscope to store analog upset waveform.

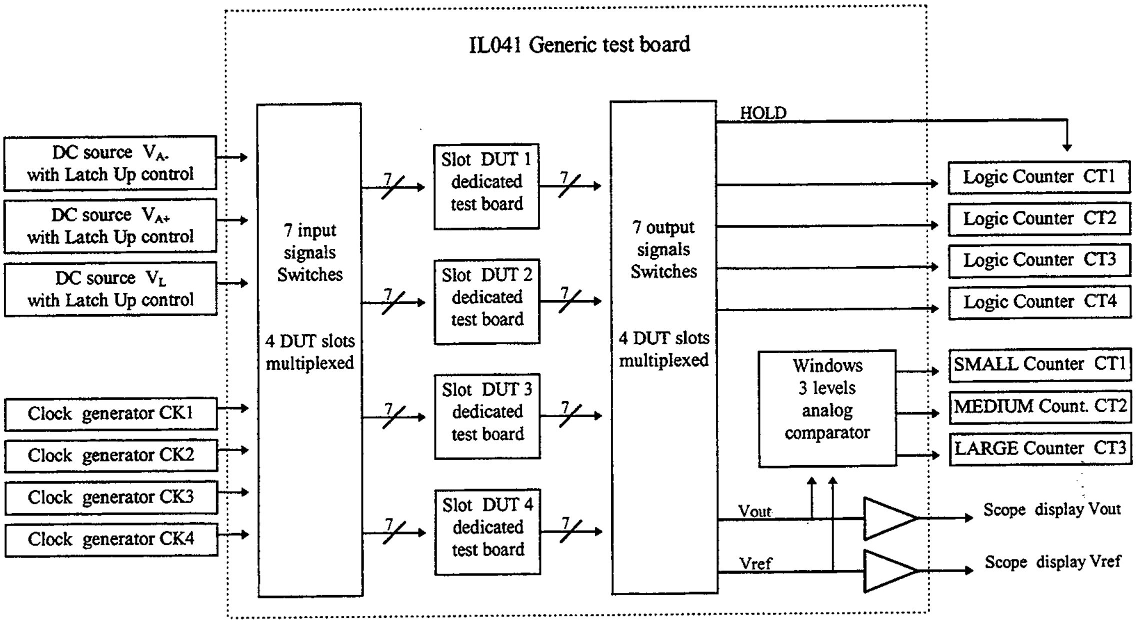


Mother board description (ref. IL041)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each DUT board slot , the following signals can be considered:

- seven inputs signals
    - 3 programmable power supplies
    - 4 programmable clocks
- seven output signals
    - 4 logic counting signals
    - 2 analog signals : DUT output and Ref . output
    - 1 HOLD signal which can inhibit temporarily the counters.

- Each device needs a dedicated plug-in test board compatible with IL041 mother board.
- IL041 board has been designed to comply with Louvain Test facilities .
- The number of slots is limited to four
  Operation is multiplexed and only one slot is powered at one time.



DUT Test board description

The device under test is mounted on a specific board support which is plugged onto the motherboard.
Mechanical outlines : 141 mm x 50 mm , wrapping or printed circuit board with two 20 pins connectors.
According to test set up and device operating conditions, the test board can accept the mounting of :

- The DUT package with beam positioning constraints (unique for Louvain facilities)
- The golden chip
- The pattern generator
- any interface circuit such as buffer, latches ...
- a standalone micro controller if necessary...

Note : beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

Three Windows analog comparator

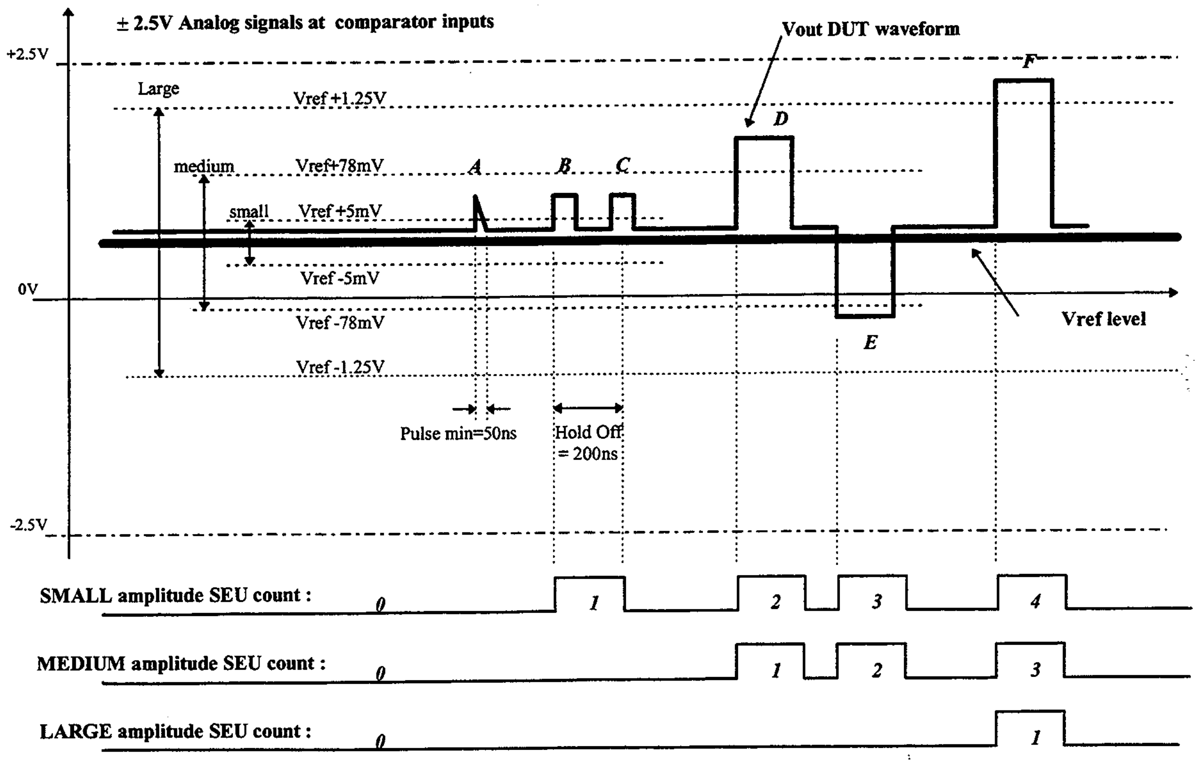
Applications :
Single analog output devices, including DAC, can be monitored with a generic 3 windows fast comparator associated to 3 counter modules .

Test principle :
Each window uses pre-defined levels centered around the awaited working point :

- The SMALL window uses the lowest levels compatible with the hardware limitation (offset, noise ...)
- The LARGE window is for counting major DUT output perturbations : Vout max /2 or DAC MSB...
- The MEDIUM window has been defined using a geometric progression between SMALL and LARGE

To illustrate how it works, the here after figure gives an example of timing diagram :
Both DUT and Ref. working point can vary within the ±2.5V allowed input range (+1V in the example).
6 transient pulses can be seen on the DUT Vout record :

- Pulse A will not be counted as its width is shorter than Pulse min parameter
- Pulse B and C : Only B will be counted as the time between B and C is less than the Hold Off parameter (this prevents of multiple counting in case of large degraded transient)
- Pulse D and E : Both pulses will be counted as the comparator works whatever polarity.
- Pulse F is an example of large event . It can be noticed that a large event is also counted as a medium and a small as well.



Interest :
The use of this principle allows for straightforward analysis of the test data, at run time. So, it is easy to react and adjust the beam conditions to obtain proper data. When preparing the report, it also shortens the subsequent run recorded data analysis exercise.
Lastly, using 3 different levels at a time, reduces the number of runs needed for the device characterization

ADC converters :
The here above method can also be transposed to the test of ADCs. In that case, the 3 windows analog comparator is replaced by a simple standalone micro controller witch execute the same windowing operation by soft.

Working point variation and HOLD function :
This window comparison is compatible with low frequency working point variation (few Hertz) . This is particularly useful with ADC and DAC devices : Saw tooth input pattern can be used to test the device with a uniform digital code distribution. In that case, the input saw tooth is rather a stair case signal. HOLD function allows to inhibit comparison and counting each time the pattern changes.

Test signals definition

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_Δ	function
V_L	8						
V_{A+}	9						
V_{A-}	10						

- **signals** V_L , V_{A+} & V_{A-} are 3 DC sources with constant voltage / current characteristic, software monitoring, Latch Up threshold detection, delayed start & stop triggering
- **module :** Slot position used by hardware & software control system
- U_{Reg} **:** DC source set up for constant voltage operation
- I_{max}: DC source set up for constant current operation, useful on large DUT latch up or failure
- I_{LU}: software Latch Up detection current threshold
- I_{nom}: nominal current when DUT operates properly
- I_Δ: minimum current measurement change required for event memory write
- **function:** DC source assignment (DUT or test board auxiliary device)

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}

- T_{wait} Sustaining Latch Up time (delay between detection and DC sources shut down)
- T_{off} Off state duration
- $T_{set\ up}$ x 3 Restart triggering Delay between the different internal sequential levels
- T_{LU} Total latch Up sequence duration

clocks & commands

signal	module	period	pulse width	function
CK1	4			
CK2	4			
CK3	5			
CK4	6			
HOLD				

- **CK 1, CK2, CK3, CK 4** are 4 dedicated programmable logic signals (static or dynamic) which can be used for DUT Clock, DUT mode selection , Upset simulation ...
- **HOLD** is a dedicated signal generated by the test board circuitry ; HOLD = 1 disable all the event counters when the analog comparison is not available, during DUT level transitions ...

Event counters

signal	module	Pulse min.	Hold Off	function
CT1	16			SMALL or Logic event 1
CT2	18			MEDIUM or Logic event 2
CT3	20			LARGE or Logic event 3
CT4	22			Logic event 4

- signals CT1 ... CT4 are 4 count input channels , either for straightforward logic event acquisition or for window analog comparator acquisition
- Pulse min : minimum pulse width required , according to overall system bandwidth
- Hold Off: minimum delay imposed between the detection of two consecutive events

oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

- **signals Vref** and **Vout** are the 2 analog input channels for both analog comparator and digital scope
- **Bandwidth:** overall channel bandwidth
- **gain:** channel gain between actual DUT level and scope displayed level

Note : The oscilloscope can be triggered by one of the event counter input signal CT1 ... CT4

Check test

nominal state check	
upset detection check	

To check that the device is operating properly, this test can be perform at any time under software control. The use of CK4 signal allows for two different modes :

- **nominal state check** : CK4 disable , absence of any event
- **upset detection check** : CK4 enable, presence of calibrated simulated event periodically introduced at a slow rate

Test board

Ref. : IL043-xx	**Dim. :**	**slot :**	

- Each set up is dedicated to a specific slot number, in order to ensure that each device is tested with the proper set up conditions.