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# RADIATION TEST REPORT

**Heavy Ions Testing of**

**AD571**

**10-Bit A/D Converter**

**from Analog Devices**

ESA Purchase Order No 171720 dated 22/07/97

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

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## 1. INTRODUCTION

This report presents the results of a heavy ion Single Event Effects (SEEs) test program carried out for the XMM project on Analog Devices AD571 10-Bit A/D Converter. Flight lot devices were tested at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.
The main aims of these tests were to assess the AD571's susceptibility to Single Event Upsets (SEUs) and Single Event Latch-ups (SELs) by heavy ion. Tests were performed in such a way that the SEU cross sections can be plotted over a wide LET range in order to allow computation of the SEU rates in XMM orbit.

This work was performed for ESA/ESTEC under P.O. No 171720 dated 20/07/97.

## 2. APPLICABLE DOCUMENTS

The following documents are applicable:
- XMM SOW QCA/RHS-XMM.DOC July 97 (fax dated 11 July, 97),
- Test Set-up Specification for heavy ion testing of XMM devices - Hirex Doc No HRX/97.2598 Issue 1 Rev. A dated 7 August 1997 -

### 2.1 REFERENCE DOCUMENTS

- Analog Devices, AD571 data sheet.
- Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
- The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

## 3. ORGANIZATION OF ACTIVITIES

The different tasks performed during this evaluation have been conducted in the order shown in Table 1 by the relevant company.

**Table 1 - Organization of activities**

| | | |
|---|---|---|
| Para. 5.1 | Procurement of Test Samples (Hi-rel serialized devices) | ESA / MMS UK |
| Para. 5.2 | Preparation of Test Samples (mounting and delidding) | Hirex |
| Para. 5.3 | Preparation of Test Hardware and Test Program | Hirex |
| Para. 5.4 | Samples Check out | Hirex |
| Para. 5.5 | Accelerator Test | Hirex |
| | Heavy Ion Test Report | Hirex |

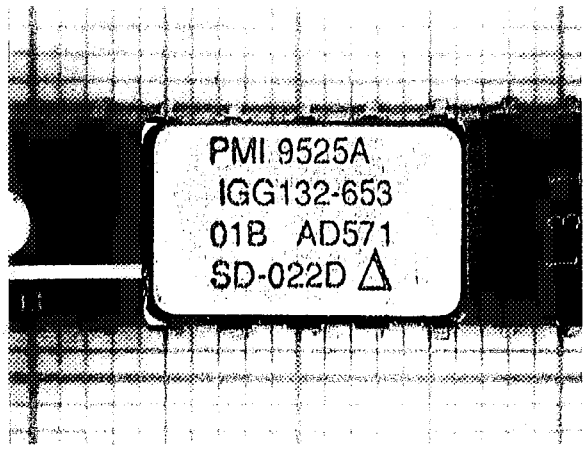
## 4. DEVICE AND MANUFACTURER INFORMATION

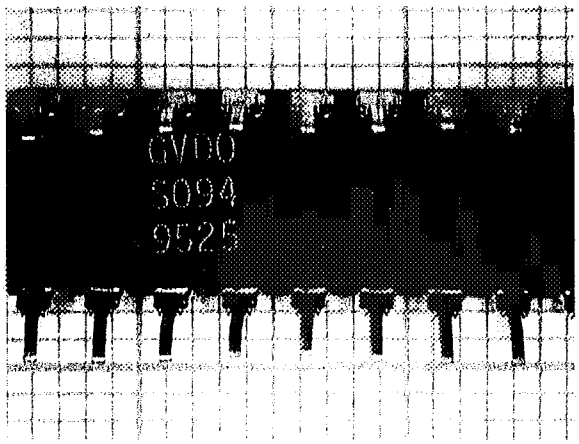
Description of the devices is as follows:

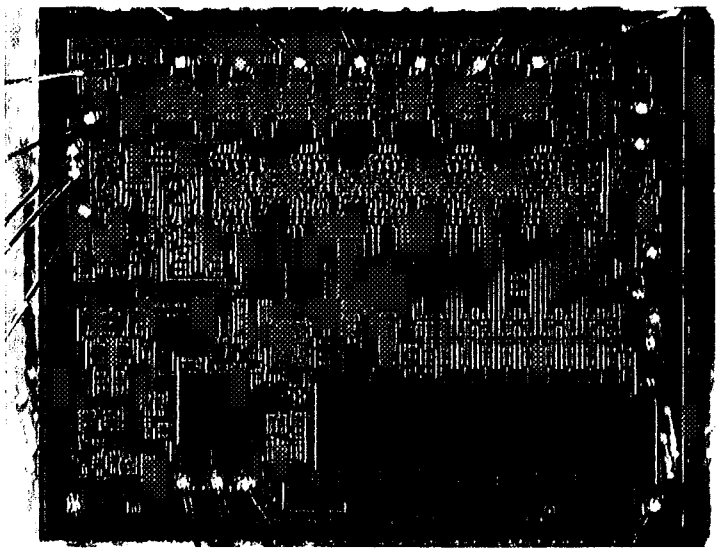
| | |
|---|---|
| Part type : | AD571 |
| Manufacturer : | Analog Devices |
| Package : | Side brazed 18-Pin DIL |
| Quality Level : | SCC B |
| Date Code : | 9525A |
| Serial Number : | #131, #132, #133 |
| Die Technology : | Bipolar |
| Die Size : | 4.0 mm x 3.2 mm approximately |
| Die Marking : | 571D |
| Tested samples : | 2 ( #132, #134) |

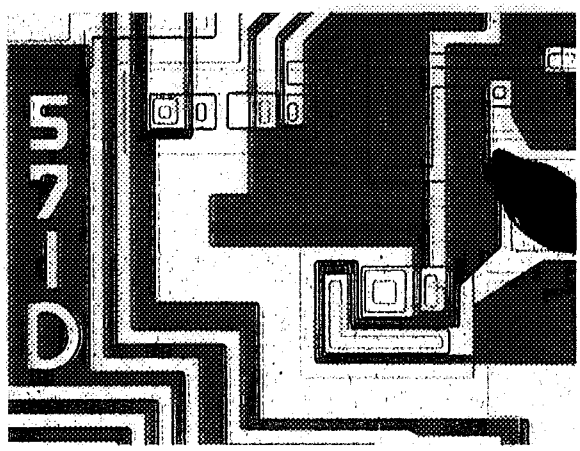
External and Internal Photos are shown in Figure 1.

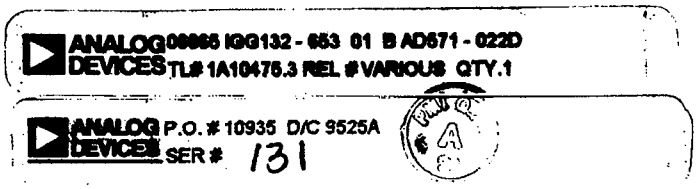
**Figure 1 - External and Internal Photos**





# 5. TASK DESCRIPTION

## 5.1 PROCUREMENT OF TEST SAMPLES

3 hi-rel samples have been procured by ESA, and provided to HIREX.

## 5.2 PREPARATION OF SAMPLES

The 3 devices with the following serialized numbers #131, #132, #134, have been delidded by HIREX lab.
No sample has been mechanically damaged during this operation.

## 5.3 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and an application specific test board.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

The detailed principle of the test is described in §7, while an overall description of the in-house test equipment and interface board is given in appendix 1.

## 5.4 SAMPLES CHECK OUT

A functional test sequence has been performed on delidded samples to check that devices have not been degraded by the delidding operation.

## 5.5 ACCELERATOR TEST

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la neuve (Belgium) under HIREX Engineering responsibility.
2 delidded samples were irradiated, while #131 was kept as reference.

## 6. DESCRIPTION OF TEST FACILITIES

### 6.1 CYCLOTRON ACCELERATOR

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.

CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$$110Q2/M$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

## 7. TEST PATTERN DEFINITION FOR HEAVY ION TEST

### 7.1 DEVICE DESCRIPTION

10-Bit A/D Converter with reference and clock
25 µs maximum conversion time.

### 7.2 TEST CONFIGURATION

The AD571 10 bit analog to digital converter is tested with the 3 windows comparison method described in appendix 1.The rationale for the pre-defined windows thresholds, is also explained. The use of such a method allows to quantify at run time, the number of errors per amplitude range.

The unipolar input signal full scale is fixed to 10V, according to DUT internal reference. Working point variation is performed within the full scale limits, via 64 steps uniformly distributed.

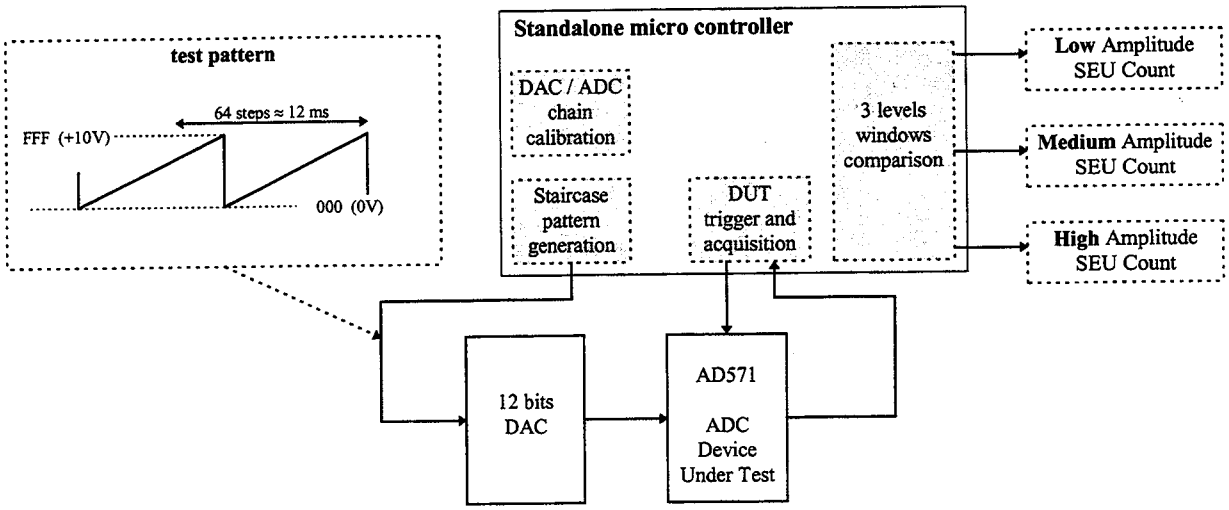
The output digital code is monitored with respect to the 3 window threshold levels:

| | |
|---|---|
| SMALL amplitude = 4 / 1024 pts | (39 mV) |
| MEDIUM amplitude = 32 / 1024 pts | (312 mV) |
| LARGE amplitude = 256 1024 pts | (2.5 V) |

The nominal DUT conversion time is 25µs.
The conversion period is fixed to 200µs, in order to comply with the micro controller computational speed.

## Figure 2 - 10-Bit A/D Converter Test Principle

**AD571 10 bit A/D converters SEU test functional diagram**




Onboard standalone micro controller is used to :

- generate via a12 bit DAC a saw tooth analog input signal,
- trig and read back the ADC under test,
- perform before the test runs a software calibration of the DAC and ADC chain, using an on board EPROM to store the measurement data,
- compute during the run, the absolute difference between previous read data stored within the EPROM during calibration and run data,
- output count pulses when upsets occur, with respect to the 3 different comparison window amplitudes.

The input pattern generated by the micro controller consist in a 64 steps stair case. A uniform digital code distribution is obtained by a linear progression of the 5 MSB and the 5 LSB.

It has been decided to operated the DUT in the following way :
As soon as "End of Conversion" signal is received ,(Max. conversion time is 25µs), the micro-controller acquires the output data word within 15µs, then perform de computing within the 200µs total cycle. It means that data can be corrupted only during 40µs (20% of the overall cycle).

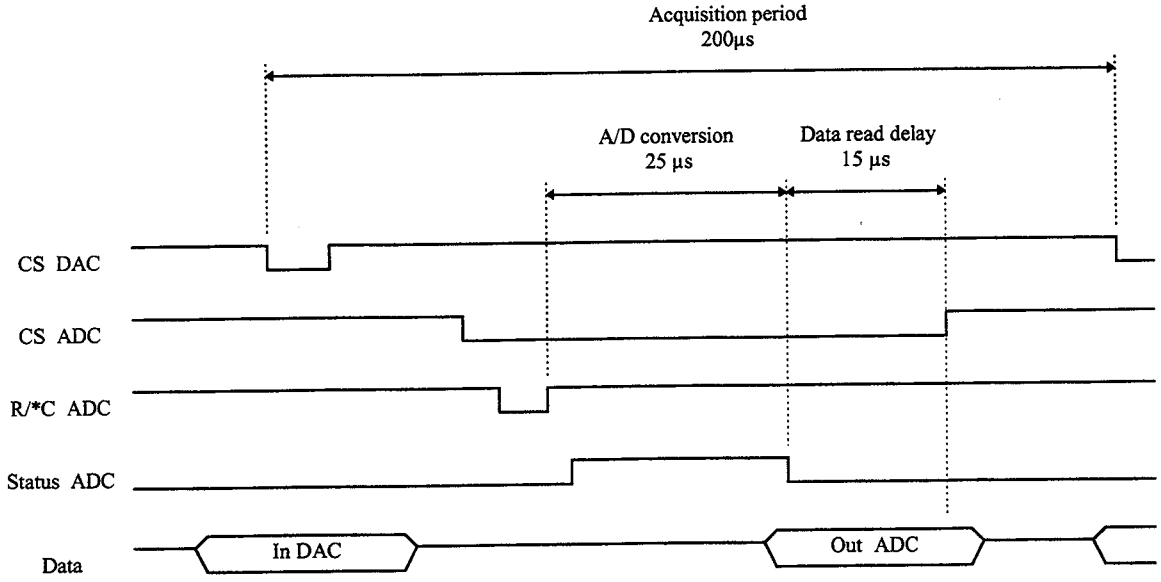
The configuration which consists in keeping the data into the ADC output register until the next acquisition cycle has not been considered as it may dramatically increases the SEU sensitivity of the electronic design.

**Note:**

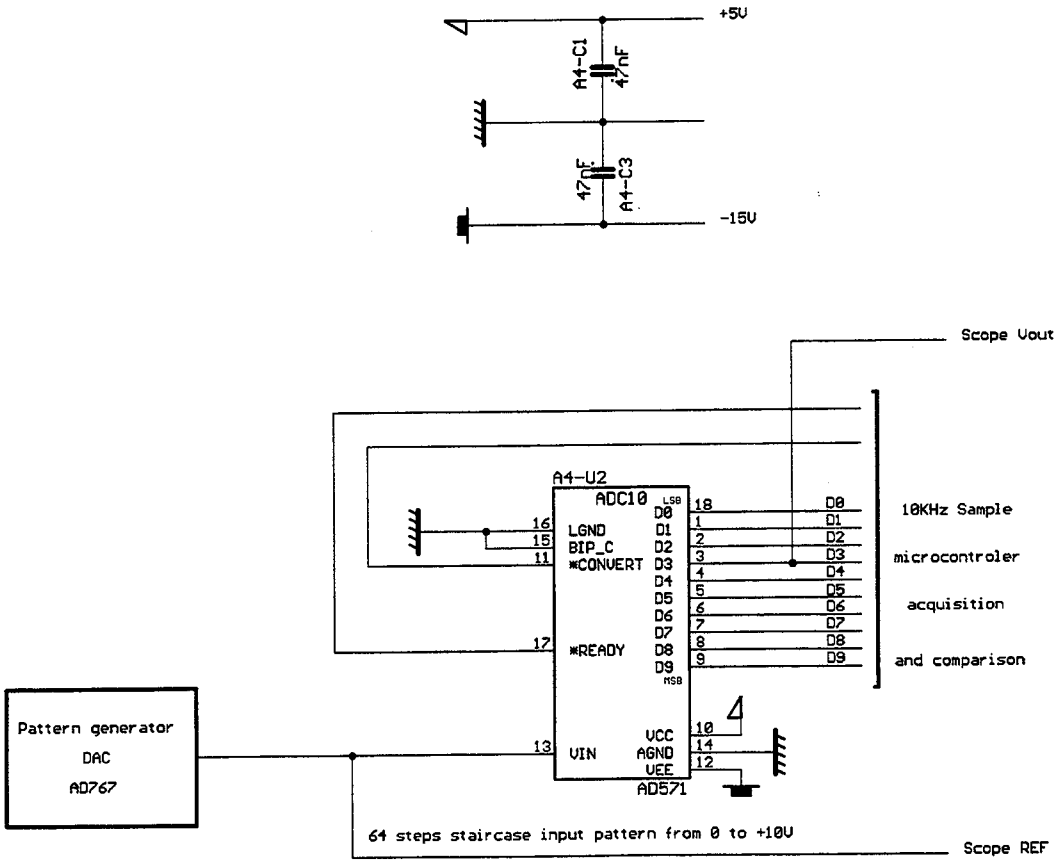
In the actual space application, providing that acquisition of the conversion data is performed as soon as the "End of Conversion" signal is received, it is easy to extrapolate the data to lower conversion operation frequencies:
For instance, if the device is operated at 1 kHz, SEE cross section results presented in Table 2 have to be divided by a factor of 5.

On the other hand, if a different operating configuration is used, that is to say, converted data are kept in the output DUT registers for a given time before acquisition starts, SEE cross section values might be much different.

**Figure 3 - Conversion DA / AD Timing diagram**




## 7.3 DEVICE CONNECTION DIAGRAM




Details on both motherboard and DUT board are provided in HRX/97.2829 document "Specific Hardware and Software Definition".

## 7.4 DEVICE TEST SET UP

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

**Supplies**

| signal | module | $U_{Reg}$ | $I_{max}$ | $I_{LU}$ | $I_{nom}$ | $I_{\Delta}$ | function |
|---|---|---|---|---|---|---|---|
| $V_L$ | 8 | +5V | 50mA | 25mA | 12mA | 1mA | Vcc DUT & µC |
| $V_{A+}$ | 9 | +15V | 50mA | | 12mA | 5mA | V+ DAC |
| $V_{A-}$ | 10 | -15V | 80mA | 50mA | 25mA | 1mA | V- DUT & DAC |

**Latch Up timing**

| $T_{wait}$ | $T_{off}$ | $T_{set\ up}$ x 3 | $T_{LU}$ |
|---|---|---|---|
| 20ms | 100ms | 10ms | 150ms |

**Clocks & commands**

| signal | module | period | pulse width | function |
|---|---|---|---|---|
| CK1 | 4 | 10MHz | | standalone micro controller |
| CK2 | 4 | | | |
| CK3 | 5 | static | | calibration mode selection |
| CK4 | 6 | 25µs | 1.7s | simulation |
| HOLD | | | | |

**Event counters**

| signal | module | pulse min. | Hold Off | function |
|---|---|---|---|---|
| CT1 | 16 | 200µs | 200µs | windows software comparison<br>SMALL absolute amplitude > 20mV = 4/1024 |
| CT2 | 18 | 200µs | 200µs | windows software comparison<br>MEDIUM absolute amplitude > 156mV = 32/1024 |
| CT3 | 20 | 200µs | 200µs | windows software comparison<br>LARGE absolute amplitude > 2.5V = 256/1024 |
| CT4 | 22 | | | not used |

**Oscilloscope monitoring @50Ω**

| signal | Bandwidth | function | gain | nominal level |
|---|---|---|---|---|
| Vref | 5MHz | DAC output | (1/10) **+1 V ⇔ +10V** | 64 steps staircase pattern<br>**from 0 to 10V @ 78Hz** |
| Vout | | output data bit D3 | | |

**Check test**

| | |
|---|---|
| **nominal state check** | CK3 = 0 ⇒ staircase pattern from 0 to 10V @ 78Hz (LED1 ON)<br>CK3 = 1 ⇒ software calibration with onboard EPROM recording (LED2 ON) |
| **upset detection check** | CK4 periodically offsets the pattern DAC<br>This produces a 20 mV pulse at the output<br>and increments only SMALL counter @ 0.6Hz |

**Test board**

| | | | |
|---|---|---|---|
| **Ref. : IL043-09** | **Dim.** : 141mm x 50m | **slot :** DUT 2 | |

## 8. EXPERIMENTAL TEST SET-UP

### 8.1 ION BEAM SELECTION

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.

Table 2 provides the ions which were used to determine the LET threshold and the asymptotic cross section within the LET range for this heavy ion characterization. In addition this table includes the ion energy, the LET, the range and the tilt angle if any.

### 8.2 FLUX RANGE

Particle flux was comprised between 1. x10E3 and 4.5 x10E3 ions/cm²/sec under normal operations (tilt 0°).

### 8.3 PARTICLE FLUENCE LEVELS

Fluence level was comprised between 1 x10E5 and 5 x10E5 ions/cm² under normal operations (tilt 0°).

### 8.4 DOSIMETRY

The current UCL Cyclotron dosimetry system and procedures were used.

### 8.5 ACCUMULATED TOTAL DOSE

The equivalent total dose (rad(Si)) received by each device under test is given in Table 2.

### 8.6 TEST TEMPERATURE RANGE

All the tests performed were conducted at ambient temperature.

## 9. RESULTS

Heavy ion SEE results are given in Table 2 and plotted as SEU cross section ($cm^2$/device) versus LET for the total number of errors, in Figure 4.

Without taking into account the point at 14,1 MeV/mg/cm², for which only one error was counted, it can be considered that LET threshold is closed to 28 MeV/mg/cm², - see Figure 4 a) -.
Asymptotic cross-section is found to be around 2 E-4 cm²/device.

Figure 4 b) shows the relative weight of the different errors when sorted by amplitude range.
No "large" (> 256 pts) errors have been observed below 48 MeV/mg/cm², and no "medium" errors (32 pts - 256 pts) below 34 MeV/mg/cm².

All tested samples have received an equivalent dose (TID) below 2.0 krads.

No SEL has been detected during the different runs performed on the two samples.

**Table 2 - Heavy ions tests results**

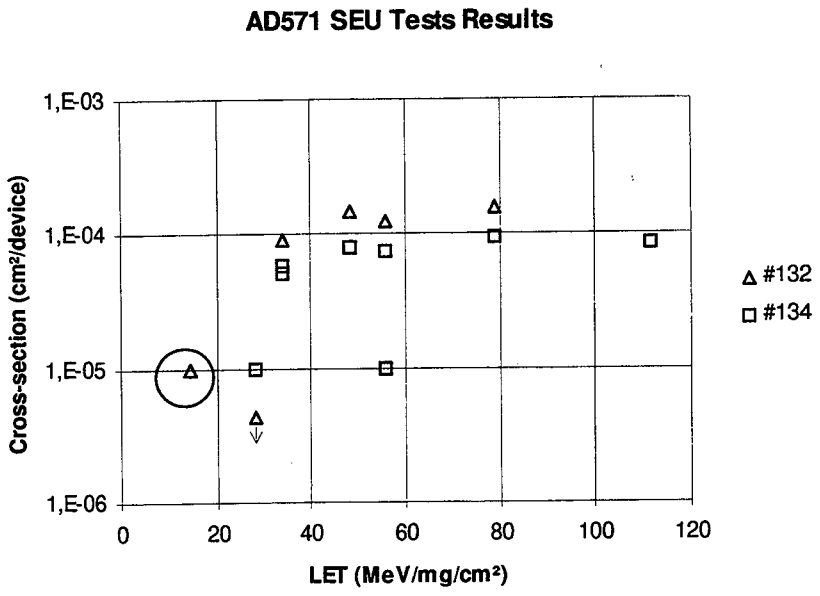
| Run # | Type | S/N | Ion | Energy | LET | Tilt Angle | Range Effective | LET Effective | Time | Flux | Fluence | SEU's | | | | | Cross Section | Dose /run | Cumulative dose /SN | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | Error type (*) | | | | Total | | | | |
| | | | | MeV | Mev/mg/cm² | ° | µm (Si) | Mev/mg/cm² | s | p/cm²/s | p/cm² | 1 | 2 | 3 | 4 | | cm² | rads(Si) | rads(Si) | |
| 24 | AD571 | 132 | Xe | 459 | 55,9 | 45 | 30,4 | 79,05 | 402 | 7,91E+02 | 100026 | 14 | 1 | 1 | 0 | 16 | 1,60E-04 | 1,27E+02 | 3,41E+02 | |
| 17 | AD571 | 132 | Xe | 459 | 55,9 | 0 | 43,0 | 55,90 | 259 | 1,12E+03 | 97541 | 10 | 2 | 0 | 0 | 12 | 1,23E-04 | 8,72E+01 | 2,15E+02 | |
| 147 | AD571 | 132 | Kr | 316 | 34 | 45 | 30,4 | 48,08 | 165 | 1,30E+03 | 502644 | 69 | 6 | 0 | 0 | 75 | 1,49E-04 | 3,87E+02 | 7,28E+02 | |
| 148 | AD571 | 132 | Kr | 316 | 34 | 0 | 43,0 | 34,00 | 110 | 1,84E+03 | 502208 | 45 | 1 | 0 | 0 | 46 | 9,16E-05 | 2,73E+02 | 1,00E+03 | |
| 16 | AD571 | 132 | Ar | 150 | 14,1 | 60 | 21,0 | 28,20 | 454 | 2,22E+03 | 231972 | 0 | 0 | 0 | 0 | 0 | | 1,05E+02 | 1,27E+02 | |
| 15 | AD571 | 132 | Ar | 150 | 14,1 | 0 | 42,0 | 14,10 | 161 | 4,43E+03 | 100270 | 1 | 0 | 0 | 0 | 1 | 9,97E-06 | 2,26E+01 | 2,26E+01 | |
| 31 | AD571 | 134 | Xe | 459 | 55,9 | 60 | 21,5 | 111,80 | 446 | 5,59E+02 | 200072 | 14 | 0 | 3 | 0 | 17 | 8,50E-05 | 3,58E+02 | 7,91E+02 | |
| 30 | AD571 | 134 | Xe | 459 | 55,9 | 45 | 30,4 | 79,05 | 314 | 7,91E+02 | 200000 | 15 | 2 | 2 | 0 | 19 | 9,50E-05 | 2,53E+02 | 4,33E+02 | |
| 29 | AD571 | 134 | Xe | 459 | 55,9 | 0 | 43,0 | 55,90 | 126 | 1,12E+03 | 201164 | 2 | 0 | 0 | 0 | 2 | 9,94E-06 | 1,80E+02 | 1,80E+02 | |
| 32 | AD571 | 134 | Xe | 459 | 55,9 | 0 | 43,0 | 55,90 | 319 | 1,12E+03 | 200764 | 13 | 2 | 0 | 0 | 15 | 7,47E-05 | 1,80E+02 | 9,70E+02 | |
| 155 | AD571 | 134 | Kr | 316 | 34 | 45 | 30,4 | 48,08 | 158 | 1,30E+03 | 501024 | 36 | 3 | 1 | 0 | 40 | 7,98E-05 | 3,85E+02 | 1,45E+03 | |
| 156 | AD571 | 134 | Kr | 316 | 34 | 0 | 43,0 | 34,00 | 37 | 1,84E+03 | 455210 | 25 | 2 | 0 | 0 | 27 | 5,93E-05 | 2,48E+02 | 1,69E+03 | |
| 157 | AD571 | 134 | Kr | 316 | 34 | 0 | 43,0 | 34,00 | 145 | 1,84E+03 | 501357 | 26 | 0 | 0 | 0 | 26 | 5,19E-05 | 2,73E+02 | 1,97E+03 | |
| 127 | AD571 | 134 | Ar | 150 | 14,1 | 60 | 21,0 | 28,20 | 177 | 2,22E+03 | 200867 | 2 | 0 | 0 | 0 | 2 | 9,96E-06 | 9,06E+01 | 1,06E+03 | |

*Error types:

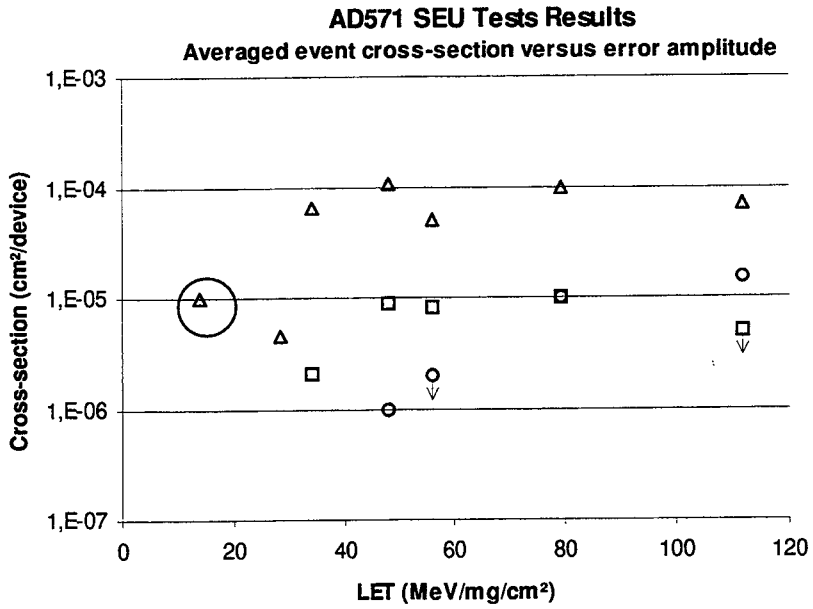
1 4 pts (39 mV) < Error amplitude < 32 pts (312 mV)
2 32 pts (312 mV) < Error amplitude < 256 pts (2,5 V)
3 256 pts (2,5 V) < Error amplitude
4 Not used

**Figure 4 - AD571 SEU Test Results**

**a ) Total SEU error number per irradiated sample**




**b ) Average SEU error number per transient amplitude range**




△ 4pts (39 mV) < Amplitude < 32 pts (312 mV)
□ 32 pts (312 mV) < Amplitude < 256 pts (2,5 V)
○ 256 pts (2,5 V) < Amplitude

## 10. CONCLUSION

SEU test have been conducted on AD571 10-Bit A/D Converter from Analog Devices, using the heavy ions available at the University of Louvain facility.

SEU susceptibility for the test configuration described in §7.2, was obtained through the cross section versus LET curve for the three different transient amplitude ranges (small, medium and large, respectively 4 pts-32 pts, 32 pts - 256 pts, and >256 pts).

With these results upset predictions on XMM orbit, can be performed for each error amplitude range

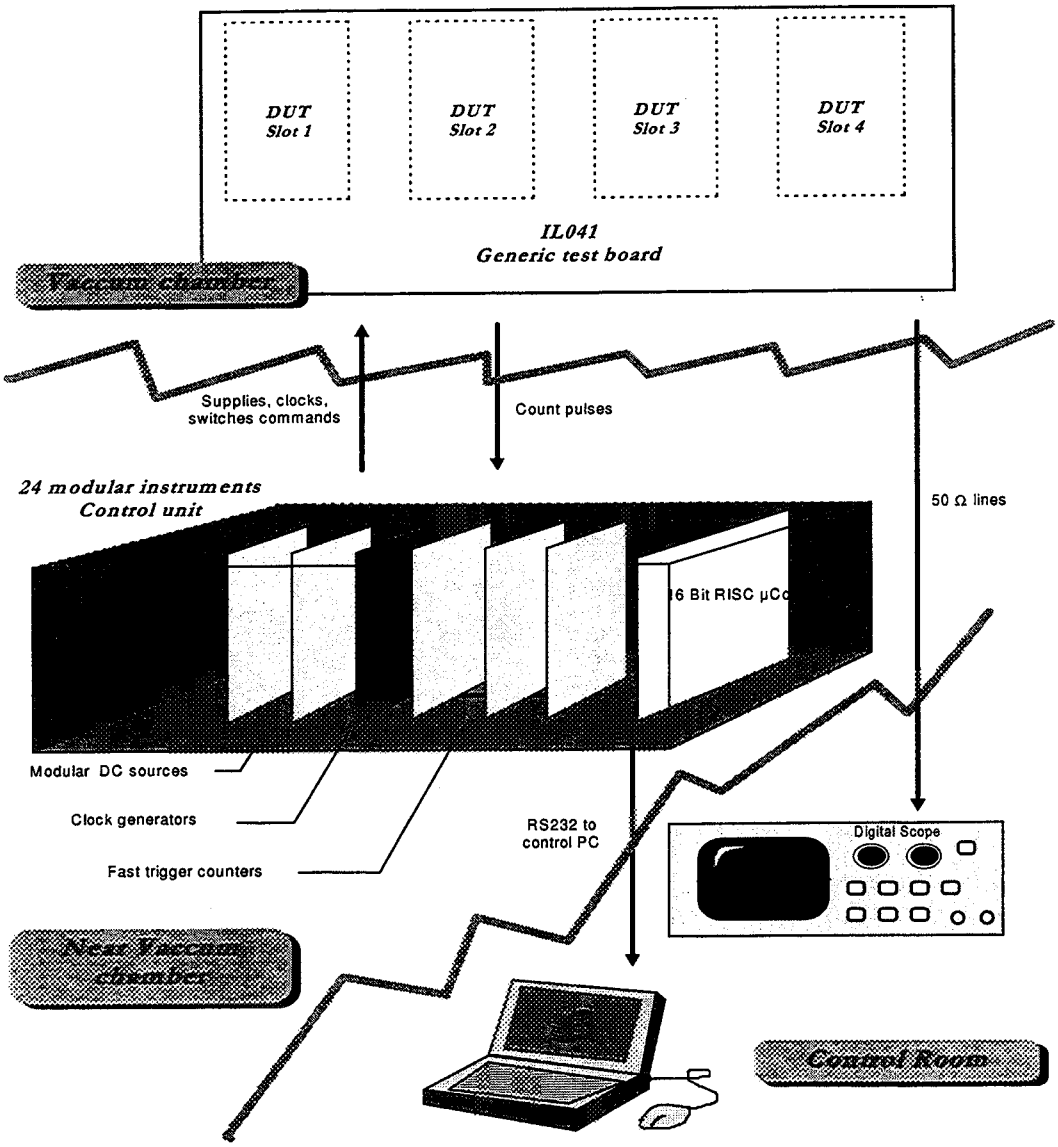
Lastly, no SEL has been detected during the different runs performed on the two samples.

## Appendix 1

### Test set-up

The complete test equipment is constituted of:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 4 devices
- A digital oscilloscope to store analog upset waveform.

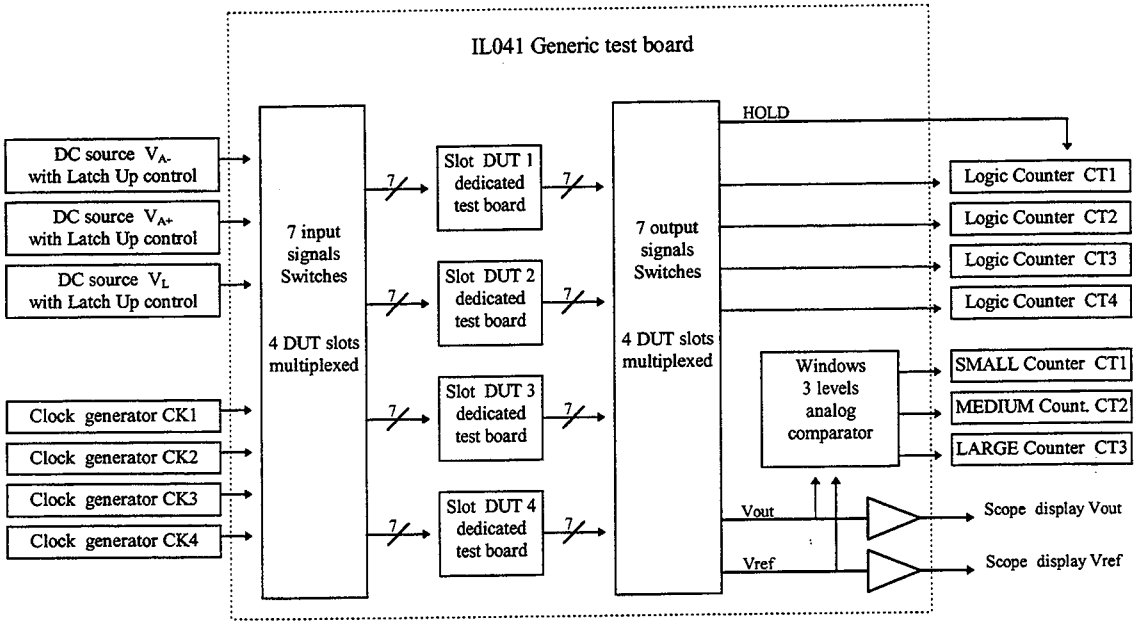


## Mother board description ( ref. IL041)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each DUT board slot , the following signals can be considered:

- seven inputs signals
  - 3 programmable power supplies
  - 4 programmable clocks
- seven output signals
  - 4 logic counting signals
  - 2 analog signals : DUT output and Ref . output
  - 1 HOLD signal which can inhibit temporarily the counters.

- Each device needs a dedicated plug-in test board compatible with IL041 mother board.
- IL041 board has been designed to comply with Louvain Test facilities .
- The number of slots is limited to four
  Operation is multiplexed and only one slot is powered at one time.




## DUT Test board description

The device under test is mounted on a specific board support which is plugged onto the motherboard.
Mechanical outlines : 141 mm x 50 mm , wrapping or printed circuit board with two 20 pins connectors.
According to test set up and device operating conditions, the test board can accept the mounting of :

- The DUT package with beam positioning constraints (unique for Louvain facilities)
- The golden chip
- The pattern generator
- any interface circuit such as buffer, latches ...
- a standalone micro controller if necessary...

Note : beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

## Three Windows analog comparator

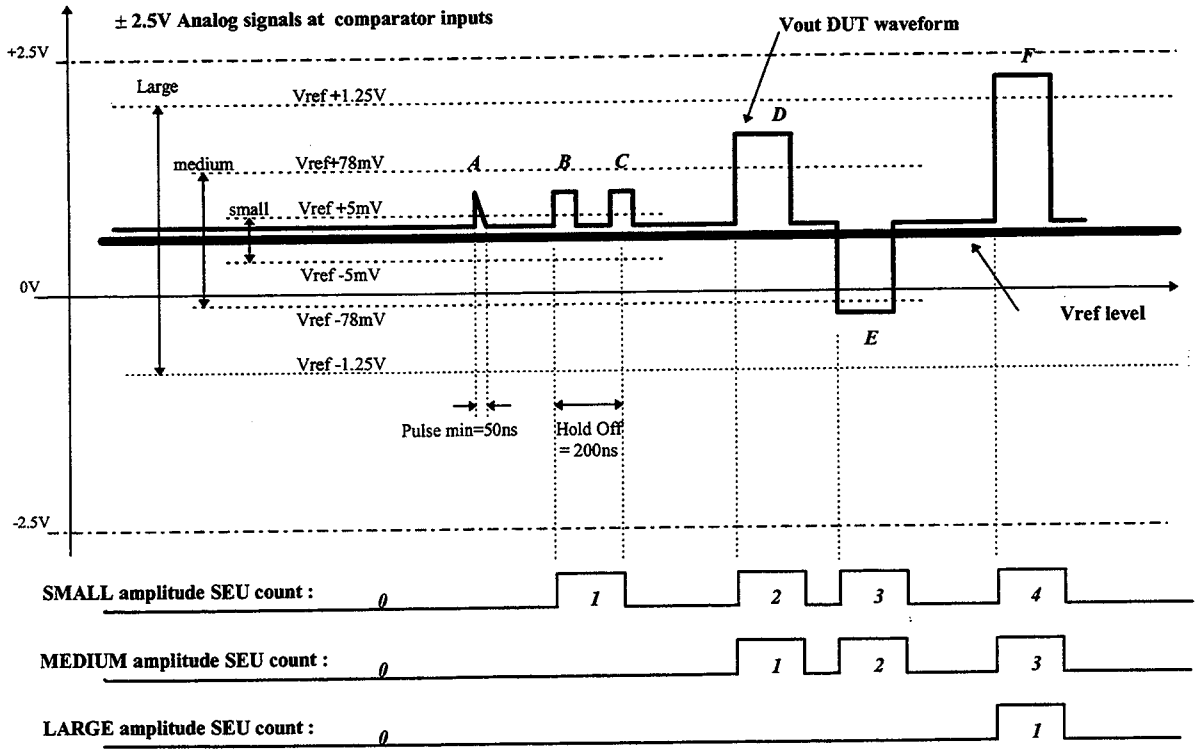
**Applications :**
Single analog output devices, including DAC, can be monitored with a generic 3 windows fast comparator associated to 3 counter modules .

**Test principle :**
Each window uses pre-defined levels centered around the awaited working point :

- The SMALL window uses the lowest levels compatible with the hardware limitation ( offset, noise ...)
- The LARGE window is for counting major DUT output perturbations : Vout max /2 or DAC MSB...
- The MEDIUM window has been defined using a geometric progression between SMALL and LARGE

To illustrate how it works, the here after figure gives an example of timing diagram :
Both DUT and Ref. working point can vary within the ±2.5V allowed input range (+1V in the example).
6 transient pulses can be seen on the DUT Vout record :

- Pulse A will not be counted as its width is shorter than Pulse min parameter
- Pulse B and C : Only B will be counted as the time between B and C is less than the Hold Off parameter (this prevents of multiple counting in case of large degraded transient)
- Pulse D and E : Both pulses will be counted as the comparator works whatever polarity.
- Pulse F is an example of large event . It can be noticed that a large event is also counted as a medium and a small as well.




**Interest :**
The use of this principle allows for straightforward analysis of the test data, at run time. So, it is easy to react and adjust the beam conditions to obtain proper data. When preparing the report, it also shortens the subsequent run recorded data analysis exercise.
Lastly, using 3 different levels at a time, reduces the number of runs needed for the device characterization

**ADC converters :**
The here above method can also be transposed to the test of ADCs. In that case, the 3 windows analog comparator is replaced by a simple standalone micro controller witch execute the same windowing operation by soft.

**Working point variation and HOLD function :**
This window comparison is compatible with low frequency working point variation ( few Hertz ) . This is particularly useful with ADC and DAC devices : Saw tooth input pattern can be used to test the device with a uniform digital code distribution. In that case, the input saw tooth is rather a stair case signal. HOLD function allows to inhibit comparison and counting each time the pattern changes.

## Test signals definition

**Supplies**

| signal | module | $U_{Reg}$ | $I_{max}$ | $I_{LU}$ | $I_{nom}$ | $I_{\Delta}$ | function |
|---|---|---|---|---|---|---|---|
| $V_L$ | 8 | | | | | | |
| $V_{A+}$ | 9 | | | | | | |
| $V_{A-}$ | 10 | | | | | | |

- **signals** $V_L$ , $V_{A+}$ & $V_{A-}$ are 3 DC sources with constant voltage / current characteristic, software monitoring, Latch Up threshold detection, delayed start & stop triggering
- **module :** Slot position used by hardware & software control system
- $U_{Reg}$ **:** DC source set up for constant voltage operation
- $I_{max}$**:** DC source set up for constant current operation, useful on large DUT latch up or failure
- $I_{LU}$**:** software Latch Up detection current threshold
- $I_{nom}$**:** nominal current when DUT operates properly
- $I_{\Delta}$**:** minimum current measurement change required for event memory write
- **function:** DC source assignment ( DUT or test board auxiliary device)

**Latch Up timing**

| $T_{wait}$ | $T_{off}$ | $T_{set\ up}$ x 3 | $T_{LU}$ |
|---|---|---|---|
| | | | |

- $T_{wait}$ Sustaining Latch Up time ( delay between detection and DC sources shut down)
- $T_{off}$ Off state duration
- $T_{set\ up}$ **x 3** Restart triggering Delay between the different internal sequential levels
- $T_{LU}$ Total latch Up sequence duration

**clocks & commands**

| signal | module | period | pulse width | function |
|---|---|---|---|---|
| CK1 | 4 | | | |
| CK2 | 4 | | | |
| CK3 | 5 | | | |
| CK4 | 6 | | | |
| HOLD | | | | |

- **CK 1, CK2, CK3, CK 4** are 4 dedicated programmable logic signals (static or dynamic) which can be used for DUT Clock, DUT mode selection , Upset simulation ...
- **HOLD** is a dedicated signal generated by the test board circuitry ; HOLD = 1 disable all the event counters when the analog comparison is not available, during DUT level transitions ...

**Event counters**

| signal | module | Pulse min. | Hold Off | function |
|---|---|---|---|---|
| CT1 | 16 | | | SMALL or Logic event 1 |
| CT2 | 18 | | | MEDIUM or Logic event 2 |
| CT3 | 20 | | | LARGE or Logic event 3 |
| CT4 | 22 | | | Logic event 4 |

- signals CT1 ... CT4 are 4 count input channels , either for straightforward logic event acquisition or for window analog comparator acquisition
- Pulse min : minimum pulse width required , according to overall system bandwidth
- Hold Off: minimum delay imposed between the detection of two consecutive events

**oscilloscope monitoring @50Ω**

| signal | Bandwidth | function | gain | nominal level |
|---|---|---|---|---|
| Vref | | | | |
| Vout | | | | |

- **signals Vref** and **Vout** are the 2 analog input channels for both analog comparator and digital scope
- **Bandwidth:** overall channel bandwidth
- **gain:** channel gain between actual DUT level and scope displayed level

**Note :** The oscilloscope can be triggered by one of the event counter input signal CT1 ... CT4

**Check test**

| | |
|---|---|
| **nominal state check** | |
| **upset detection check** | |

To check that the device is operating properly, this test can be perform at any time under software control. The use of CK4 signal allows for two different modes :

- **nominal state check** : CK4 disable , absence of any event
- **upset detection check** : CK4 enable, presence of calibrated simulated event periodically introduced at a slow rate

**Test board**

| | | | |
|---|---|---|---|
| **Ref. : IL043-xx** | **Dim. :** | **slot :** | |

- Each set up is dedicated to a specific slot number, in order to ensure that each device is tested with the proper set up conditions.