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A STUDY OF DIGITAL-TO-ANALOG CONVERTERS FOR SPACE APPLICATIONS

Young Graduate Trainee Report

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Foreword

The study described in this report was performed in the Young Graduate Trainee scheme in ESTEC during march -91 to february -92 within the Radiation Effects and Analysis Techniques Unit.

The topic for the study was derived from fruitful discussions with Scientific Institutes and their contractors, designing and building scientific instruments for ESA space projects as well as several semiconductor manufacturers.

It is hoped that this report will become useful for both parts selection purposes as well as for semiconductor manufacturers who assessing the potential of the space market.

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Abstract

A brief market survey of commercially available low-power Digital-to-Analog Converters is presented. Several interesting products were selected to be subjected to radiation testing. Total dose tests were performed using the ESTEC ^{60}Co-source; depending on device performance devices were irradiated to total doses of up to 100 krad.
Test strategies to verify the static and dynamic performance after irradiation were developed; test results are discussed and interpretations as to the possible mechanisms that lead to degradation and finally to device failure are given.
It was found that parts from different manufacturers show widely varying radiation tolerances. In most parts threshold voltage shifts of the n-MOSFETs were found (charge trapping in the gate oxide); increased leakage due to poor field oxide quality was another common failure mechanism. Best results with virtually no degradation in performance up to a total dose of 70 krad was found for the Sipex 7541A and the Sipex 7584 current output DACs.

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1. Introduction

As DACs become more and more important in many electronic applications, there are a lot of different companies producing them and competing for their share of the market.
High-precision, high-resolution DACs (16 - 20 bits) for audio purposes (CD-players) and ultra-high speed DACs (settling times below 25ns) for video applications have been the latest big successes for that kind of device.
But with the variety and flexibility of available DACs increasing, the number of possible applications is steadily on the rise. DACs are used e.g. in the design of microprocessor-controlled filters, programmable gain or attenuator circuits, voice synthesizers, process control actuators and arbitrary signal generators.
Due to rapid progress in applying power-efficient CMOS technology for DACs and the successful combination of bipolar and CMOS elements on a monolithic chip, further use of these devices for an increasing number of space applications seems to become more and more interesting as well.

The scope of this work was to give a brief market survey of available D/A Converters and then apply space-related selection rules to choose a number of devices that were subsequently subjected to total dose radiation testing using the ESTEC ^{60}Co radiation source.

It is also intended to stress the importance of radiation effects when electronic components are used for space applications. Sometimes considerations of these effects are implemented into a project design at a rather late stage. Keeping in mind that space is a very hostile environment ([1],[2]) and defining the mission radiation profile as early as possible (with appropriate consequences for device selection and/or shielding requirements) may save a lot of unnecessary work.

2. Basic working principles of Digital-to-Analog Converters

The general purpose of a DAC is to convert a quantity specified as a binary number to a current or voltage proportional to the value of this number. There are several popular methods:

1) Connecting scaled resistors to the summing junction of an OP-AMP. Disadvantages: Requires a number of high precision resistors of widely different values, which is almost impossible to achieve for a larger number of bits (for a 12 bit DAC one needs a range of resistor values having a ratio of 2000:1)

2) Scaled current sources: The currents can be generated by an array of transistor current sources with scaled emitter resistors (see figure 2.1)
In cases where a current output is sufficient this approach has the advangtage of being very fast; bipolar circuits are rather power-hungry, though.

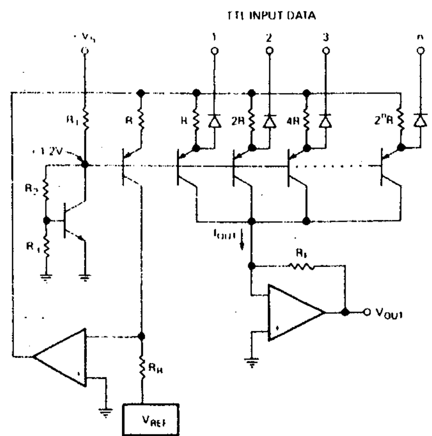


Figure 2.1: Weighted current source D/A Converter

3) R-2R resistor ladder network: Working very similar to the method of scaled current sources, it is the most elegant, most widely used technique. The working principle can be seen in figure 2.2.

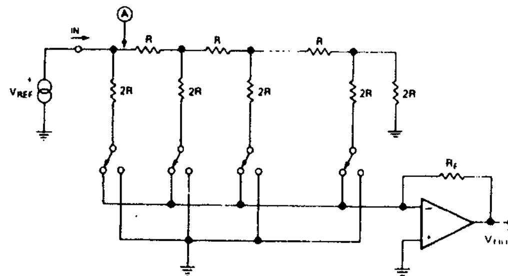


Figure 2.2: R-2R ladder D/A Converter. Very often the OP-AMP has to be added externally; the feedback resistor is always included in a commercially available DAC to guarantee identical temperature coefficients of all resistors.

Only two different resistor values are needed, from which the R-2R network generates binary scaled currents if the network is connected to a voltage reference. These currents are constantely flowing and they are switched either to ground or the "virtual ground" point of an OP-AMP by CMOS switches at the end of each leg of the resistor ladder (12 legs for a 12-bit DAC). The use of CMOS switches means that this method is very power-efficient. A possible configuration for the switches is shown in figure 2.3:

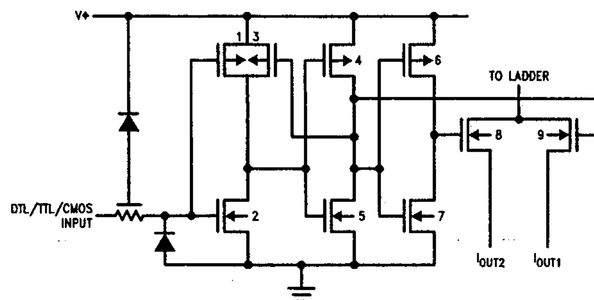


Figure 2.3: CMOS current switches with input voltage level shifters

It allows for DTL/TTL/CMOS digital input levels by using internal voltage level shifters; n-MOS transistors 8 and 9 are connected to the end of a leg of the resistor ladder in such a way that one of them is always in its conducting, the other one in its nonconducting state. The designer has to take care to include the "ON"-resistance of the n-MOS transistors in the total resistance value of the respective R-2R ladder leg in order to preserve accuracy.

In fact, the overwhelming majority of commercially available DACs uses the concept of the R-2R ladder. The most simple DACs like the 7541 type consist of an R-2R ladder network and unbuffered digital inputs driving the CMOS switches at the end of the ladder legs. A precision voltage reference has to be added externally, just as the OP-AMP converting the output current into a voltage (two OP-AMPs are necessary for bipolar voltage output). What is included in even the most simple current output DACs is an internal feedback resistor to be used with the OP-AMP. This is very important because it is matching the resistors of the R-2R ladder in value and in temperature coefficient; the use of external trimpots to adjust gain and offset therefore usually increase the gain temperature coefficient and should be avoided if possible.
Current output DACs normally have a settling time below 2us; for video applications settling times of about 20ns are achieved. If, however, the current has to be converted to a voltage the settling time will increase considerably even if a fast OP-AMP is used.

3. Market survey

3.1 General

The market for DACs with more than 12 bit resolution is clearly dominated by the major US semiconductor manufacturers (Analog Devices, Burr Brown, Harris, Siliconix, Sipex, Maxim) which all claim to do their own fabrication. European manufacturers are almost nonexistent (some Philips and SGS Thomson parts available) and Japanese companies also play only a minor role.
The situation is different for DACs with less than 12 bits and Video DACs which have very short settling times and resolutions up to 8 bits (some parts having a resolution of 10 and even 12 bits were introduced recently): here Japanese (Fujitsu, Sony, NEC, Hitachi) and other European companies (notably GEC Plessey) can offer a broad range of products as well [D1]

3.2 Recent trends in DAC products

Bipolar devices, which have been the early DACs, are more and more being replaced by CMOS DACs, i.e. the current switches implemented in the most popular designs are CMOS switches. One obvious advantage is lower power consumption and high speed; as the physical dimensions of CMOS transistors are becoming smaller and smaller, it is also possible to include an ever increasing number of logic and buffer elements on one chip, increasing the flexibility and making it easy to create interfaces to other logic chips. A major effort of all the companies involved on the market has been to make DACs compatible to a wide range of microprocessors and Digital-Signal-Processing (DSP) devices. This required to incorporate various types of latches in different architectures (12-bit single, 8+4-bit, 4+4+4-bit) and the necessary control logic into their design.
Finally some companies developed production processes which made it possible to combine analog and digital circuitry on the same chip. In this way the OP-AMPs used to convert a

current to a voltage can be included in the device. Some companies, however, switched to hybrid devices to achieve this.
Some examples of the ever increasing complexity of devices will be given in the chapters dealing with the individual manufacturers.
Another goal that is pursued by most manufacturers is the trend to reduce the power supply voltage from +15V (or +/-15V for bipolar output devices) to +5V (+/-5V). In fact, most of the devices that have only recently been introduced to the market operate on 5V supplies. This might have some influence on radiation tolerance as lower voltages allow for the use of thinner gate oxides to be used.

Collecting information as to the exact nature of the manufacturing process, planned changes of processes now in use etc. turned out to be a rather tedious task as many companies are rather uncooperative when asked about these details. In a complementary study of Analog-to-Digital converters (ADCs), another author nevertheless made great efforts to extract exactly that kind of information from major companies. As his questions were mostly directed at successive-approximation ADCs, which have a built-in DAC as one of their major building blocks, the information he got is most likely also the current state of DAC technology. For that kind of information the reader is referred to this report [3].

A final fact to keep in mind is that new devices are being developed in rapid succession these days and appear on the commercial market almost every month. A close observation of these developments is therefore absolutely necessary.

3.3 Brief overview of the product line of major companies

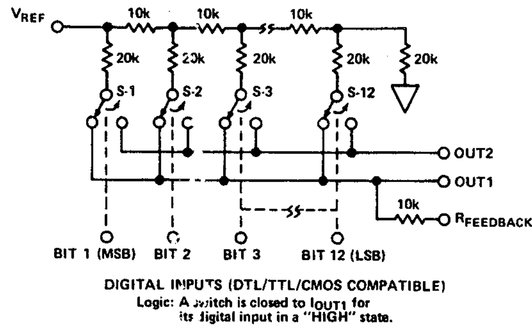
ANALOG DEVICES

This company seems to offer the largest variety of DACs. In fact, in the 1990 databook already 87 different types of devices are offered. They range in resolution from 4 to 18 bits, have settling times from 5ns (4-bit video DAC) to 40us (high-precision 18-bit DAC) with widely varying degrees of functional completeness and interfacing compatibilities.
Analog's so called "LC^{2}MOS process" (Linear Compatible CMOS) allows for the combination of precision bipolar circuits and low-power CMOS logic on the same monolithic chip. As a consequence, more recent products include even a couple of OP-AMPs in addition to already rather complex logic circuits.
To give an impression of what Analog Devices can offer, the block diagrams of a few products are presented.

AD7541A

This is an example of the simplest form of a current output DAC. It is also an industry standard, with many other manufacturers second-sourcing Analog Devices on this device.
As can be seen in the circuit schematics below, it only consists of an R-2R resistor ladder and CMOS current steering switches with level shifters so that the inputs are DTL/TTL/CMOS compatible. No input or output buffering is available, and a precision voltage reference and an OP-AMP (for current-voltage conversion) have to be provided externally. The OP-AMP feedback resistor is included, however.
This configuration will be referred to as a "basic DAC".

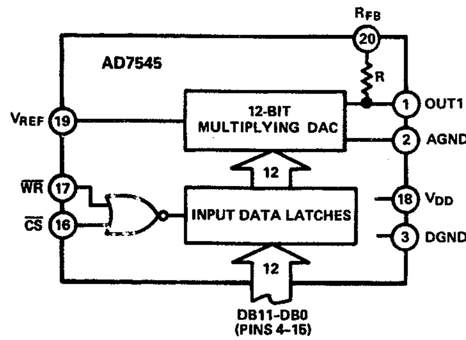
AD7541A FUNCTIONAL BLOCK DIAGRAM



AD7545

A "basic DAC" with buffered digital inputs and the accompanying, simple control logic.

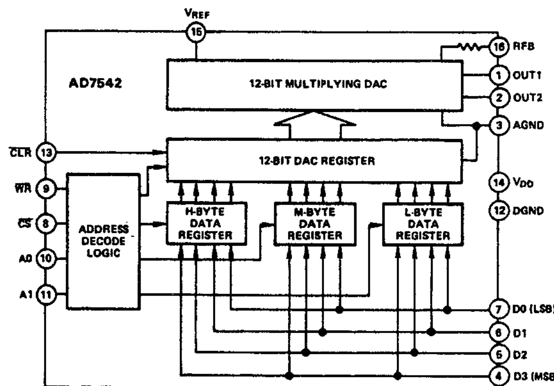
AD7545 FUNCTIONAL BLOCK DIAGRAM



AD7542

A "basic DAC" having two stages of input buffers to allow for easy microprocessor interfacing.

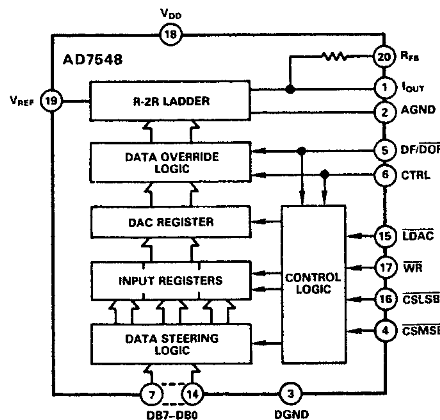
AD7542 FUNCTIONAL BLOCK DIAGRAM



AD7548

A "basic DAC" with double-buffered inputs and the necessary control logic. It also includes a voltage reference and an output OP-AMP (voltage output).

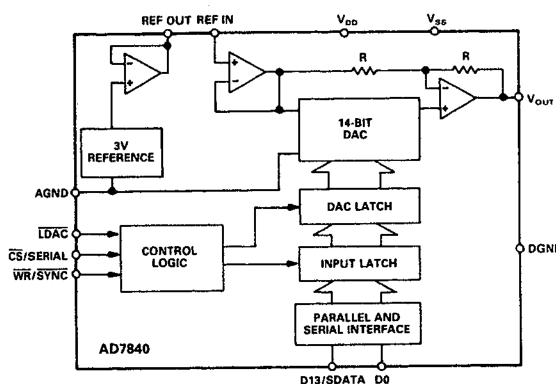
AD7548 FUNCTIONAL BLOCK DIAGRAM



AD7840 (14-bit DAC)

It provides double-buffered inputs wherein data can be loaded serial or parallel, determined by the setting of the control logic. Also included are a buffered 3V-reference and two output OP-AMPs for bipolar output when using +5V and -5V supplies (also operates from a single +5V supply in unipolar mode)

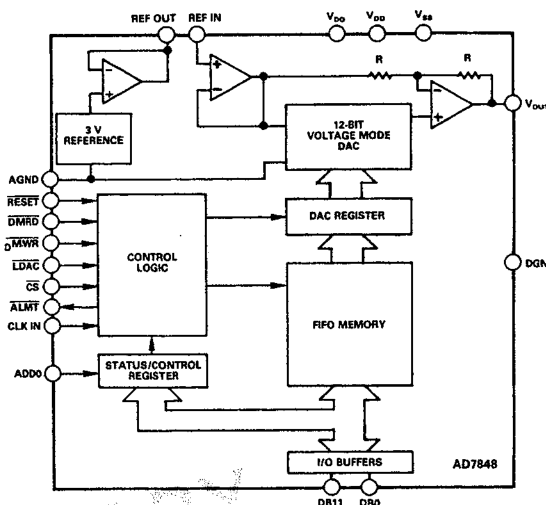
AD7840 FUNCTIONAL BLOCK DIAGRAM



AD7848

basically like the AS7840, but also including a FIFO (first-in, first-out) memory for easy interfacing to high-speed Digital Signal Processors.

AD7848 FUNCTIONAL BLOCK DIAGRAM



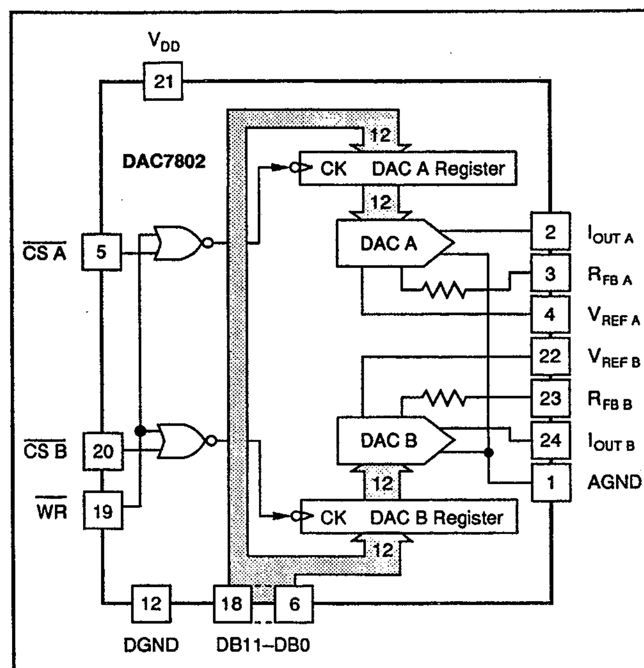
BURR BROWN

Another important manufacturer, although the range of available products is smaller. The main strength seems to lie in Audio, Communication and DSP DACs. Again the trend to include precision analog circuitry monolithically on one chip can be seen: quite recently a number of rather fast voltage output DACs appeared on the market, including voltage reference, latches and OP-AMPs (e.g. DAC813). Unfortunately their power dissipation is rather high.
Recent developments are devices with a single +5V power supply sometimes including more than one DAC on a single chip. A good example for the latter is the

DAC7802

It features two basic DACs whose individual latches share one set of input pins. The necessary write control logic enables the user to address the latches either individually or simultaneously.

BLOCK DIAGRAM



Burr Brown is also second-sourcing the AD7541A, which was chosen as a test object for irradiation testing.

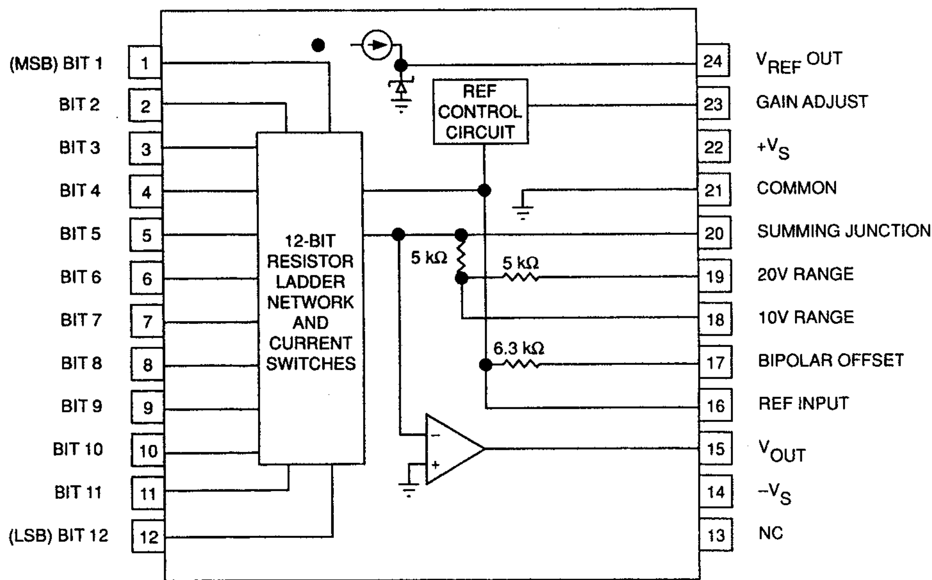
Harris

It seems as if Harris does not play a major role in the market for DAC products. They offer a rather limited choice of DACs which are older types that have been on the market for some time. No recent developments have been released to the author's knowledge.
Harris, however, is an important manufacturer of rad-hard analog and digital devices and therefore is of potential interest. Their version of the AD7541 was included in the tests.

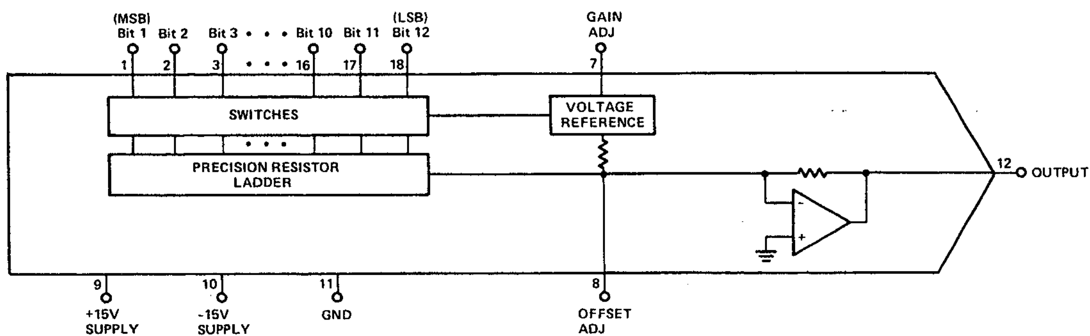
Sipex

Although Sipex is also second-sourcing the popular 7541A monolithic current-output DAC, it pursues a rather independent policy with a product range that is rather unique. Their focus is mainly on complete, high-end products, combining many building blocks into one chip, offering resolution up to 18 bits. Most of their DACs feature voltage output.
However, instead of using monolithic designs, a large part of the available devices is made up of hybrids (note that Sipex acquired Hybrid Systems, another manufacturer specialising in hybrid designs, a few years ago). Therefore their power consumption is rather high (approx. 300mW for a simple voltage output DAC). Their recent new developments seem to indicate that also Sipex recognizes the trend towards monolithic devices: a good example is the new SP DAC87, a complete monolithic DAC with voltage reference and OP-AMP, but no input latches.

SP DAC87



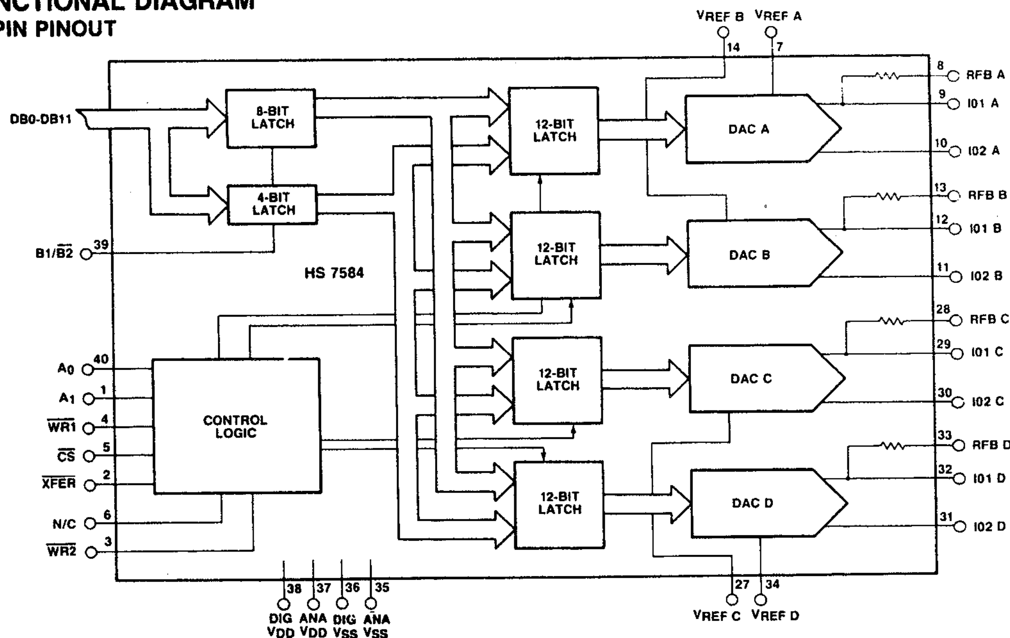
Despite its slow settling time of 50us for a full scale step, the Sipex DAC356-12 was chosen to be tested because the manufacturer claimed that its power consumption was only 70mW. (for all test devices it turned out to be about twice as much, however).
It is a hybrid voltage output DAC including Voltage reference and an OP-AMP operating on +/-15V supplies.



HS7584

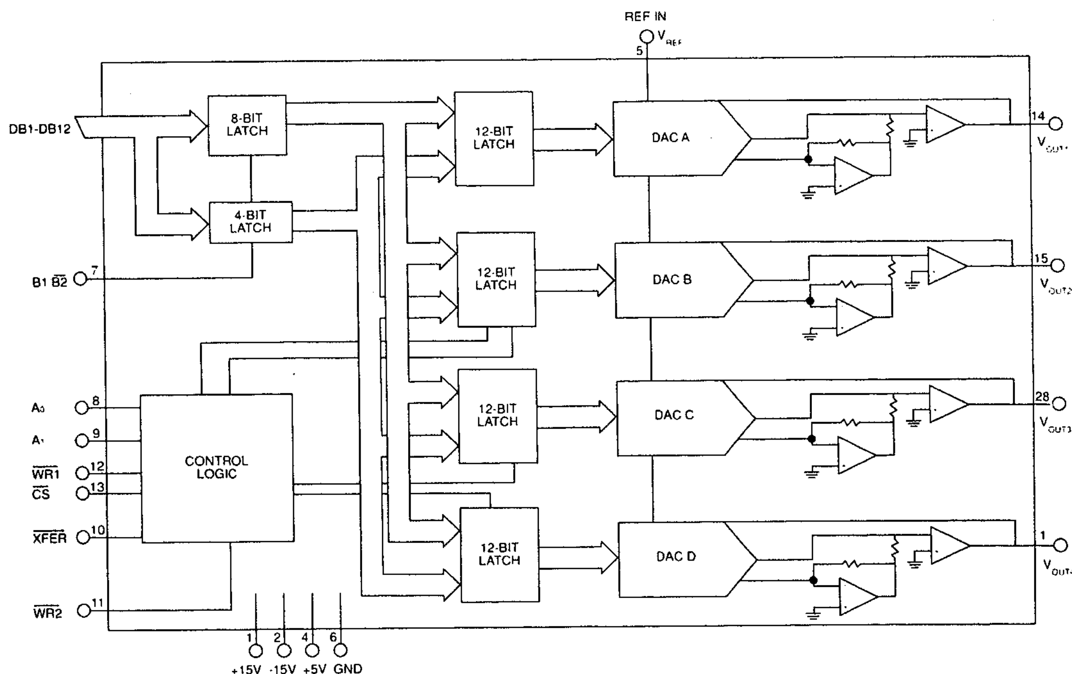
Another test candidate was the monolithic HS7584 Quad current output DAC. It works on a single +5V power supply, needs an external voltage reference, but includes two stages of input latches and dissipates a mere 25mW, about 7mW per DAC if digital levels are 0.8V and 2.4V, respectively! (even less for digital input voltages of 0V and V_{dd}).

FUNCTIONAL DIAGRAM
40-PIN PINOUT



SP9344

FUNCTIONAL DIAGRAM



This voltage-output Quad-DAC is an extension of the HS7584 where OP-AMPs have been added to enable voltage output. It was still in the preparatory phase and about to be released,

but according to preliminary information it works on +/-15V and +5V supplies which makes it more complicated to operate and consumes about 600mW, i.e. 150mW per individual DAC, excluding external voltage reference.
Although it might be useful for applications that require more DACs and where board space is limited, the need for 3 different supply voltages is a drawback. It is supposed that it also will be a hybrid device.

Maxim

Maxim seems to compete mostly in the range of low-end products. They are mostly second-sourcing Analog Devices products (like the popular and simple 75XX series of DACs) with few recent developments of their own.

PMI

This company has been acquired by Analog Devices, but it seem as if they keep their own fabrication lines and only the marketing has been taken over. Its main product line in the 12-bit segment are CMOS current output DACs.
It is also noted here that a product of possible interest was announced in the Sept. 1989 databook: a GaAs-based 12-bit voltage output DAC with 3ns settling time. The power dissipation of 450mW is extremely low for a product of that speed. Due to the material used it might also show considerable radiation tolerance. This was preliminary data, however, and as the power requirements were too high for the present tests, no information as to the present status of this product has been gathered.
The PMI 7541A was subjected to radiation testing.

4. Choice of devices

To limit the number of devices to be tested, the DACs had to meet certain criteria to be of potential interest in space applications. Basically the search was limited to converters giving 12-bit resolution as most DACs currently used in space are 8-bit devices. Apart from that, the most stringent restriction was POWER CONSUMPTION: being of great importance in space applications, only low-power devices were sought, the maximum being in the order of 150 mW. This meant that virtually all high-speed devices were excluded as these usually require some 500 mW to a few watts to achieve settling times below 100ns for current output DACs (e.g. Analog Devices AD568 or HDM-1210) and below 3us for voltage output DACs (e.g. Analog Devices AD767, Sipex HS3860 or DAC338). Most bipolar devices have a rather high power consumption,too; as they have been on the market for quite some time, even radiation test reports for some of them are already available (for example the AD565A had to be radiation tested for use in the ISO project [4]). Sipex as a manufacturer performed some irradiation tests under a radiation hardening program currently under way. For some of their DACs data on total dose and neutron testing is available.

Table 4.1: Radiation data available from Sipex on some of their products. Data on voltage references was also included as this is a vital external part for many multiplying DACs.
The numbers give the upper radiation limit where the devices were still within specification limits.

Type	Remark	total dose [krad]	Neutrons [n/cm^2]
HS 2700 family voltage reference	bipolar	3000	5.10^{12}
HS 3860 12 bit DAC	bipolar	300	3.10^{12}
DAC 370 18 bit D/A	CMOS	5	n.a.

Further selection requirements were SPEED (settling time should be no more than 10us for voltage output DACs and no more than 3us for current output DACs) and the BINARY DATA CODING (meaning that the digital input code had to be either "offset binary" or "2s complement"). Finally, care was taken to select only devices requiring "standard" input voltages, i.e. either +/-15V, +15V or +5V.

Although these restrictions excluded a large percentage of devices from being selected, quite a lot of commercially available DACs fulfilling the above-mentioned requirements was still left. At this stage it became clear, however, that only CMOS devices could meet the requested power consumption limits. A closer examination reveales that most manufacturers produce a variety of DACs which are very similar to each other with regard to their "central" part, while the "periphery" was slightly different to meet the various demands of the customers.
A good example is the 7521/7531/7541/7541A/7542/7543/7545 family of CMOS-DACs where the same core building blocks (resistor ladder and CMOS switches) can be seen on each chip, while a varying amount of additional features is included in different chips (different kinds of latches in different arrangements, two stages of latches, control circuitry, provisions for serial or parallel data input). This principle (identical "core" DAC, different logic interfaces and peripheries) can be verified for example by comparing the physical chip topographies for different DACs as they are shown in the MAXIM 1989 databook [D2].

Another example is the Burr Brown DAC7800/7801/7802 series, wherein the digital interface is the only difference between the devices.

As the investigation was also intended to find the weak points and to identify with a high degree of certainty the parts which degrade under irradiation, the "simplest" version of these DACs (i.e. having the fewest functional blocks) was usually chosen. Obviously it is much more difficult to determine the location of failure and the failure mechanism in a highly complex device (comprising for example one or two sets of latches with the according control logic, an internal voltage reference and internal OP-AMP in addition to the central resistor ladder and CMOS switches) than in a rather simple one. While for the first group only the observation of degradation of the performance is possible (with many possible reasons for it), a much more detailed analysis can be performed for the second group by comparison of various input and output parameters at different stages of the irradiation program.

Therefore, in general "simple" devices were chosen to be tested. On the other hand, it is clear that for applications a high degree of functional integration is desirable. But as requirements for different missions might differ considerably (microprocessor interface compatibility yes/no, serial/parallel data input, settling time crucial yes/no...) it is sure that further testing has to be done anyway which might build on the results gained in the course of this evaluation.
In some cases it might even be worth to use a rather primitive current output DAC because this provides some additional flexibility: the OP-AMPs necessary to convert the output current to a voltage can be chosen to be rather slow, low-power devices or fast types with increased power consumption, tailored to the application's needs. A reference voltage, needed for most of the simple DACs, might already be necessary for some other purpose and be available on the board anyway.

Final choice of test devices

In the end, after a first and second pre-selection, the final candidates were chosen. A natural choice seemed to be to include the AD7541A (and compatible):

* it is a simple device (resistor ladder and current switches
* it seems to be form a "industry standard" and therefore is produced by a lot of manufacturers, which allows a direct comparison of the quality of the manufacturing process used by them.

The other test candidates were not so obviously found; finally a choice had to be made among a number of different devices which according to the data sheets had about the same performances.
It was therefore decided to vary the power supply voltages, including devices working from a single +5V supply which seem to become more and more popular among manufacturers as well as "standard" DACs working on +15V. The trend to include more than one DAC in one chip was also taken into respect, although it is then necessary to buffer the inputs and provide control circuitry.
Finally a DAC with built-in OP-AMP and a complete bipolar voltage output DAC were also included.
It should be noted that all these DACs used the principle of the R-2R resistor ladder in combination with current switches.

List of test devices:

1) Analog Devices 7541A
2) Burr Brown 7541A
3) Harris 7541
4) PMI 7541A
5) Sipex 7541A

These devices were multiplying CMOS current output Digital-to-Analog converters requiring an external precision voltage reference and one (for bipolar output: two) external OP-AMPS.

6) Burr Brown 7802

This was a dual multiplying CMOS current output DAC working on a single +5V power supply with buffered inputs.

7) Sipex 7584

A CMOS multiplying current output device including 4 DACs in a single package. Supply voltage was +5V, and power consumption was claimed to be a mere 5mW.

8) Analog Devices 7845

A multiplying CMOS DAC, including an OP-AMP monolithically integrated on the chip and produced with Analog Devices' LC^2MOS process. Power requirements were some 150mW typ., 200mW max., though. Latches were also included, they could be operated in a "transparent" mode.

9) Sipex DAC356

This was the only complete voltage output device, operating from +15V and -15V power supplies, including a voltage reference, but without latches. According to the data sheet its settling time was slower than required but it was included as it was supposed to dissipate only 70mW of power; however, it was found that all the available devices consumed more than 150mW! By opening a device it turned out that it was not monolithic, but a hybrid device.

5. Test setup and strategy

To convert the current output of DACs to a voltage output, a circuit as shown schematically in Fig. 5.1 was used. This circuit theoretically produces an analog output voltage of -10V for a digital input code of 00..00 and of +9.995V (=10V - 1 LSB) for an input of 11..11. The resolution of 12 bits therefore resulted in a voltage resolution of 4.88mV.
The OP-AMPs used were PMI OP-42 with a pretty high slew rate of 50V/us, which in theory translates into a settling time of approximately 500ns for a 10V step [D3]. However, as indicated in the schematic of the circuitry, a feedback capacitor had to be used to dampen the "ringing" that otherwise would have occurred. This slowed down the settling time a bit; it still did not exceed 1.5us for current output DACs, though.

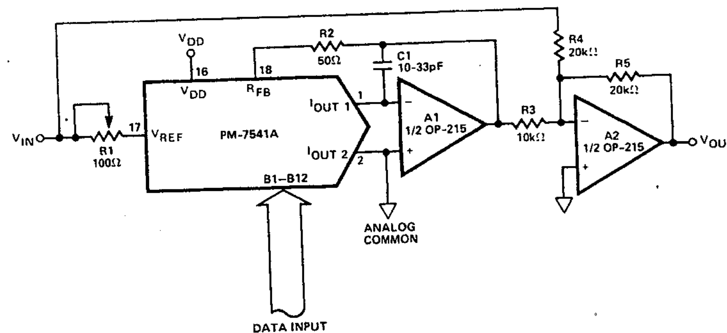


Figure 5.1: External circuitry that was used for current output DACs to convert the current into a voltage. For most DACs that were tested an external voltage reference as indicated in the picture was also necessary. Note the feedback capacitor which is necessary for very fast OP-AMPs to prevent them from oscillating.

In order not to introduce more potential error sources than necessary, no external trimpots for offset and gain adjustments were used (External trimming also causes increased drift with temperature; as all measurements were performed at a constant temperature of 20°C this would not have had any influence).
As the fixed resistors were accurate to 0.1% of their nominal value, the gain error could not be determined more precisely than that. However, as the same circuit was used for all DACs of the same type, the relative change of that parameter in response to radiation could be determined very accurately.

5.1 STATIC TESTING

The main parameters that were determined were

1) **Differential Nonlinearity (DNL):** defined as the largest deviation of any analog voltage output step from the ideal step size of 1 LSB when the digital input code is increased by 1. DACs with DNL greater than +/- 1 LSB may be nonmonotonic.

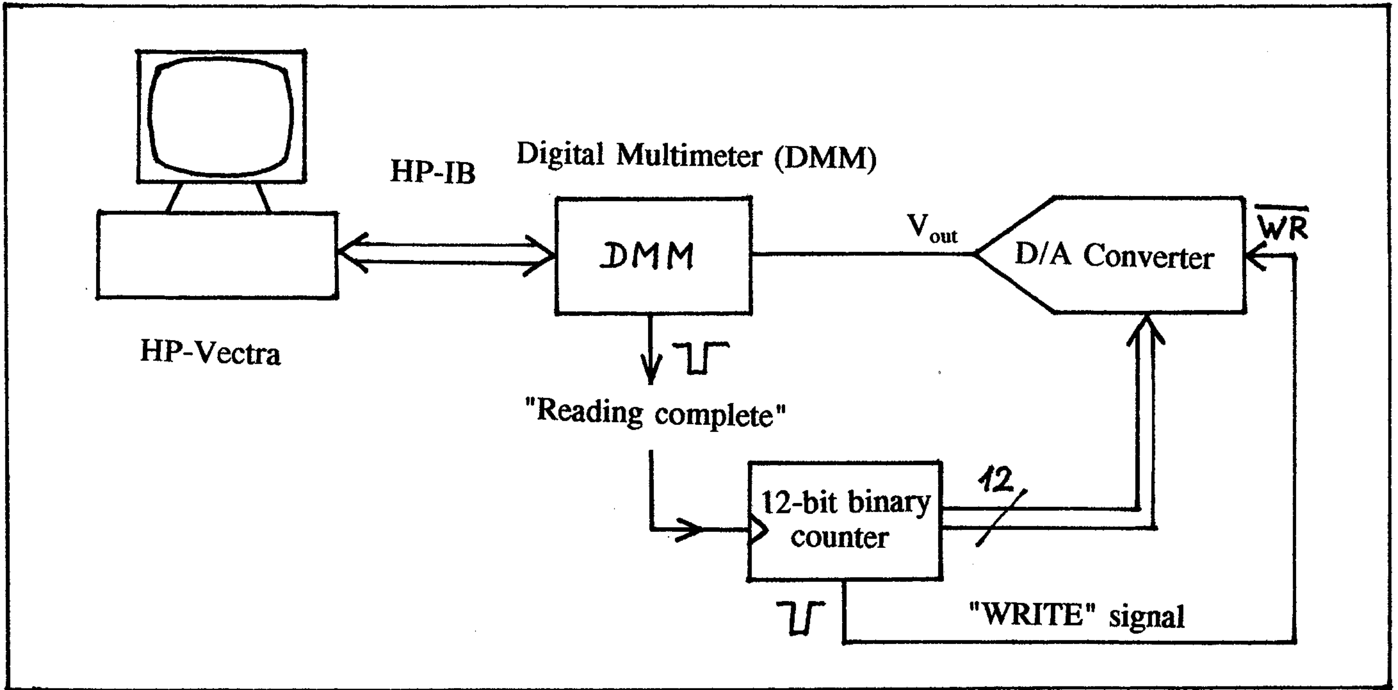
2) **Integral Nonlinearity (INL):** defined as the maximum deviation of the plotted analog output characteristics from a straight line drawn between the end points.

3) **Standard Deviation:** calculated according to its definition, it gives an estimate of the "mean" deviation of the analog output from a straight line drawn between the end points.

4) **Gain Error:** the difference between the actual and the ideal output range when using only the internal feedback resistor. As pointed out above, it could not be determined more accurately than to 0.1%. Comparison between similar devices at various stages of the irradiation process can nevertheless provide interesting results as the relative accuracy is much better than the absolute one.

To measure the value of these parameters, a digital ramp was fed into the device under test (DUT). The ramp was generated by TTL counters (74LS393), which were triggered by a TTL-level input signal. A few microseconds after the digital input code for the DAC was set up, a "WRITE" signal (active low) was available to latch the data word into those DACs whose latches could not be operated in a "transparent" mode. The measurement itself was computer-controlled, using a Keithley model 195 Digital Multimeter (DMM) having a resolution of 0.1mV to measure the voltage output for all 4096 different input codes. The DMM, in turn, provided a "reading complete" TTL output signal that was used to trigger the counter, thereby increasing the binary count by 1.

The HP-Vectra acting as a controller and the DMM were interconnected via their HP-IB interfaces, and a software program written in HP-Basic took care of all timing and data transfer considerations. The measurement data was stored and finally processed by another HP-Basic program which calculated Differtial and Integral Nonlinearity, gain error, standard deviation and the output value of each individual bit of the DUT.



start measurement
start next measurement
HP-IB Trigger
integration time of DMM
"reading complete"
binary data
DATA
DATA
"WRITE" (WR)

Figure 5.2: Schematic measurement set-up used for quasi-static testing D/A converters (top) and the timing diagram for that measurement (bottom). The HP-Vectra acting as controller triggered each measurement via the HP-IB bus; after reading in the result from the DMM on the same way the next measurement was started.

5.2 PARAMETRIC TESTING

The HP 4145 parameter analyzer turned out to be a valuable tool in assessing the radiation damage after an irradiation step in a very quick way. It allowed for the determination of such basic parameters as input current and output leakage current and it was possible to use the test results to interpret what was happening inside the device, i.e. which physical processes lead to degradation of device performance.

The general approach to parametric testing was as follows:

* all necessary power supplies for a device were provided (+5V, +15V or +/-15V)
* for multiplying DACs: a +10V reference voltage was provided
* all digital inputs were shorted and connected to a variable voltage source
* for DACs where input data had to be latched in: a "WRITE" pulse was applied to the appropriate pin(s) after the desired input code had been set up
* for voltage output DACs: the output voltage was measured
* for current output DACs: the output current pins were connected to very sensitive current sensors which could detect currents as low as 1pA

The actual measurement consisted of sweeping the input voltage applied to the digital inputs from 0V to 5V while all the other voltages were kept constant.

Measured parameters were:

1) Positive power supply current
2) Negative power supply current (where applicable)
3) Reference voltage input current (where applicable)
4) Combined input current of all 12 digital inputs
5) Output current (for current output DACs)
6) Output voltage (for voltage output DACs)

All these parameters were determined as a function of digital input voltage. The change of some parameters in response to irradiation made it possible to roughly estimate the radiation sensitivity of a device and to predict the total radiation dose at which the device would probably fail even at a time when the output characteristics were still rather normal.
The measurement was computer-controlled by a simple HP-Basic program, and the measurement data was printed out in tabular form.

5.3 DYNAMIC TESTING

A very powerful tool for dynamic testing seemed to be available with the HP 3653A spectrum analyzer. It offered extremely fast FFT routines, 13-bit resolution and it could operate up to a speed of 256kHz, i.e. taking one measurement every 4us, which seemed just about right to test the performance of the DACs at their upper limit.
Considerable effort was therefore made to design and produce a printed circuit board that did not sacrifice settling speed by keeping the important tracks as short as possible and minimizing the use of sockets by directly soldering most components very close to each other.

The measurement principle was rather simple: the HP 3653A was programmed to output a 12-bit digital sinewave, which was applied to the inputs of the DUTs. Data was updated at a rate of 250kHz and just before a new 12-bit word was set up, the analog output of the DAC (which had settled to its final value by then) was read back into the spectrum analyzer. In this way a corresponding analog output from the DUT was sampled by the spectrum analyzer for every digital data point of the sinewave. The complete time-domain signal was subjected to a Fast Fourier Transform (FFT) to determine the dynamic parameters Total Harmonic Distortion (THD) and Signal to Noise Ratio (SNR). The idea was to detect any possible degradations in dynamic behaviour that might be apparent at an irradiation stage when the quasi static results are still unchanged. In other words, the reason was to see if radiation damage could initially lead to slower device operation while the static accuracy was still within specifications. A schematic drawing of the measurement set-up is shown in figure 5.3:

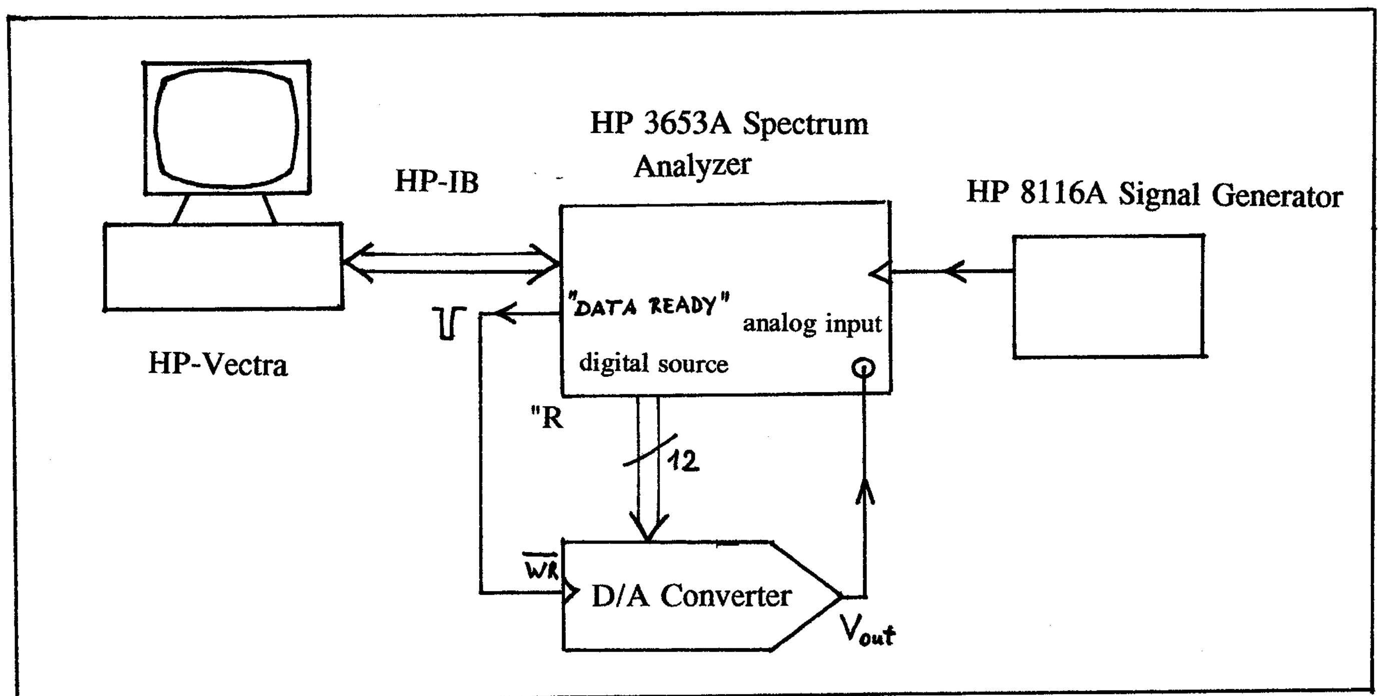


Figure 5.3: Measurement setup used for dynamic testing of D/A converters

The setup of the spectrum analyzer and the measurement sequence was controlled by an HP-Vectra computer running under HP-Basic, which also took care of data output and data storage. The HP8116A programmable signal generator served as the main system clock by supplying a TTL squarewave signal of 250kHz. It determined the digital update rate as well as the analog input sample rate. For some DACs the frequency was lowered to 150kHz (in one case even to 20 kHz) as their specified settling time was greater than 4us.

While above-mentioned data update frequency remained constant for any individual kind of DAC, the frequency of the digital sinewave fed into the DUTs was varied. As increasing that frequency means that successive digital codes have to differ in value more and more, it also means that the analog output steps of a DAC become bigger. Another way to look at this is that a full period of the digital sinewave is made up of less and less points, so they have to be spaced further apart. In this way it should have been possible to detect any influence of the stepheight on the settling time, which is usually the case.

However, it turned out that the spectrum analyzer was not as ideal an instrument for that kind of test as originally thought. The reason for it was rather simple, but nontheless crucial: The analog input path of the spectrum analyzer contained a high-order lowpass filter with a cutoff frequency of 100kHz. This filter prevents aliasing by simply filtering out frequencies that are higher than the spectrum analyzer is supposed to sample. This filter, however, heavily distorted the analog signal from the DACs as their output is a step signal when the digital input code is changed. Theoretically a step signal consists of a superposition of sinewaves whose frequencies are not limited. So even as the DAC output steps are not infinitely steep, they are steep enough to contain frequencies that are much higher than the 100kHz cutoff frequency of the filter. If an analog step is applied, the filter responds by oscillating around the new final value and it takes about 50-100us to settle completely. If the data update rate is 4us, then the next input step arrives when the filter has not yet settled but is still heavily oscillating. As a consequence the measurement is not reliable.
The amplitude of the oscillations is proportional to the stepheight of the input signal, so a lower sinewave frequency should yield rather accurate numerical results (e.g. for a 100Hz sinewave a full period consists of 2500 datapoints; if the amplitude of the analog sinewave is 20V full scale as it was for the DACs used, then the maximum possible stepheight is 25mV. The amplitude of oscillation was observed to be about 10-20% of the stepheight, which means that the measurement error should not exceed 5mV in that case).
Test results obtained at higher frequencies however can only give a rough impression of changes in the DAC when comparing the data at different stages of the radiation tests. Their absolute values are meaningless.
As a complementary measurement and in order to "see" possible changes in the output signal shape a hardcopy of the output signal of the DACs as it appeared on the screen of an LeCroy 9410 digital oscilloscope was also recorded. The basic settings for all DACs were kept the same, so without any changes due to radiation damage no change in the signal shape would be detected. This additional test provided some valuable insight into the switching behaviour of devices coming from different manufacturers.

Definitions:

Total Harmonic Distortion: is the ratio of the rms sum of the harmonics of the DAC output to the fundamental value when the DAC is driven by the digitized representation of a sinewave.

$$THD = 20.\log\frac{V_1}{\sqrt{(V_2^2 + V_3^3 + ...)}}$$

V_1 is the rms amplitude of the fundamental and V_2, V_3... are the rms amplitudes of the individual harmonics.
Usually the only the first 10 harmonics were included in the calculation.

Signal-to-Noise Ratio: is the measured signal to noise at the output of a converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (including harmonics) up to half the sampling frequency. The theoretical SNR for a sinewave is given by:

SNR = (6.02N + 1.76) dB where N is the number of bits.

6. Irradiation facilities and device setup

Irradiations were carried out using the ESTEC ^{60}Co radiation source, which had an activity of about 1.4 kCi or 5.2 10^{13} Bq at the time of this work. The source produced gamma rays with two discrete energies which are very close; their average energy was 1.25MeV.
Doserates were adjusted simply by varying the distance of the samples from the source. The angle of incidence was kept at 90° throughout the tests. All total dose figures that will subsequently be given are in krads(H_2O); to convert to krads(Si) the numbers have to be multiplied by the conversion factor of 0.91. All doses were measured using an Ionex Dosemaster with a 0.6cm^3 Ion probe which was calibrated to +/-0.5%.
During irradiation, all devices were biased to their nominal supply voltages with a +10V reference voltage supplied to those devices that did not have an internal one. The digital inputs were either kept static at logic 'HIGH' (+5V) or a digital ramp was fed into the DACs at a frequency of approximately 50 kHz.

Table 6.1 and 6.2 give an overview of irradiation levels and the bias mode used.
Doserates varied from 4 rads/minute to 30 rads/minute for Table 6.1 and from 5.7 rads/minute to 26 rads/minute for Table 6.2. This was due to smaller irradiation steps at the beginning of each test run with ever increasing steps in further course.

Table 6.1: Main test parameters for the first group of devices

device		digital inputs	Irradiation
Burr Brown 7541A KP	#1	dynamic	0 - 8 krad
PMI 7541A GP	#4	dynamic	0 - 8 krad
Analog Devices 7541A BQ	#4	dynamic	0 - 16 krad
Harris 7541 LN	#4	dynamic	0 - 100 krad
Harris 7541 LN	#5	static	0 - 25 krad
Sipex 7541A BQ	#2	dynamic	0 - 100 krad
Sipex 7541A BQ	#3	static	0 - 100 krad
Sipex DAC356	#1	dynamic	0 - 100 krad
Sipex DAC356	#3	static	0 - 12 krad

Table 6.2: Main test parameters for the second group of devices

device		digital inputs	Irradiation
Burr Brown 7802 KP	#1	dynamic	0 - 8 krad
Burr Brown 7802 KP	#2	static	0 - 8 krad
Analog Devices 7845 BQ	#1	dynamic	0 - 16 krad
Analog Devices 7845 BQ	#2	static	0 - 100 krad
Sipex HS7584C	#1	dynamic	0 - 25 krad
Sipex HS7584C	#2	static	0 - 100 krad

7. Test results

The results obtained will be presented on a device-by-device basis, beginning with a short description and a list of specifications according to the manufacturer and a brief resume of pre-irradiation characteristics, followed by the results of parametric, quasi static and dynamic testing at different total dose levels. Finally for each device a short interpretation of the results is presented.
Failure of any device to comply with any of the specifications during the tests will be mentioned. No comment on a characteristic therefore means that the device was still within the allowable tolerances.

7.1 BURR BROWN 7802 KP

Brief characterisation: dual, current output DAC with input latches and control logic. No internal voltage reference or OP-AMP.

Specifications (according to datasheet):

Integral nonlinearity	max.	+/- 1 LSB
Differential nonlinearity	max.	+/- 1 LSB
Gain error	max.	+/- 3 LSB (*)
Output leakage current	max.	10 nA (**)
Digital input current	max.	+/- 1uA (**)
Power supply current	max.	2mA
output current settling time	max.	0.8us (***)

(*) when using internal feedback resistor
(**) at 25 degrees Celsius
(***) to 0.01% of full scale; load resistor 100 .

Pre-irradiation characteristics
As can be seen in table 6.2, two devices (=4 DACs in total) were tested up to 80 krad. 2 DACs were irradiated under "static" input conditions (device #1 DAC A and DAC B), 2 DACs had "dynamic" inputs (device #2, DAC A and DAC B)
All DACs showed similar characteristics well within specifications.

Electrical parameters and quasistatic test results

Input current

Maybe the best parameter to see what is going on is the evolution of input current vs. input voltage applied to the shorted digital input pins ("digital input voltage") during irradiation. Figure 7.1.1 shows the input current of device #1 before the tests started.

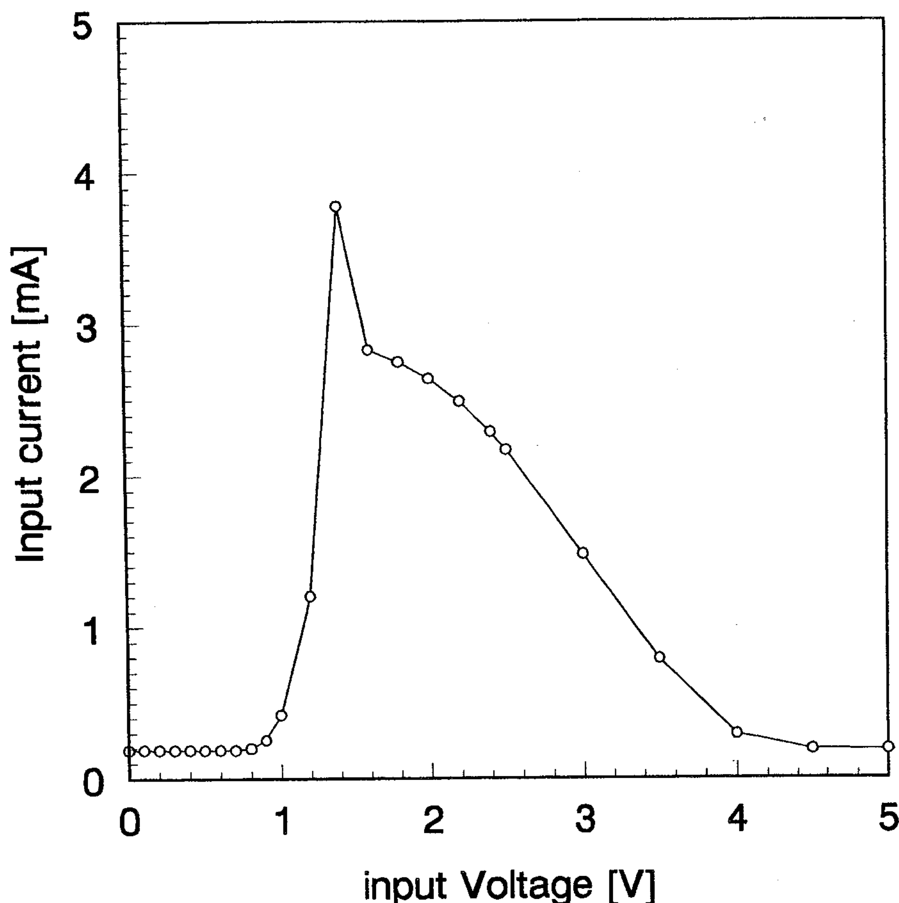


Figure 7.1.1: Input current vs. digital input voltage for Burr Brown 7802 #1 prior to irradiation.

It can be seen that the input current is very small as long as the digital input voltage is within allowed logic levels (i.e. 0V to 0.8V and 2.4V to supply voltage, respectively). Between these levels the MOSFETs of the input buffers and current switches operate in their linear region, corresponding to a sharp surge in input current.

This behaviour can be qualitatively unterstood by examining the current flow in a single CMOS inverter (only a brief overview will be given here; for a complete treatment of radiation effects on CMOS devices see [5] and for an in-depth coverage of radiation effects on MOS structures see [6]).

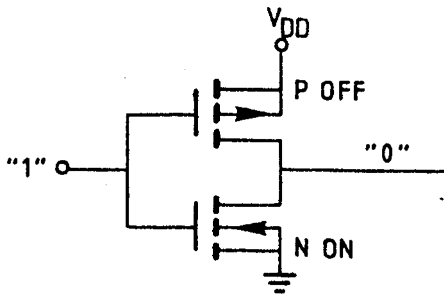


Figure 7.1.2: CMOS inverter

If the input voltage (=gate voltage of the MOSFETs) is kept to ground, the n-MOS transistor is in its nonconductive state, while the gate-source voltage of the p-MOS transistor is equal to $-V_{dd}$, and consequently its channel is conductive. The current is limited by the leakage current of the n-MOSFET. In case the input voltage is equal to Vdd, the p-MOS transistor is in its nonconductive state and limits the current. Between these input voltages, however a region exists where both transistors are in their transition phase where the current flow increases considerably. At an input voltage of about half the supply voltage the inverter output changes its logic state.

It is well known that the I-V characteristics of p- and n-MOSFETs change under the influence of ionising radiation: Threshold voltages shift towards lower voltages due to a buildup of positive charge in the gate oxide, and the leakage currents increase in magnitude. It is also known that these changes depend on the type of transistor (n-MOSFETs usually show greater shifts than p-MOSFETs) and the bias conditions (the worst case is usually the gate biased positive with respect to the substrate).
Briefly the big problem is the n-MOSFET of the inverter. As the threshold voltage is moving to lower voltages with increasing total dose and finally even crosses 0V, the quiescent current of the device increases sharply. The principle of that mechanism is explained in the text of figure 7.1.3.

Increased leakage can also be found predominatly in n-MOSFETs. The p-MOSFET, on the other hand, poses much less problems because the worst thing that could happen is a threshold voltage shift far enough so that the transistor cannot be turned ON anymore. However, long before that happens the characteristics of the n-MOS transistor have shifted to a point where it is no longer possible to switch that transistor OFF. It is clear that as soon as the threshold voltage of the n-MOSFET shifts into the logic LOW region (0 - 0.8V), reliable operation can not be guaranteed any more. By the time when it crosses 0V changes in logic state become impossible ("logic failure").
One should carefully distinguish between leakage as a result of a threshold voltage shift as described above and leakage caused by poor quality of the field oxide. The latter can also be found in many devices and is caused by trapped charge in the field oxide, especially in those parts adjacent to the gate oxide ("bird's beak"). It causes leakage currents at the periphery of the transistor. Contrary to threshold voltage shift it leads to a general increase in quiescent current, not limited to the region near the current peak. So if an overall current increase in the "flat" part of the current characteristics is observed (e.g. in the region below 0.8V in

Figure 7.1.1) this is almost certainly due to this mechanism.

Before the device fails completely some secondary effects might become apparent like slowing down of switching speed. This is due to interface states created by the irradiation which in turn distort both the I-V ("transconductance") and C-V characteristics, thereby reducing switching speed.

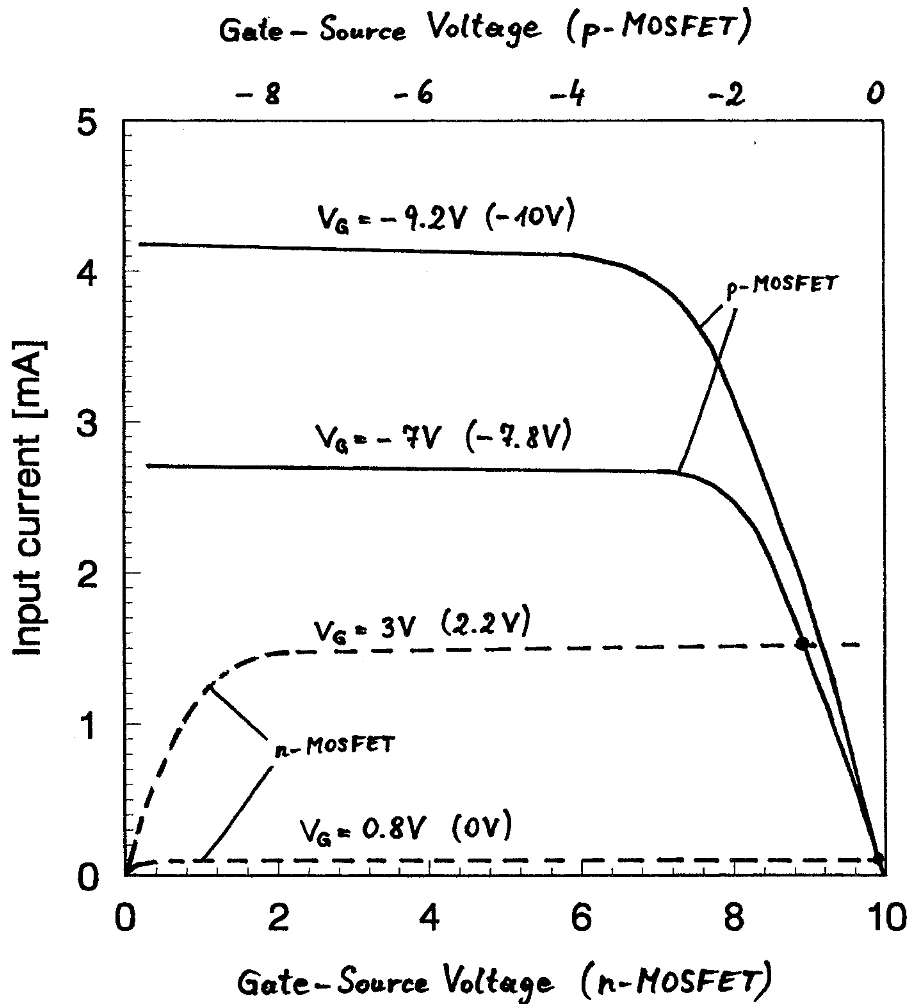


Fig. 7.1.3: Graphical determination of the output voltage and supply current of a CMOS inverter: A few rules are sufficient to calculate this voltage provided the characteristics of the transistors are known.

1) The current through both transistors is the same

2) The sum of the gate-source voltages of the p- and the n-MOSFET is equal to the supply voltage (here +5V)

The broken lines show the drain current of an unirradiated n-MOSFET as a function of drain-source voltage for a gate voltage of 0.8V and 3.0V, resp. In the linear region the curves almost coincide. The solid curves show the same characteristics for a p-MOSFET. The polarity of all voltages is negative in that case (right end of the figure corresponds to 0V). To determine the output voltage for a given input voltage (e.g. 0.8V) one has to look at the corresponding curve for the n-MOSFET and determine the intersection with the "complementary" curve of the p-MOSFET (i.e. 10V-0.8V=9.2V). This intersection (Point X) is still in the linear part. The x-coordinate yields the output voltage of the inverter, the y-coordinate the current flow. Applying this method to a different input voltage (e.g. 3.0V) shows that now the output voltage is somewhat lower and the current increased considerably (Point Y).

To see the influence of irradiation one has to bear in mind that charge buildup in the oxide acts as if the gate voltage for all I-V curves is lowered by an amount about equal to the shift in threshold voltage. Therefore the curves in the graph now describe the behaviour for gate voltages lower than the original ones. In brackets a shift by 0.8V for both n- and p-MOSFET has been assumed. Now Point X describes the situation for an input voltage of 0V instead for 0.8V. Similarly, the current for an input voltage of 2.2V is already about as high as was previously the case for 3.0V. The current peak, before irradiation located close to 5V, also shifted by the same amount.

Discussion
Although the actual DAC is certainly much more complex, the general features described above can be found in the I-V relationship as shown for device #1 in Fig.7.1.4

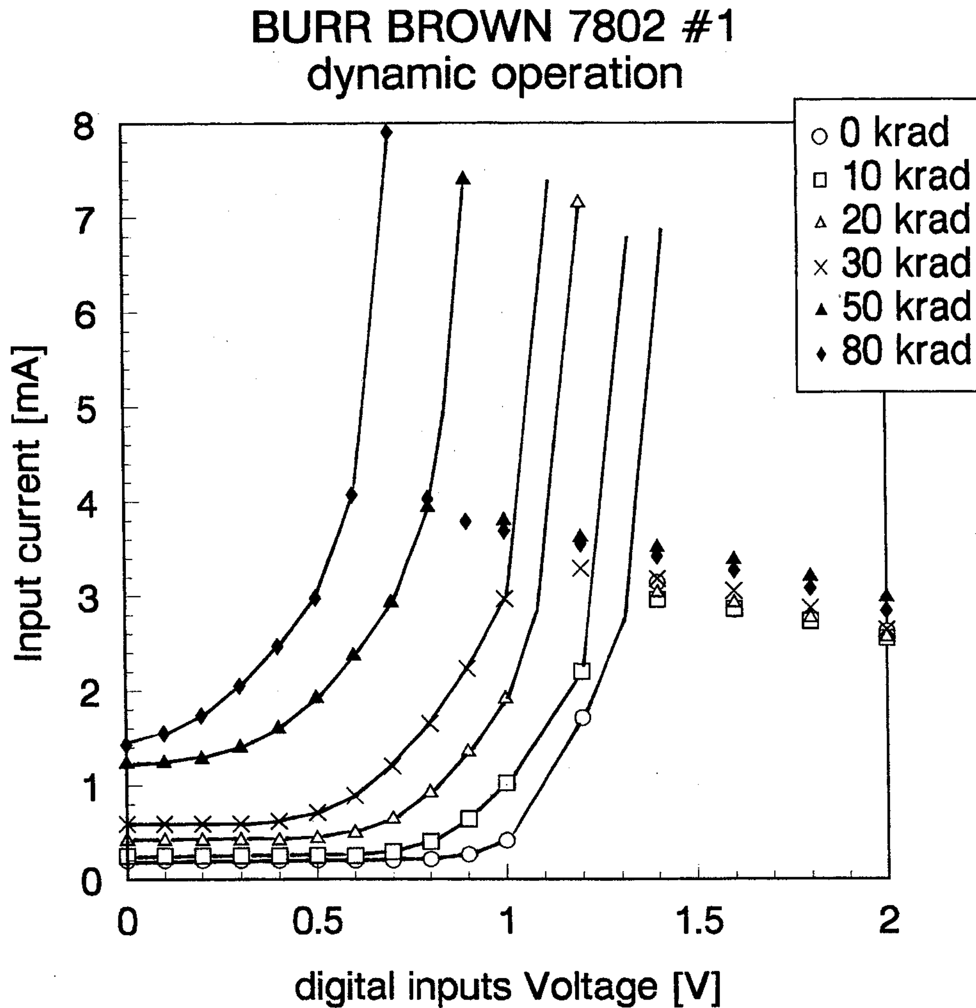


Figure 7.1.4: Input current vs. digital input voltage for several total doses for device #1. For reasons of clarity only the region between 0 and 2V is shown. In the left part of the curve the datapoints have been connected to show the almost linear shift to lower voltages.

One can see

a) an increase in leakage current with increasing total dose. This can be seen best by comparing the input current for a digital input voltage of 0V.

b) that the input current - input voltage curve shifts towards lower voltages, reflecting the shift in threshold voltage of the n-MOSFETs. This shift seems to be fairly linear with total dose.

It is interesting to compare this behaviour to the results for device #2 (Fig. 7.1.5)

The difference between them was their bias condition during irradiation: while #1 had the digital inputs continuously changing, device #2 had all the inputs tied to +5V, and consequently one of the n-MOSFETs acting as a current switch at each leg of the R-2R ladder was turned ON all the time, the other transistor was OFF (see Figure 7.1.6). Of course this also meant that all the other MOSFETs in that device did not change their biasing condition, too. One might therefore expect a higher radiation sensitivity for device #2 because 50% of

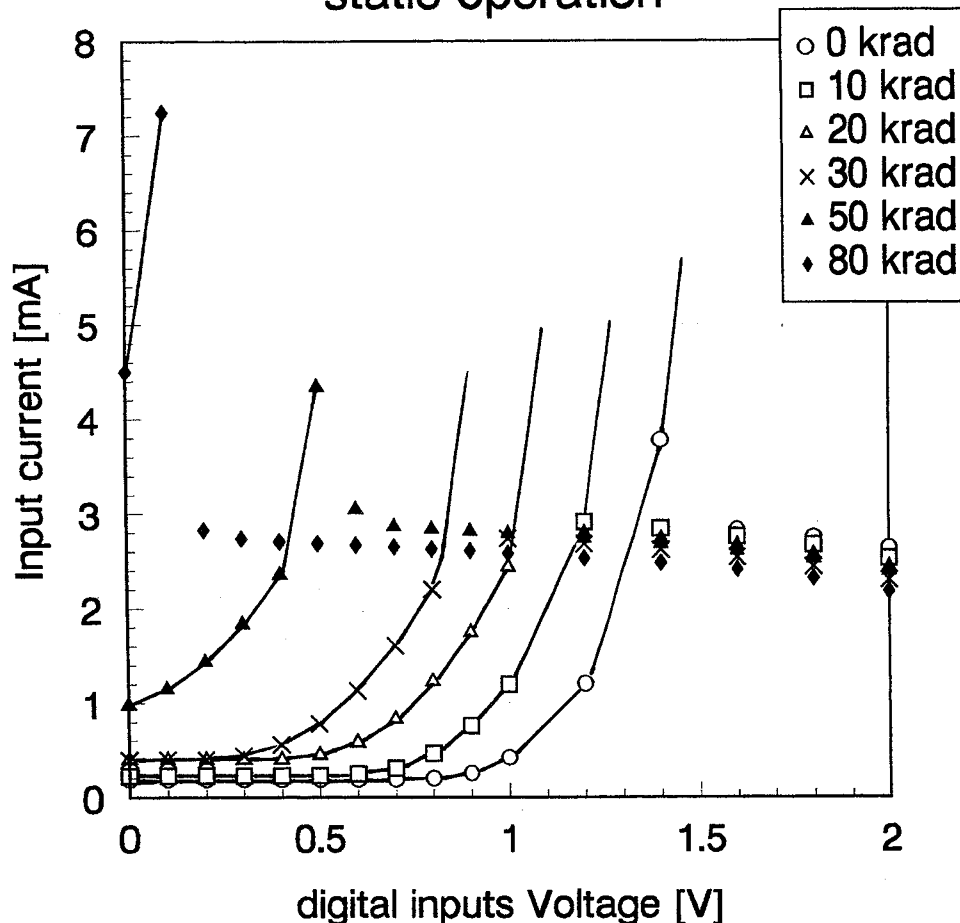


Figure 7.1.5: Input current vs. digital input voltage for several total doses for device #2. For reasons of clarity only the region between 0 and 2V is shown. In the left part of the curve the datapoints have been connected to show the almost linear shift to lower voltages.

the transistors were constantly biased to "worst case", allowing bigger changes to take place. As the overall behaviour of a complex device is determined by its most affected parts, this means that constant bias leads to greater device degradation.

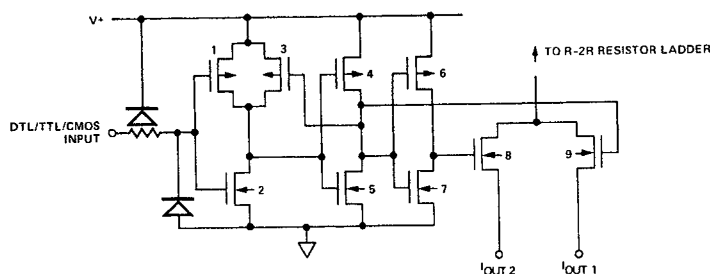


Figure 7.1.6: Schematic of the current switches at the end of each leg of the R-2R resistor ladder. Driven by different stages in an inverter chain, one n-MOSFET is always switched ON, the other is OFF.

And in fact it turned out that device #2 showed complete functional failure after 80 krad;by then no change in logic states was possible any more. One should recall that the change in logic state of an inverter takes place approximately at the point where the input current reaches its maximum; this point obviously shifted into the region between 0V and 0.8V for higher doses, finally leading to a complete functional failure after 80 krad. The total dose that is necessary to achieve this is dependent on the irradiation bias; obviously static bias is worse than dynamic bias.

Conclusions

From figures 7.1.4 and 7.1.5 it can be seen that due to the shift of the input current peak the input current specification of max. 2mA is not fulfilled for total doses above 30 krad (taking an input voltage of 0.8V as valid logic LOW). For static operation (device #2) this figure is even lower, close to 25 krad.
It can also be seen that the input current for small voltages, i.e. close to 0V, also increases with total dose. This seems to be mostly a result of growing leakage current of all the transistors (caused by charge trapping in the field oxide) in the DAC because in that region of the curve the effect of the threshold voltage shift is negligible.

Output leakage current

Output leakage current was measured with nominal supplies and all digital inputs set to LOW. It is basically determined by the deterioration of the n-MOSFET acting as a switch at the end of each leg of the R-2R resistor ladder (see Figure 7.1.6).

These 2 MOSFETs redirect the current between two output pins of the DAC, both of them driven by different outputs of an inverter chain.
Several major changes can be caused by irradiation:

* The leakage current of the MOSFETs increases
* The shift in threshold voltage eventually leads to a noticeable current flow although the driving inverter delivers a proper LOW on the gate (if it is assumed that all n-MOSFETs in an IC are affected equally, then an inverter will still produce a proper LOW level because for this state the n-MOSFET has to be conductive, the p-MOSFET nonconductive. This condition is easily achieved, even if irradiation caused some degradation and even if the prior inverter stage produces a somewhat degraded HIGH output). The quality of the logic HIGH level will deteriorate.

Observations

Table 7.1.1 shows that there is a big difference in the output leakage currents for device #1 and #2; both DACs of each individual device showed a very similar behaviour as expected for identical bias conditions.
A closer examination of the change in analog output between "startpoint" (digital input code 00..00) and "endpoint" (digital input code 11..11) shows that for device #1 these changes are comparable. For device #2 hardly any change in the "endpoint" value was observed, but a

Table 7.1.1: Output leakage current for different total doses. Measurements were taken for a input voltage at the digital inputs of 0.2V.

	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
7802 #1 DAC A	1.6pA	5.3nA	230nA	205nA	1.3uA	19uA
7802 #1 DAC B	1.3pA	2.9nA	175nA	270nA	1.1uA	16uA
7802 #2 DAC A	1.2pA	88nA	670nA	980nA	29uA	n.f.
7802 #2 DAC B	1.5pA	94nA	600nA	1.04uA	29uA	n.f.

big change in "startpoint" value took place. This corresponds to a small leakage current for the MOSFET switching to current output #2 and a large leakage current for the second MOSFET, leading to current output #1 (Figure 7.1.6). This implies that a positive bias on the gate of an n-MOSFET during irradiation, as it was the case for the second MOSFET, leads to a quicker degredation compared to almost no bias which was the case for the first one. This is not surprising as a positive gate bias encourages the formation of trapped positive charge close to the interface where it has the greatest effect on threshold voltage; leakage caused by poor field oxide is also enhanced by positive bias.

Conclusions

Device #1 failed to comply with the specification somewhere between 10 and 20 krad, device #2 already failed at about 6 krad.

Digital input current

The limit given in the specifications is quite high (+/-1uA). For both devices this parameter increased from a few pA to more than 1 uA at 80 krad. The latter value is not negligable as an additional current of that magnitude changes the output voltage by approximately 10-20mV (2-4 LSB). However, compared to the changes that had already taken place at that stage of the irradiation this was of no great importance.

Conclusions: both devices finally failed on that specification, but only after a total dose of 80 krad.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.1.2.

Table 7.1.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. (n.e.: not evaluated; n.f.: device not functional any longer)

ALL NUMBERS ARE IN mV

Burr Brown #1 DAC A

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	-0.1	+0.9	+1.9	+3.5	+24.2	+286.8
endpoint	-0.3	+0.6	+2.4	+3.2	-11.8	-297.0
Gain	-0.2	-0.3	+0.5	-0.3	-36.0	-583.8

Burr Brown #1 DAC B

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	n.e.	-0.3	n.e.	+1.0	+19.6	n.e.
endpoint	n.e.	+0.1	n.e.	+0.9	-20.8	n.e.
Gain	n.e.	+0.4	n.e.	+0.1	-40.4	n.e.

Burr Brown #2 DAC A

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	n.e.	+1.4	+8.2	+22.1	+531	n.f.
endpoint	n.e.	+2.4	+5.8	+8.5	+6.9	n.f.
Gain	n.e.	+1.0	-2.4	-13.6	-524	n.f.

Burr Brown #2 DAC B

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	n.e.	+2.6	+8.6	+18.1	+550	n.f.
endpoint	n.e.	+2.0	+3.5	+3.9	+5.8	n.f.
Gain	n.e.	-0.6	-5.1	-14.2	-544.2	n.f.

The evolution of INL and DNL can best be seen by a graphics plot of these parameters; numerical values are given in Table 7.1.3.

Table 7.1.3: Numerical values of INL and DNL for Burr Brown 7802 #1 and #2. Values are in mV. (n.e.: not evaluated; n.f.: device not functional any more)

ALL NUMBERS ARE IN mV

Differential nonlinearity

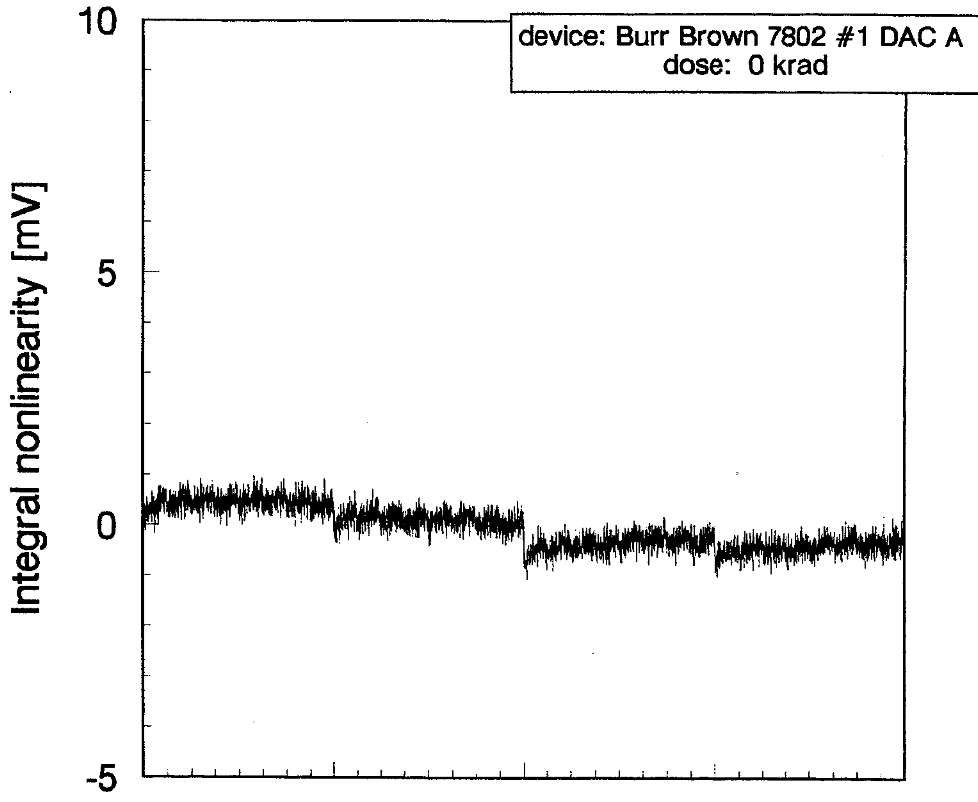
	0 krad	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
#1 DAC A	0.9	0.7	1.1	1.1	1.4	2.6	6.2
#1 DAC B	0.8	n.e.	0.8	n.e.	1.7	2.0	n.e.
#2 DAC A	0.9	n.e.	1.2	6.2	10.9	13.9	n.f.
#2 DAC B	0.9	n.e.	1.7	n.e.	6.5	8.5	n.f.

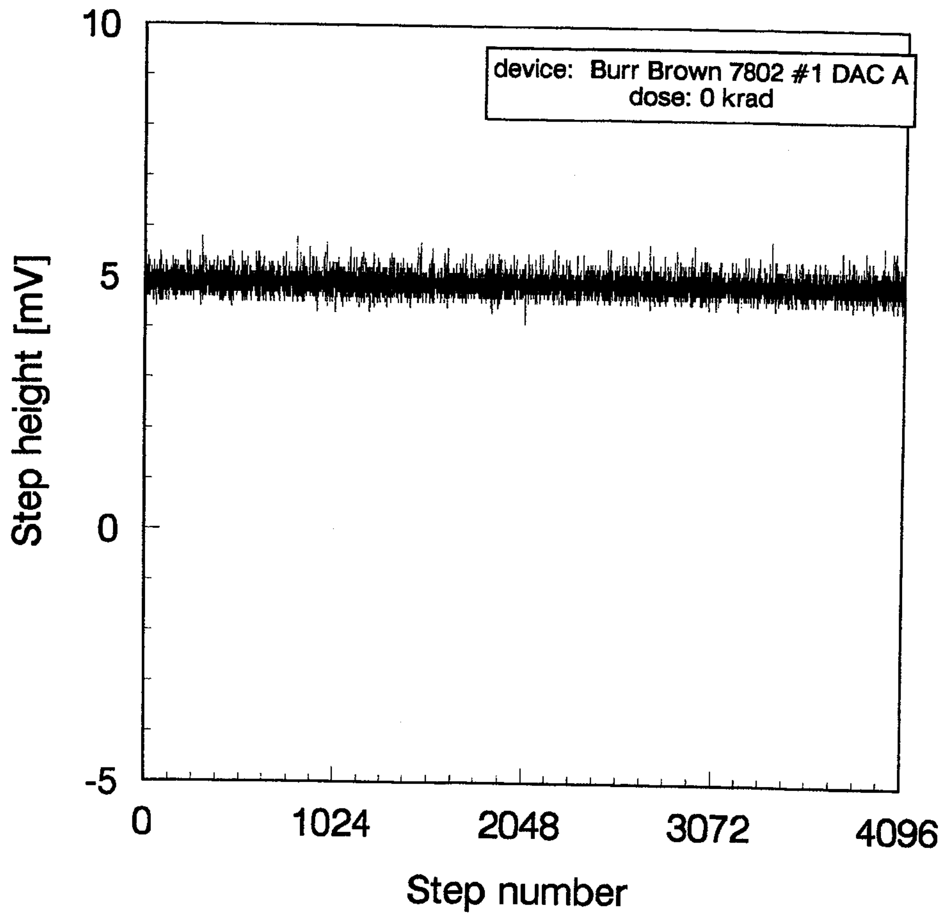
Integral nonlinearity

	0 krad	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
#1 DAC A	1.1	1.2	1.0	1.4	1.3	2.7	5.7
#1 DAC B	0.9	n.e.	1.0	n.e.	1.8	1.9	n.e.
#2 DAC A	0.9	n.e.	1.9	4.6	7.8	11.2	n.f.
#2 DAC B	1.7	n.e.	1.8	2.9	6.5	10.7	n.f.

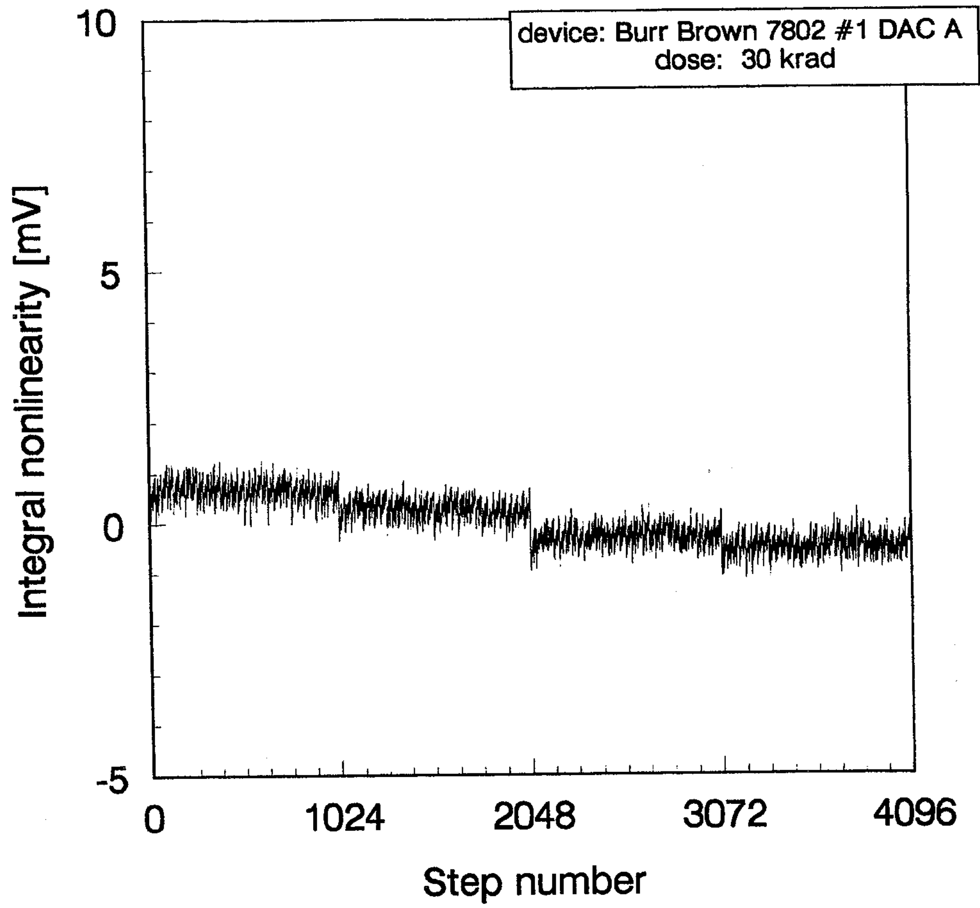
Figure 7.1.7 shows INL and DNL for device #1 prior to irradiation. Both parameters are well within specifications, although small discontinuities are visible for INL at major bit changes. Figure 7.1.8 shows the evolution of INL with increasing total dose. At 30 krad no obvious changes have taken place; after 80 krad, however, the appearance changed significantly. The rather smooth curve developed into a kind of sawtooth-like shape, reflecting the growing mismatch between individual bits.

The evolution of DNL, shown in Figure 7.1.9, can give some additional information. Initially confined to a small band of about 2mV width around the "ideal" value of 4.88mV (=1 LSB), it can be seen that after 80 krad the step size at major bit changes is greatly reduced and even nonmonotonic at steps 1024 and 3072.





<u>Figure 7.1.7:</u> Quasistatic parameters of device #1 prior to irradiation



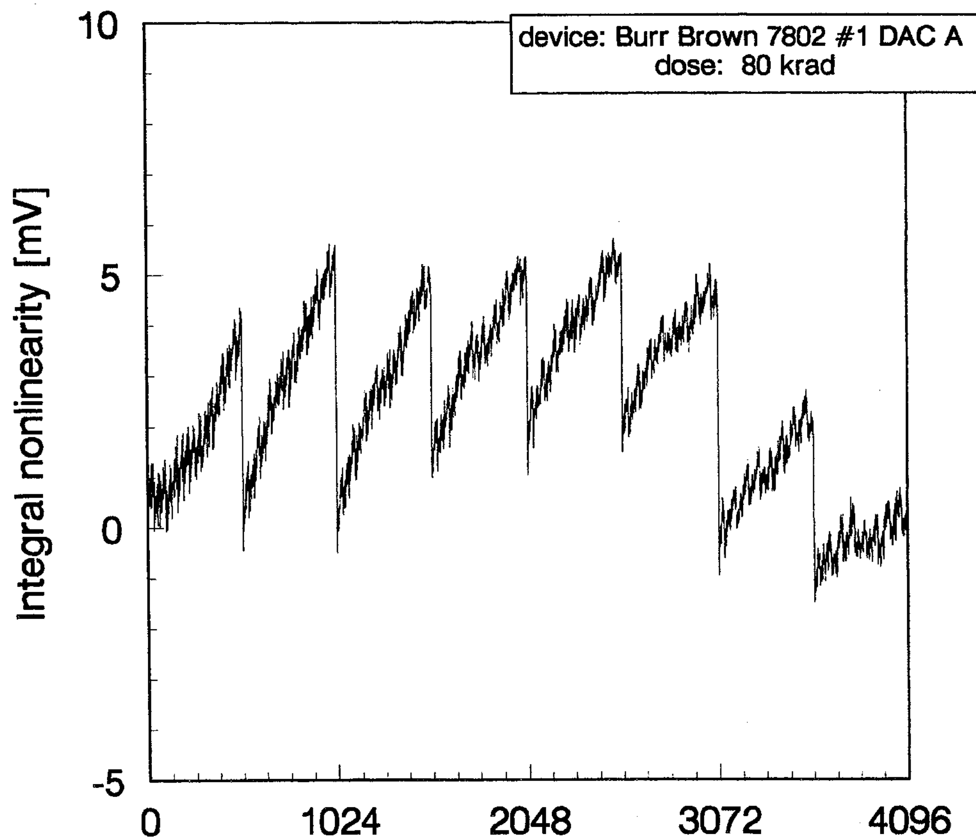
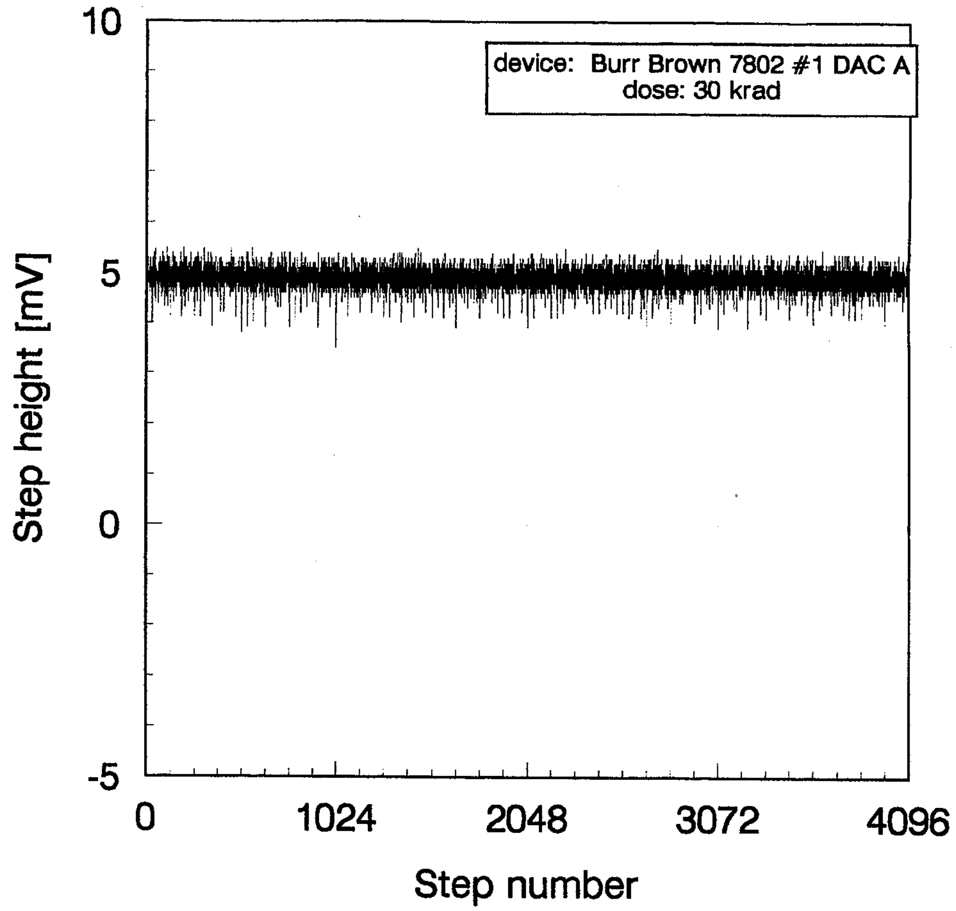


Figure 7.1.8: Evolution of integral nonlinearity with increasing total dose for device #1, DAC A. DAC B showed a similar behaviour.



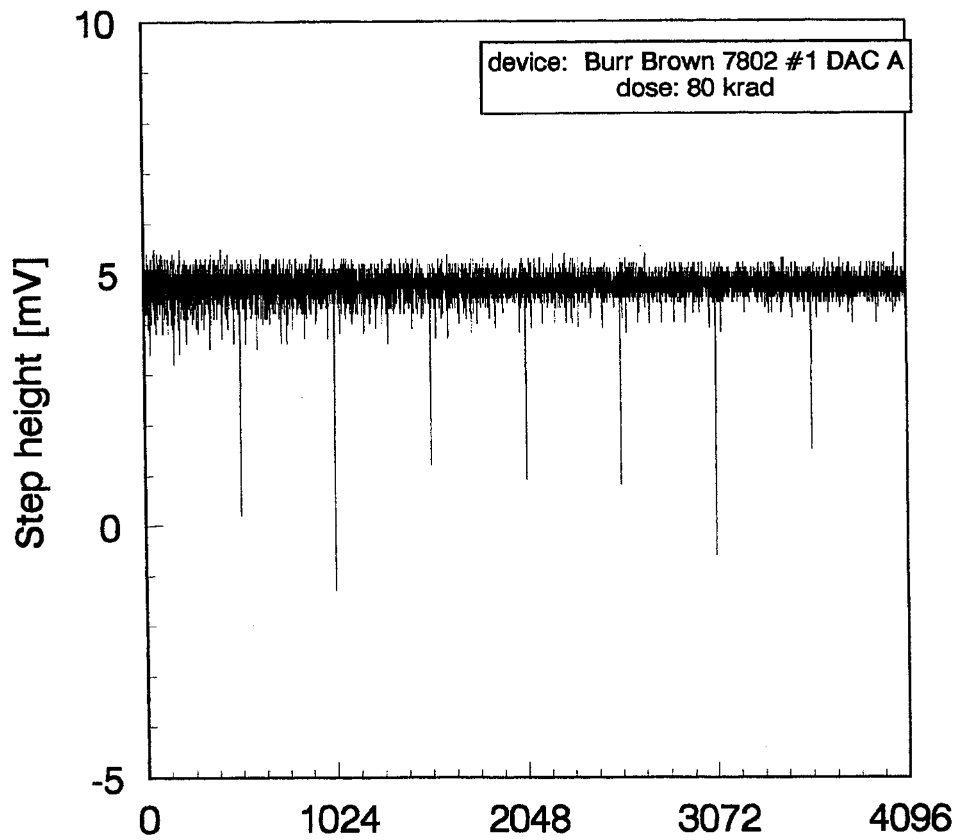


Figure 7.1.9: Evolution of differential nonlinearity with increasing total dose for device #1, DAC A. General behaviour of DAC B was similar.

Discussion

A major bit change is said to take place when the increase of digital input code by 1 causes most (or all) bits to change, e.g. 00111..11 -> 0100..00. The output voltage is determined by the amount of current that is directed to current output pin 1. A smaller than usual increase or even decrease in output voltage necessarily means that this current hardly increased or even decreased. As it can be safely assumed that turning a n-MOSFET OFF is the main problem after a certain amount of irradiation, this means that the current cannot be completely redirected into one of the 2 outputs. So a small portion of it is "leaking" to the wrong output, less current than usually is being converted into a voltage by the external circuitry. An immediate consequence is that the voltage step when turning ON a single bit can only become smaller, but never larger (if the resistor values remain constant). This was observed during the tests: for device #1 the MSB value decreased by 18.5mV, for device #2 by 273mV after 50 krad. The other bits showed similar changes in proportion to their weight. This means for example that the corresponding figures for bit 10 were 9.4mV and 131mV, respectively.

The big difference in the development of gain figures (Table 7.1.2) between device #1 and #2 is a result of different irradiation bias conditions. For DACs with "static" inputs the unbiased switching MOSFETs suffered almost no degradation (=no change in output voltage), while the biased MOSFETs showed a leakage current about twice as large as compared to the equivalent MOSFETs of device #1, resulting in an output voltage shift about twice as large. In device #1, however, both transistors were affected equally because each of them spent the same amount of time in biased and unbiased condition. This result all out confirms the theory of positive gate bias on MOSFETs being worst case.

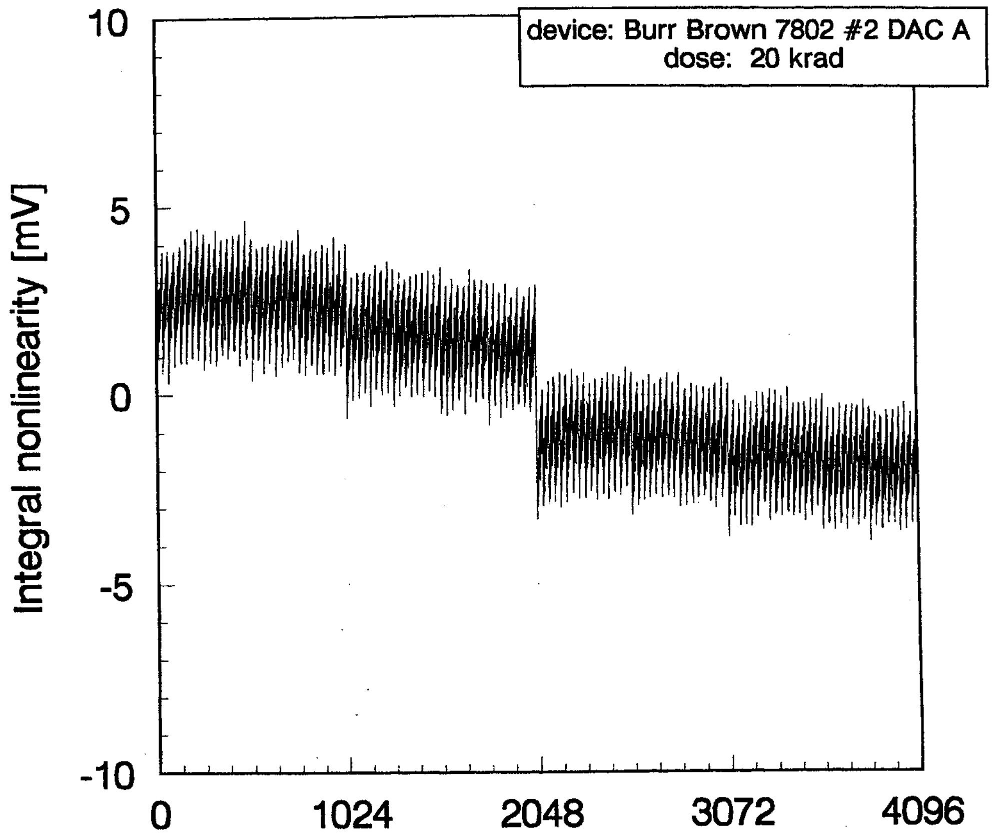
Close examination of the endpoint values revealed that for device #2 these increased with increasing irradiation. The effect was small (about 5mV after 50 krad), but detectable for both DACs. This can only be explained by two mechanisms: either the resistor values in the R-2R ladder decreased slightly, allowing more current to flow, or the resistor ratio between the ladder resistors and the internal feedback resistor changed. Both effects could lead to the observed results. The main conclusion seems to be that it cannot be taken for granted that resistors are not at all affected at these relatively low total doses.

If for a digital input code of 00..00 the output voltage shifts to higher values this means that a certain amount of current is leaking to the wrong output path. The same holds true for a smaller output voltage after irradiation for a input code of 11..11. The overall effect is a decrease in gain as described above. If all bits were affected equally, then the total gain would be reduced by a certain amount, but the DNL figures would only change very slightly, the INL (according to its definition) would stay the same. Only if some bits show a greater relative leakage than other ones, then this mismatch causes INL and DNL to fluctuate and sharp steps occur in the plots when these most degraded bits change state.

This is the case for device #1, DAC A, where especially bit 9 (representing decimal 512) and bit 10 (decimal 1024) have been affected.

The results for device #2 (Figures 7.1.10 and 7.1.11) were qualitatively similar, but radiation effects were already visible at a much earlier stage. Here bits 10 (decimal 1024) and 11

Integral nonlinearity



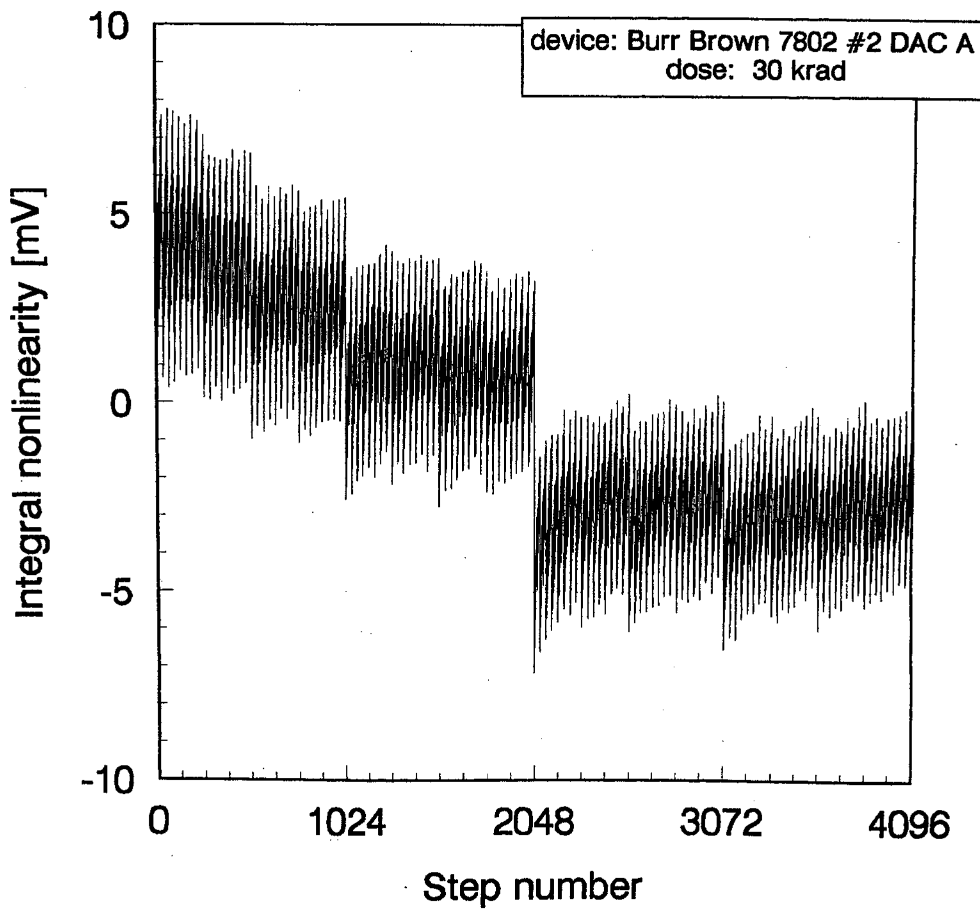


Figure 7.1.10: Evolution of integral nonlinearity with increasing total dose for device #2, DAC A. DAC B showed a similar behaviour.

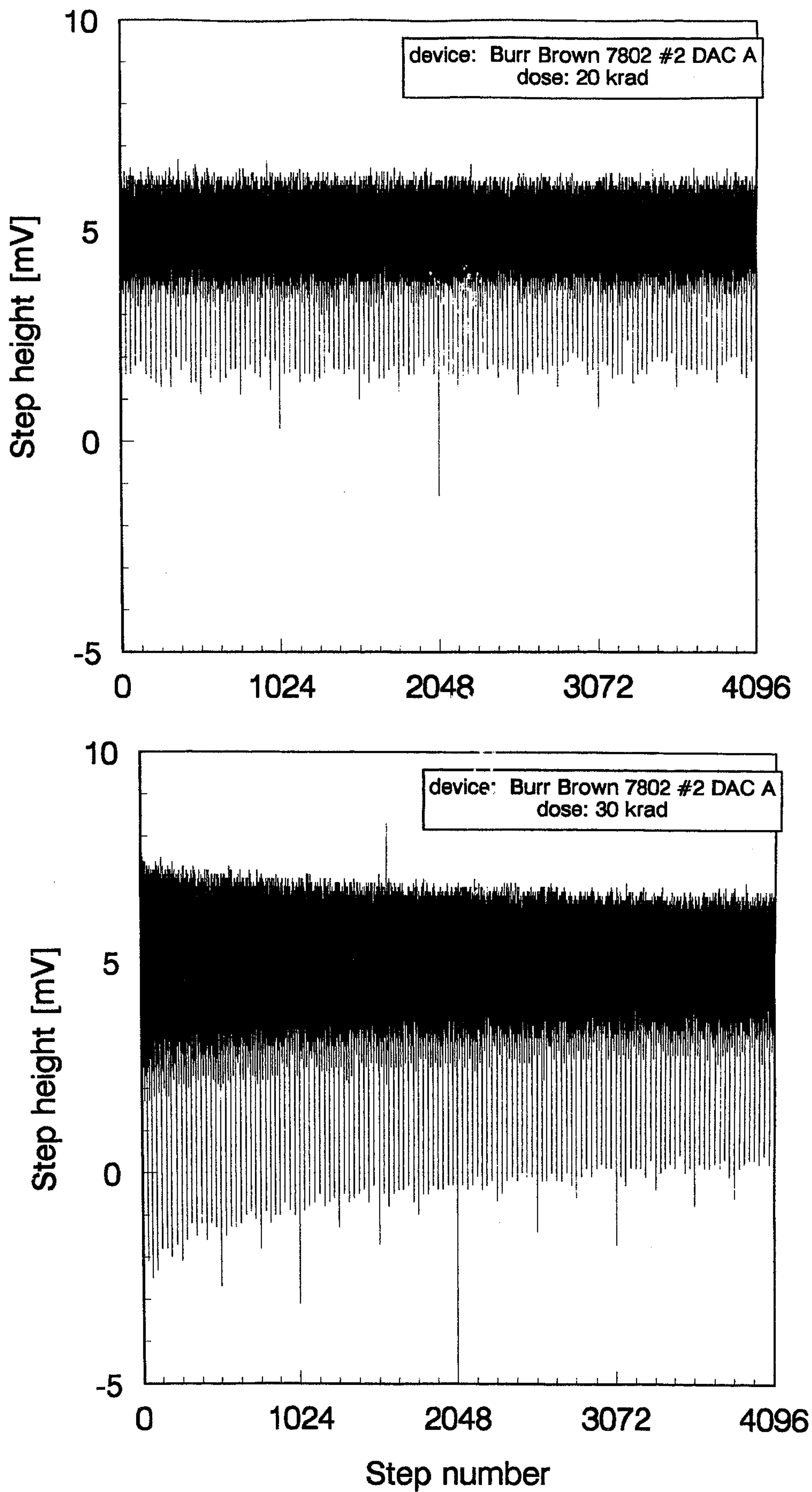


Figure 7.1.11: Evolution of differential nonlinearity with increasing total dose for device #2, DAC A. General behaviour of DAC B was similar.

(decimal 2048) were most affected, but also the lower bits showed larger degradation than those of device #1. As the pre-irradiation curves looked very similar to those of device #1 they were omitted.

It should be kept in mind that the main indicator for a beginning degradation is a shift in the "startpoint" and "endpoint" values.

Conclusions
Device #1 failed on gain specifications between 30 and 50 krad, probably close to 40 krad. Failure due to degradation in DNL and INL figures was only detected after 80 krad.
Device #2 failed on gain specifications at about 25 krad; failure to comply with DNL was already detected after 20krad (nonmonotonicity at step 2048), while INL figures exceeded the allowable limit shortly after 20krad. Somewhere between 50 and 80 krad the device showed complete functional failure.

Dynamic parameters

Because of the equipment problems already described earlier (see Section 5.3) the absolute measurement values for the dynamic parameters Signal/Noise Ratio (SNR) and Total Harmonic Distortion (THD) are not reliable. For low digital sinewave frequencies (a full period of the sinewave is represented by many points, so the stepheight from one point to the next is small) the numbers should be quite accurate; for higher frequencies only the relative change of the results for different total doses will give some qualitative information; the numbers itself are meaningless.

The following table shows the results obtained with the HP3653A Spectrum Analyzer; digital data was updated at a rate of 150kHz, and sinewaves of different frequencies were fed into the DAC under test (f_{in}=125Hz and 9.875kHz). It was avoided to test frequencies that are a multiple of 50Hz because of possible mains noise pickup.

Table 7.1.4: Figures for THD and SNR for two different input frequencies. Numbers are in dB.

Total Harmonic Distortion

f_{in}= 125 Hz	0 krad	5 krad	10 krad	20 krad	30 krad	50 krad
7802 #1 DAC A	-81.8	-81.6	-80.1	-79.6	-82.3	-80.2
7802 #2 DAC B	-81.4	n.e.	-81.3	-81.3	-81.1	-72.7
f_{in}= 9.875 kHz						
7802 #1 DAC A	-64.4	-64.1	-64.4	-63.8	-63.0	-60.5
7802 #2 DAC B	-60.1	n.e.	-63.7	-63.1	-61.7	-45.7

Signal/Noise Ratio

f_{in}= 125 Hz	0 krad	5 krad	10 krad	20 krad	30 krad	50 krad
7802 #1 DAC A	-68.3	-68.5	-68.0	-68.3	-68.1	-68.2
7802 #2 DAC B	-68.4	n.e.	-68.3	-68.3	-68.2	-66.8
f_{in}= 9.875 kHz						
7802 #1 DAC A	-54.7	-54.9	-54.4	-54.4	-54.4	-51.6
7802 #2 DAC B	-53.7	n.e.	-54.5	-54.5	-54.1	-44.2

Discussion

The figures above indicate that for low frequencies like 125Hz the DACs perform close to their theoretical limit of approx. -72.8dB for their SNR. For device #1 the figures hardly change up to 50 krad; after 80 krad a significant deterioriation must have taken place which can be seen in the change in output waveform shown in Figure 7.1.12. Unfortunately no Spectrum Analyzer tests could be performed after 80 krad because of technical problems (HP-Vectra was not available). But as a similar slowing down in settling time was observable for device #2 after 50 krad (Figure 7.1.13), the change in numbers for SNR and THD between 50 krad and 80 krad for device #1 should be similar to the changes for device #2 between 30 krad and 50 krad.

Conclusion

No dynamic specifications except the maximum settling time for the output current were given by the manufacturer. The use of OP-AMPs to convert the current into a voltage slows down the settling time, so no direct observation of that figure is possible.
As the external OP-AMPs were not subjected to irradiation, the change in settling time and the degraded figures for SNR and THD after 80 krad for device #1 and after 50 krad for device #2 can undoubtedly be attributed to changes in the DACs. The most likely explanation is slower switching of the current switch MOSFETs.
It seems that these effects are a good indication that complete functional failure is not too far away, meaning that further irradiation will soon destroy the devices.
However, these noticeable changes only took place at doses when some static parameters had already failed to comply with specifications.

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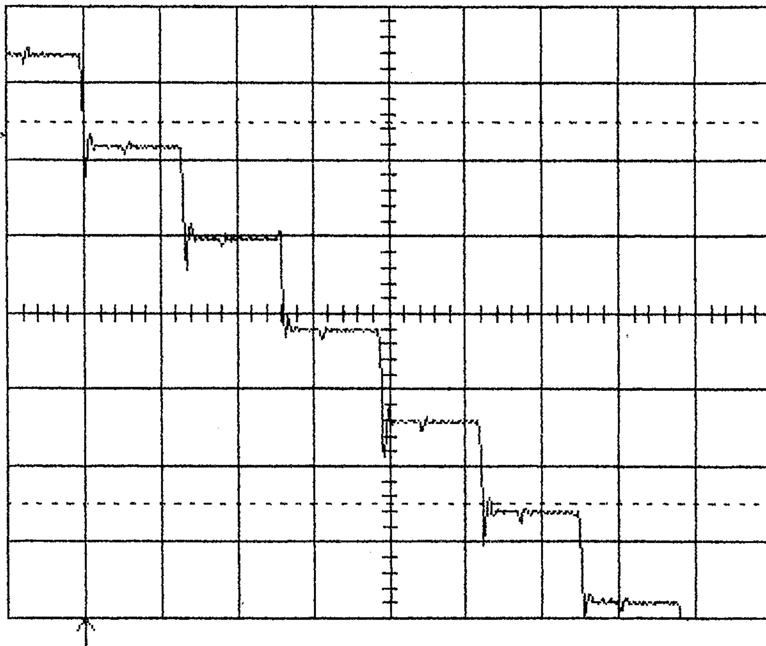


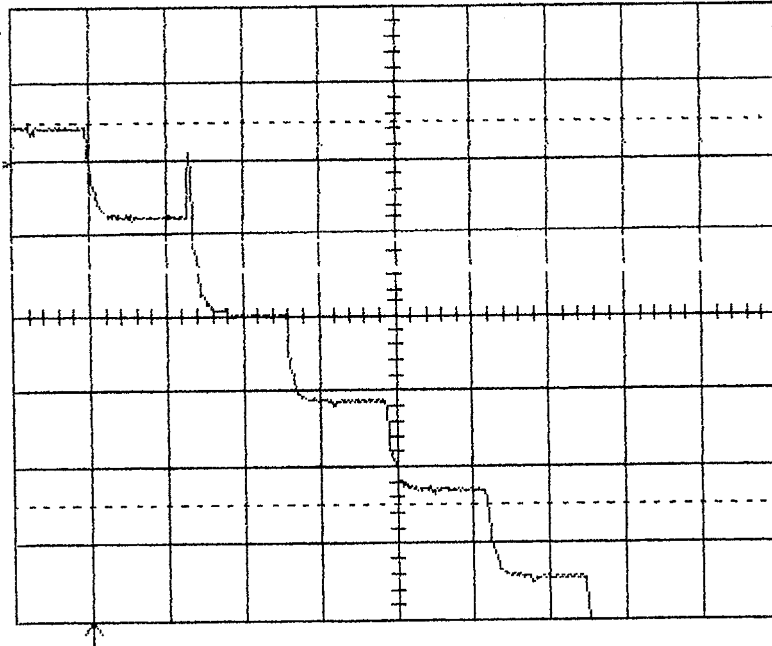


Figure 7.1.12: Hardcopy of the output signal of device #1 as seen on the oscilloscope. Digital inputs were updated at a rate of 150kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). The top picture shows the signal prior to irradiation; settling time is about 1.5us. No change in shape occurred up to 50 krad. After 80 krad, however, a detectable slowing down can be seen (bottom picture). Settling time now was an estimated 3us.

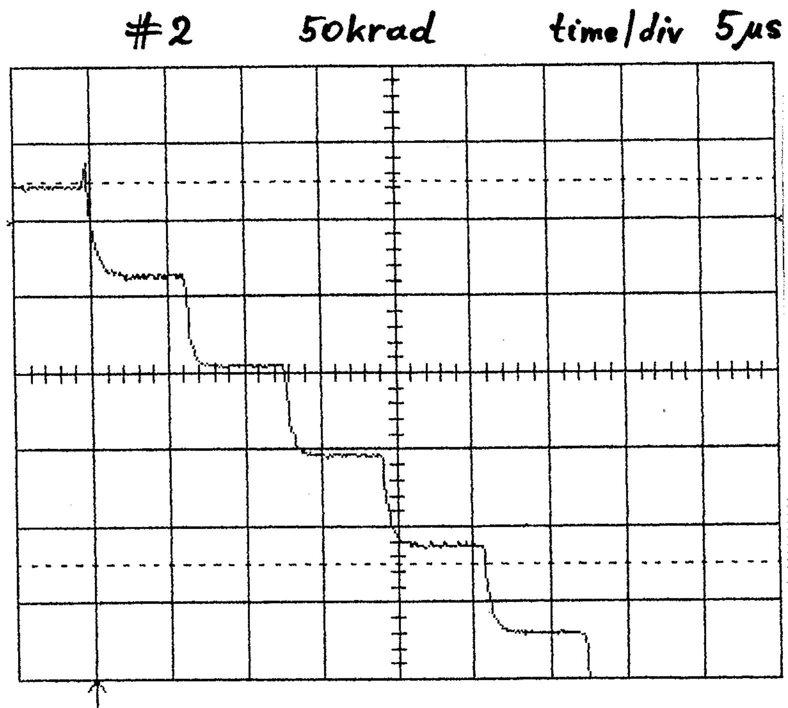


Figure 7.1.13: Same data as in Figure 7.12, for device #2. Here the shape of the initial output signal remained unchanged up to 30 krad After 50 krad the settling time was considerably slower

7.2 SIPEX 7584C

Brief characterisation: quad current output DAC with input latches and control logic. No internal voltage reference or OP-AMP.

Specifications (according to datasheet):

Integral nonlinearity	max.	+/- 0.5 LSB
Differential nonlinearity	max.	+/- 1 LSB
Gain error	max.	+/- 2 LSB (*)
Output leakage current	max.	10 nA (**)
Digital input current	max.	+/- 4uA (**)
Power supply current	max.	10mA (***)
Output current settling time	max.	0.8us
Reference input resistance		5k < R < 15k

(*) when using internal feedback resistor
(**) at 25 degrees Celsius
(***) V_{in}=0.8V or 2.0V. For 0V or 5.0V max. current is 1mA

General remarks

As can be seen in table 6.2, two devices (=8 DACs in total) were tested up to 80 krad. 4 DACs were irradiated under "static" input conditions (device #1), 4 DACs had "dynamic" inputs (device #2).

Pre-irradiation characteristics

Prior to irradiation their characteristics were in accordance with specifications except for INL (0.75 LSB for some of the DACs) and reference input resistor value which was a bit lower than 5k .

Electrical parameters and quasistatic test results

Input current

Figure 7.2.1 shows the influence of irradiation on the input current vs. digital input voltage curve for device #1, DAC D, which is representative for the DACs included in that package. (It is worth noting that all four DACs were individually adressable but had only one common power supply pin. The supply current therefore depends on the state of the input latches of

the 3 DACs that were not adressed; after power-up it might be random. This might lead to a constant offset in input current for different test runs. Therefore only information about changes in the current peak position can be deduced from these plots).
By comparing the parts left of the peak position a very small shift to higher voltages can be found. The magnitude of this shift is below 0.2V and therefore hardly detectable. Input current increased in general up to 50 krad. After 80 krad a sudden decrease was observed, together with a sudden "dip" in the curve where the peak used to be.

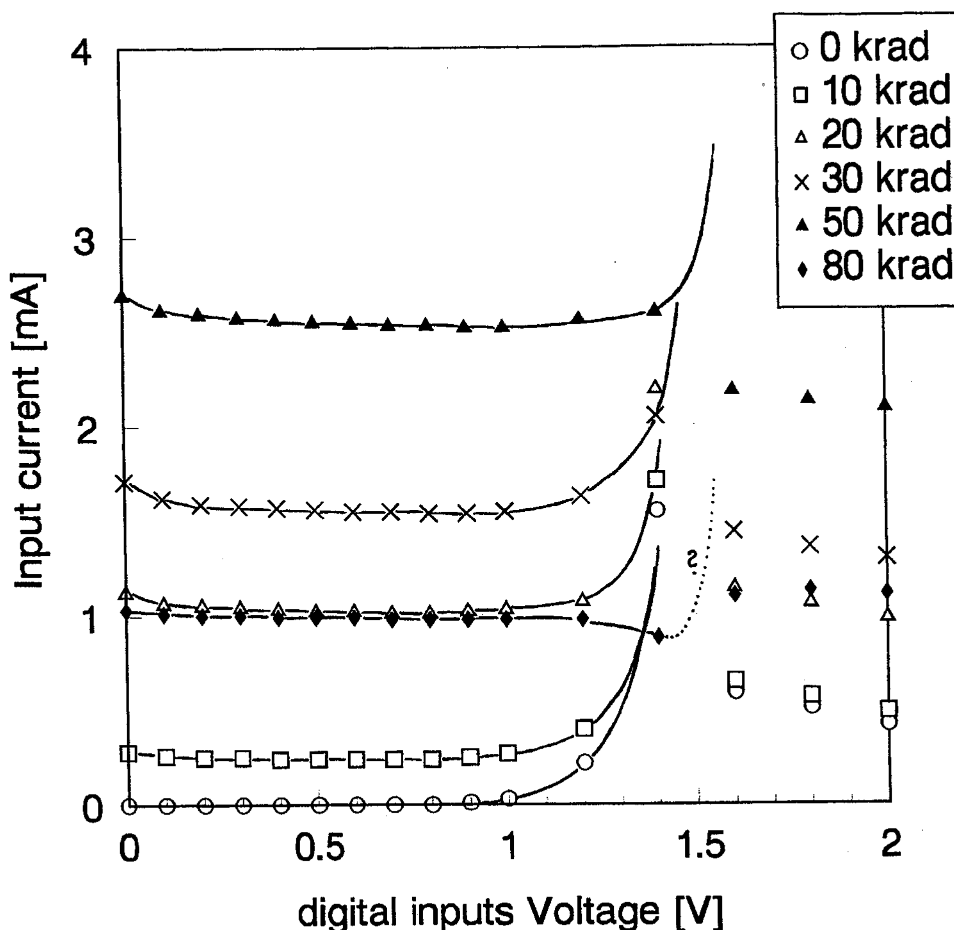


Figure 7.2.1: Input current vs. digital input voltage for several total doses for device #1. For reasons of clarity only the region between 0 and 2V is shown. In the left part of the curve the datapoints have been connected to show the almost linear shift

Device #2, which had been statically biased, showed a larger shift (about 0.4V) in current peak position, again towards higher voltages for increasing total dose. Input current increased up to 50 krad, too, and dropped after 80 krad.

Discussion

The observed effects are rather difficult to interpret. A shift in threshold voltage to higher values would imply negative charge build-up which has never been observed in a MOSFET simply because electrons are mobile even in the nonconducting oxide. What has been observed and what might be an explanation is the creation of interface states at the Si-SiO_2 boundary. These interface states have an effect that finally leads to higher threshold voltages

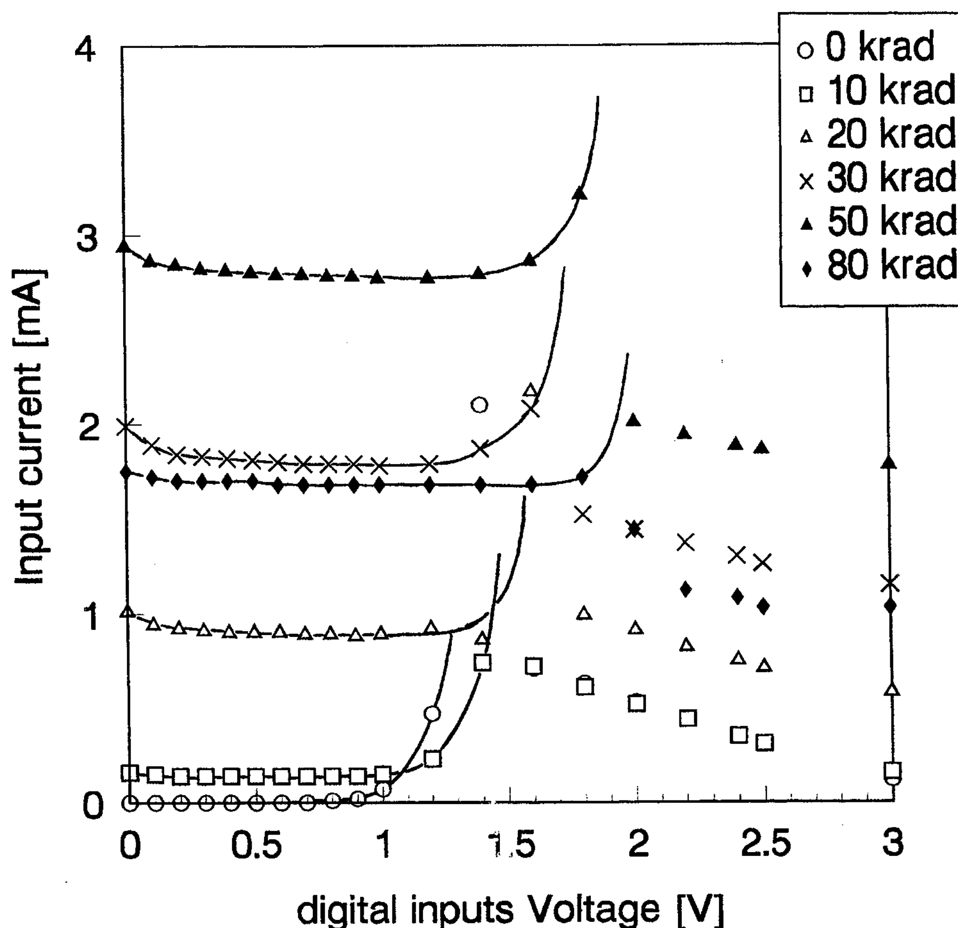


Figure 7.2.2: Input current vs. digital input voltage for several total doses for device #2. For reasons of clarity only the region between 0 and 3V is shown. In the left part of the curve the datapoints have been connected to show the almost linear shift

("rebound"). On the other hand their creation usually goes hand in hand with considerably slower switching speed. As no obvious slowing down was observed it might be concluded that

> a) the gate oxide of these devices was of good quality, allowing only very little trapping of positive charge
> b) this charge was more than offset by the effects of interface states created by the radiation.
> c) the density of these interface states is probably rather low as a high density would lead to considerably slower switching of the MOSFETs which was not observed.

The small shifts in threshold voltage (< 0.2V and 0.4V for device #1 and #2, respectively) are also an indication of a high quality gate oxide.
Even here it could be seen that keeping digital inputs constantly HIGH during irradiation causes faster degradation than "dynamic" bias. As already discussed this is due to the fact that in the first case about 50% of all MOSFETs are biased to "worst case" all the time, thereby suffering maximum damage.
The overall increase in quiescent current (consider e.g. the region from 0V to 1V in Figs.

7.2.1 and 7.2.2) is probably a consequence of increased leakage. However, the sudden decrease after 80 krad is not consistent with this explanation and probably other mechanisms are involved as well.

Conclusions

Both devices showed an input current in excess of 1mA after approximately 20 krad for a digital input voltage of 0V which was violating the specifications. No further increase was found after the current peaked at about 3mA after 50 krad.

The specification limit of 10mA for digital inputs of 0.8V and 2.0V was not exceeded by any device.

Output leakage current

Table 7.2.1 shows the output leakage current for two representative DACs of each device. The behaviour of the other DACs was almost identical and therefore omitted.

Table 7.2.1: Output leakage current for different total doses. Measurements were taken for an input voltage at the digital inputs of 0.2V.

	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
7584 #1 DAC A	0.4pA	0.5pA	1.0pA	0.9pA	0.6pA	0.9pA
7584 #1 DAC D	0.5pA	0.3pA	1.6pA	1.4pA	1.7pA	1.3pA
7584 #2 DAC A	5pA	1.4pA	0.7pA	0.6pA	2.3pA	1.2pA
7584 #2 DAC D	0.2pA	0.6pA	2.3pA	1.6pA	2.6pA	2.6pA

Observations

The measurements show that the output leakage currents basically stay the same; the fluctuation in values can be explained by the fact that their absolute values were at the measurement limit of the HP4145.

But another interesting observation should be mentioned: When a digital "11...11" was applied to the inputs, all the current coming from the reference voltage source should be directed to current output pin 1. The measurements showed that this current decreased with increasing dose. At 80 krad this decrease amounted to a difference in current of 5uA (device #1) and 8.5uA (device #2) compared to the pre-irradiation value. There are two possible reasons for this:

a) the second MOSFET switch (FET No. 8 in Figure 2.3) started leaking
b) the resistor values of the R-2R resistor ladder changed under irradiaton

In the first case a corresponding decrease in the "endpoint" output value of about 50mV to 85mV would be the consequence. As will be seen later this was not observed which leaves a change in resistor values as the only explanation. The internal feedback resistor which is

small change of the output voltage.
Another argument supporting changes in resistor values: The output MOSFET switches are closely matched. It is therefore very unlikely that for "dynamic" digital inputs one of these FETs shows no leakage at all (< 5pA) while the other one starts leaking with a final leakage current exceeding 5uA after 80 krad.

Conclusions
All 8 DACs, independent of irradiation bias, showed no increase in output leakage current and remained well within specifications.
Small changes in resistor values seem to occur. These changes were slightly bigger for "static" digital irradiation bias.

Digital input current

No major changes in digital input currents were observed for any device up to 80 krad. The maximum value recorded was below 50pA of combined input current for all 12 inputs.

Conclusions:
Specifications were easily met by the test devices irrespective of the irradiation bias conditions.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") for two representative DACs of each device is given in table 7.2.2.

Table 7.2.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV. (1 LSB = 4.9mV)
(n.e.: not evaluated)

Sipex 7584C #1 DAC A

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	-0.5	-0.5	+0.2	+0.3	+0.1	-0.7
endpoint	+1.6	+1.7	+3.0	+3.5	+4.3	+4.5
Gain	+2.1	+1.2	+2.8	+3.2	+4.2	+5.2

Sipex 7584C #1 DAC C

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	n.e.	n.e.	n.e.	-0.3	-0.5	-1.1
endpoint	n.e.	n.e.	n.e.	+11.6	+17.0	+24.5
Gain	n.e.	n.e.	n.e.	+11.9	+17.5	+25.6

Sipex 7584C #2 DAC A

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	n.e.	+0.3	-0.3	+0.1	+0.1	+1.0
endpoint	n.e.	+0.3	-0.6	-2.0	-5.4	-13.2
Gain	n.e.	0.0	-0.3	-2.1	-5.5	-14.2

Sipex 7584C #2 DAC D

dose	5 krad	10 krad	20 krad	30 krad	50 krad	80 krad
startpoint	-0.1	n.e.	-0.7	-1.0	-0.4	+0.2
endpoint	+1.0	n.e.	+0.6	-0.6	-4.1	-12.3
Gain	+1.1	n.e.	+1.3	+0.4	-3.7	-12.5

The evolution of INL and DNL can best be seen by a graphics plot of these parameters; numerical values are given in Table 7.2.3.

Table 7.2.3: Numerical values of INL and DNL for Sipex 7584 #1 and #2. Values are in mV. (n.e.: not evaluated)

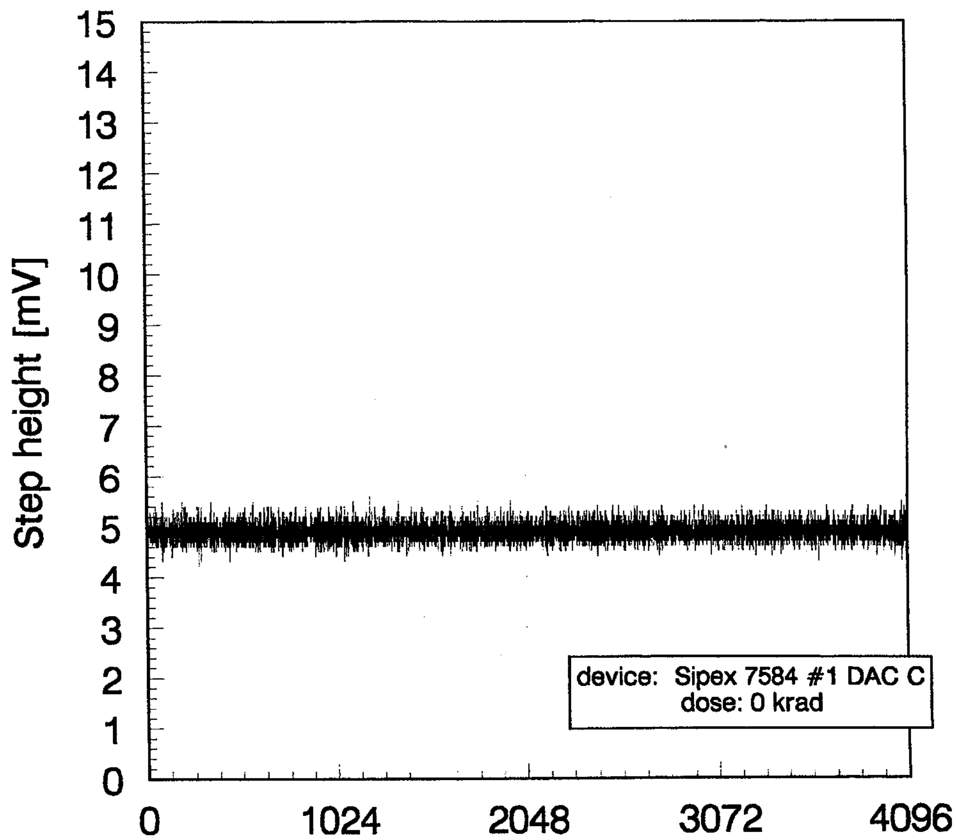
Differential nonlinearity

	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
#1 DAC A	0.8	0.9	0.9	n.e.	1.4	2.4
#1 DAC C	0.8	0.9	n.e.	2.4	4.2	7.0
#2 DAC A	1.6	0.9	0.9	1.0	1.3	3.0
#2 DAC D	1.0	n.e.	1.2	1.4	1.4	2.5

Integral nonlinearity

	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
#1 DAC A	3.5	3.3	3.2	3.1	3.1	4.0
#1 DAC C	3.7	3.9	n.e.	5.2	6.8	9.3
#2 DAC A	2.2	3.0	3.0	3.2	3.8	5.0
#2 DAC D	2.8	n.e.	2.5	2.7	3.1	3.9

Differential nonlinearity



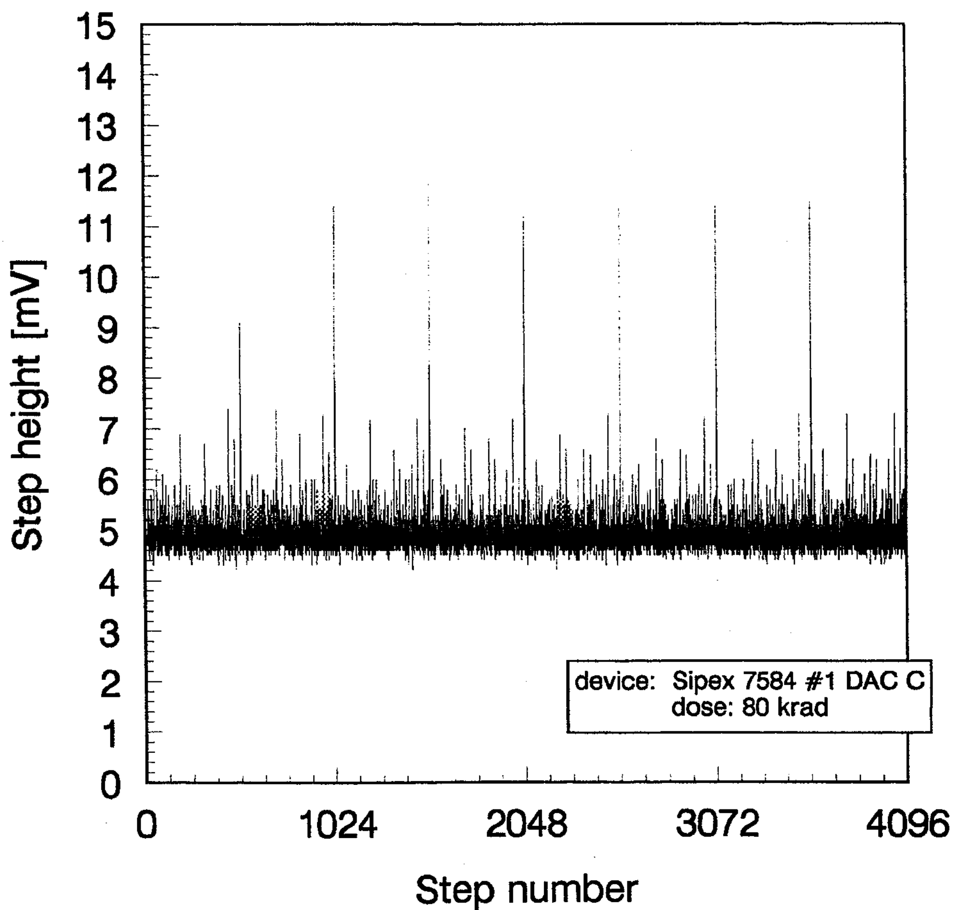


Figure 7.2.3: Evolution of DNL for device #1, DAC C. This DAC was most severely affected by the irradiation and therefore showed the biggest performance degradation.

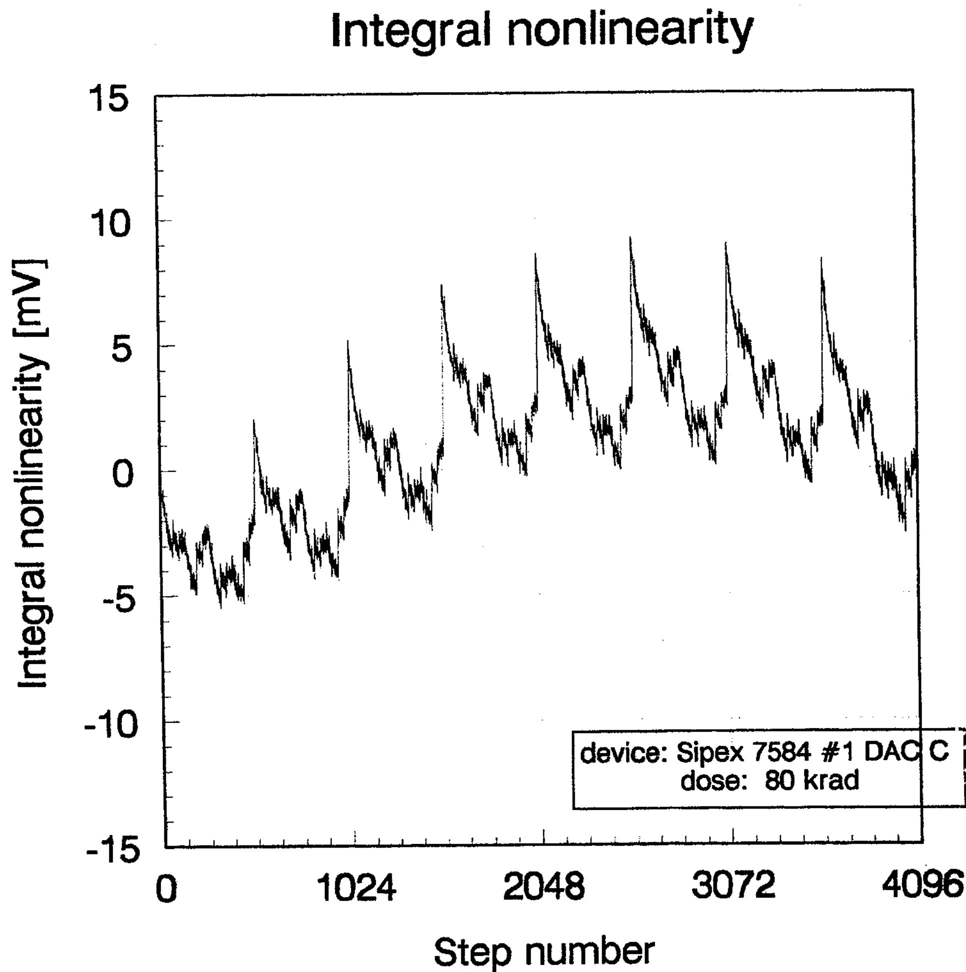


Figure 7.2.4: INL after 80 krad for DAC C of device #1. The figures recorded were the worst for all DACs of that kind.

Discussion

What the low figures for the output leakage current already suggested could be verified in these tests: The "startpoints" in output voltage hardly shifted at all, independent of the irradiation bias conditions. There was some shift in the "endpoint" value, though. No clear direction was observable, endpoints moved to lower as well as to higher values. As explained before, such a shift can only be attributed to a change of the values of the internal resistors forming the R-2R ladder and the feedback resistor. This would also be consistent with the observed decrease in total output current (see chapter "Output leakage current").
A decrease in this current without any changes of resistor values would cause

1) a decrease in output voltage value and
2) this decrease would amount to some 50 - 85mV for the present current figures

The degradation in INL and DNL which can be seen graphically in Figures 7.2.3 - 7.2.6 is therefore attributed to increasing mismatches in resistor values but not to leakage of the current switches.

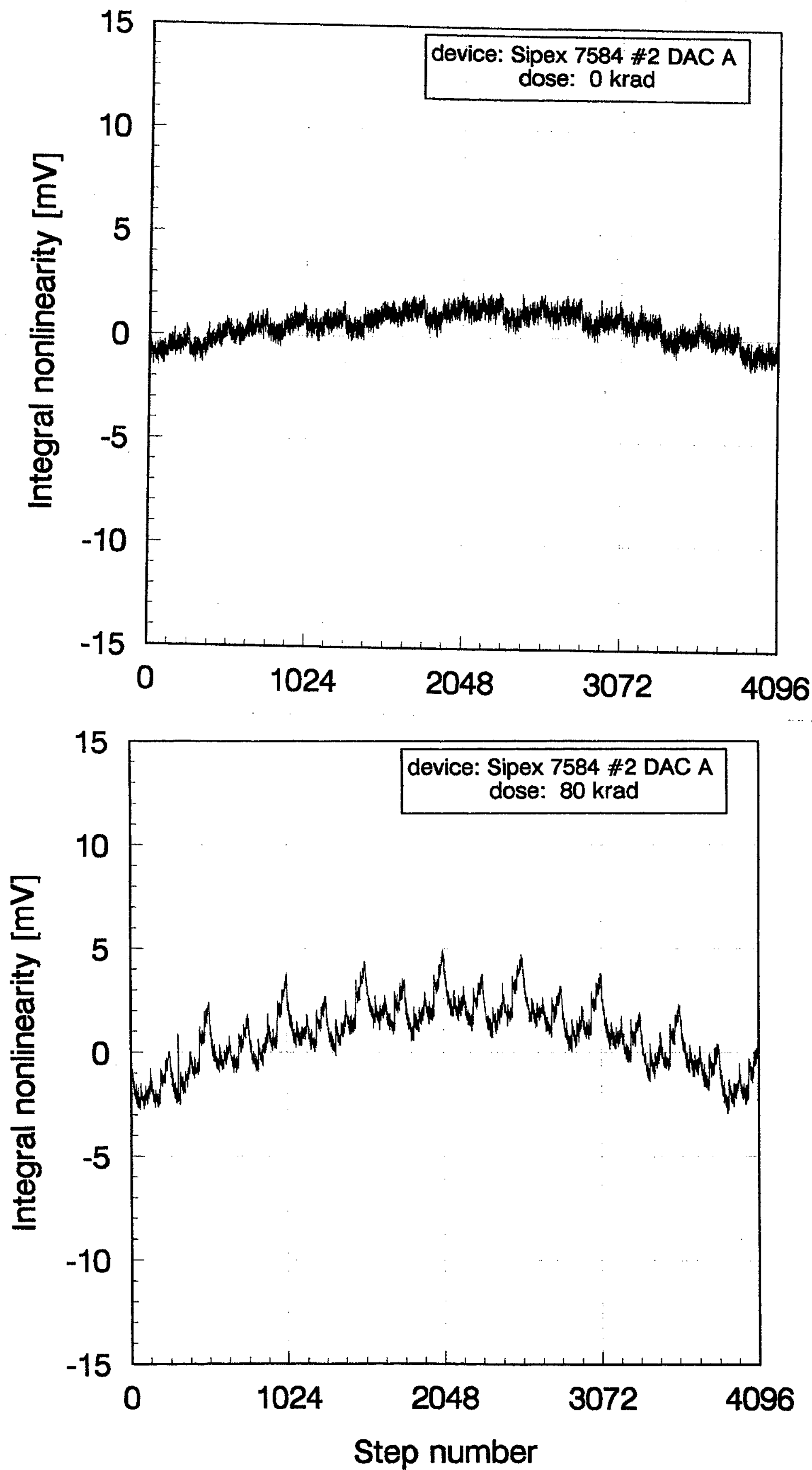


Figure 7.2.5: Evolution of integral nonlinearity with increasing total dose for device #2, DAC A. The other DACs of device #2 showed a similar behaviour.

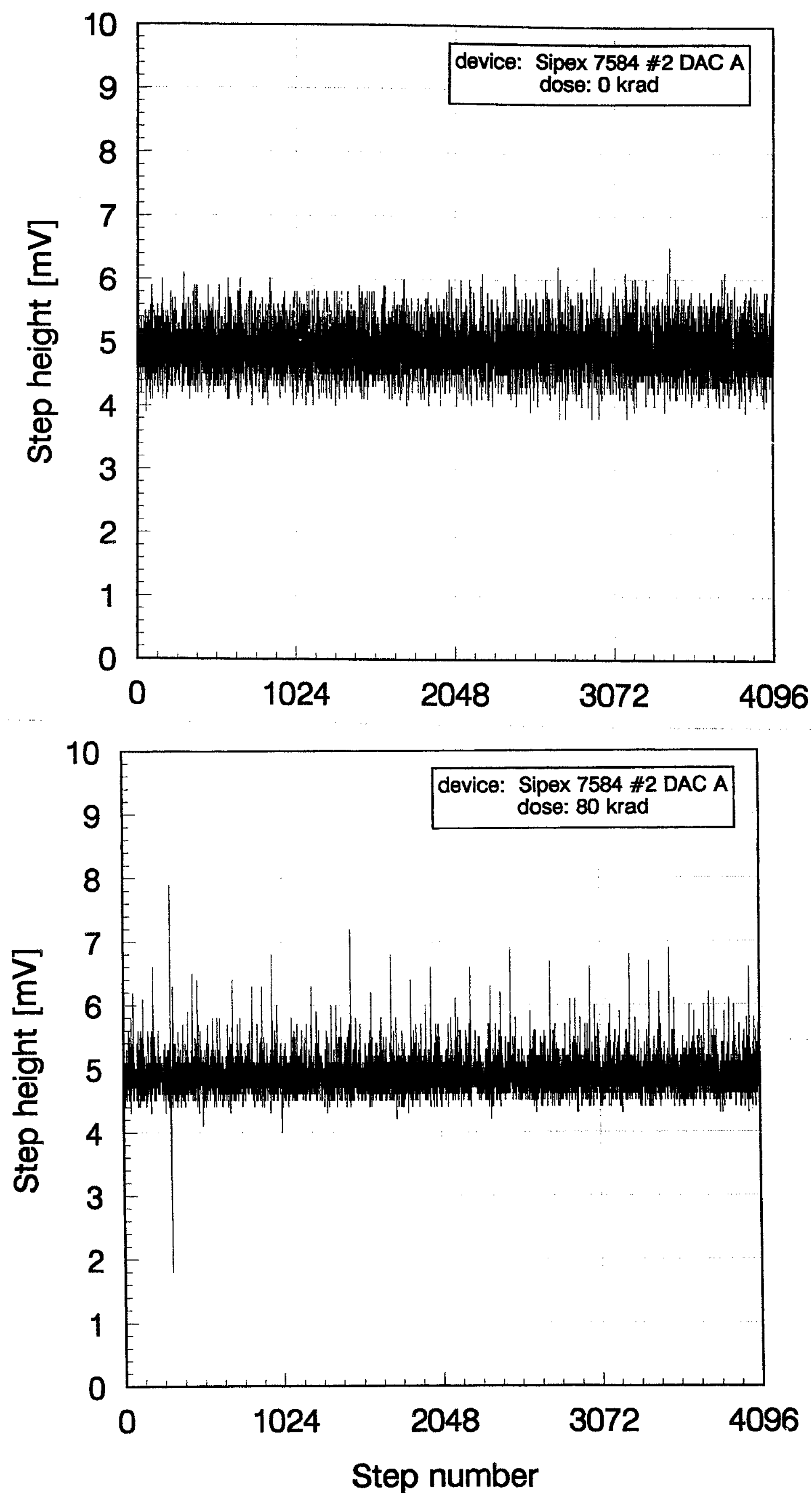


Figure 7.2.6: Evolution of differential nonlinearity with increasing total dose for device #2, DAC A. General behaviour of the other DACs was similar.

Conclusions

All 8 DACs showed little changes up to 80 krad. The performance of individual DACs was very similar with DAC C of device #1 showing the biggest changes. This DAC failed to meet the specifications on gain, INL and DNL after 30 krad, 50 krad and 80 krad, respectively. The other DACs were doing better, failing on gain figures only slightly after 80 krad and staying within tolerance ranges of the other parameters throughout the test. As the violation of the specifications was rather small (in the order of 1 LSB max.) this device might be of some interest.

Dynamic parameters

The following table shows the results obtained with the HP3653A Spectrum Analyzer; digital data was updated at a rate of 150kHz, and sinewaves of different frequencies were fed into the DAC under test (f_{in}=125Hz and 9.875kHz). It was avoided to test frequencies that are a multiple of 50Hz because of possible mains noise pickup.
The results for one representative DAC of each device are shown.

Table 7.4: Figures for THD and SNR for two different input frequencies. Numbers are in dB.

Total Harmonic Distortion

f_{in}= 125 Hz	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
7584C #1 DAC A	-73.8	-74.5	-75.0	-75.8	-75.7	-77.3
7584C #2 DAC A	-76.0	-76.4	-75.3	-75.9	-73.3	-72.9
f_{in}= 9.875 kHz						
7584C #1 DAC A	-66.3	-66.5	-66.2	-65.5	-64.9	-61.0
7584C #2 DAC A	-68.5	-68.9	-69.9	-69.6	-67.5	-55.6

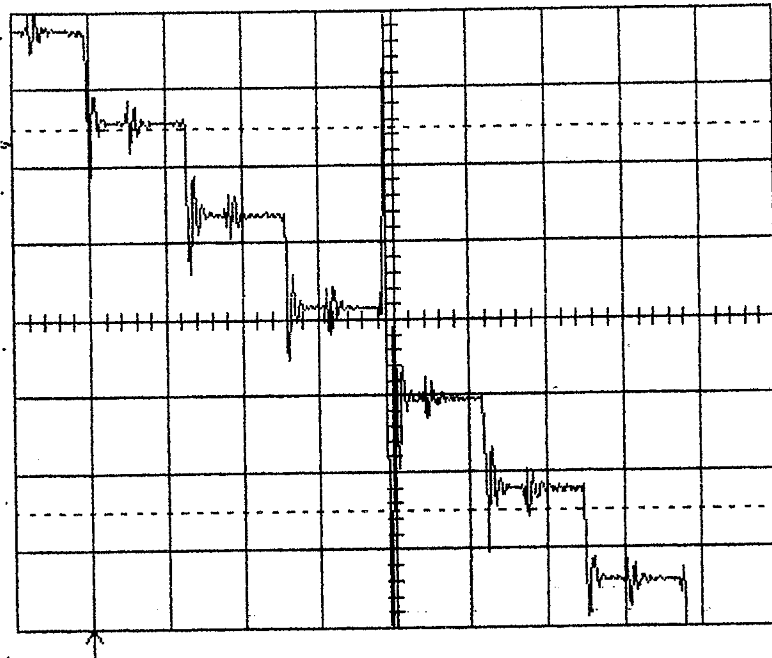
Signal/Noise Ratio

f_{in}= 125 Hz	0 krad	10 krad	20 krad	30 krad	50 krad	80 krad
7584C #1 DAC A	-67.3	-67.3	-67.4	-67.5	-67.7	-68.0
7584C #2 DAC A	-67.4	-67.6	-67.3	-67.5	-67.0	-66.9
f_{in}= 9.875 kHz						
7584C #1 DAC A	-60.4	-60.3	-60.3	-59.8	-59.2	-57.2
7584C #2 DAC A	-61.0	-61.4	-61.3	-61.5	-60.6	-53.0

Discussion

The relative big fluctuations (especially for THD and the improvement of dynamic figures at higher doses (in contrast to a small degradation in static parameters) shows that this measurement is of limited value. SNR figures seem to be a bit more reliable, especially for 125Hz.

The only striking thing that can be undoubtedly extracted is the change in figures for DAC A of device #2 between 50 and 80 krad. The reason can be seen on the oscilloscope screen (figure 7.2.8): A large "glitch" is visible at the major bit change, i.e. where the output voltage crosses zero. This indicates slower switching of at least a few switches. A similar behaviour can be noticed for DAC A of device #1 (figure 7.2.7). Here the difference in THD and SNR figures is smaller because this DAC showed a quite large "glitch" even prior to irradiation which became somewhat worse after 80 krad.



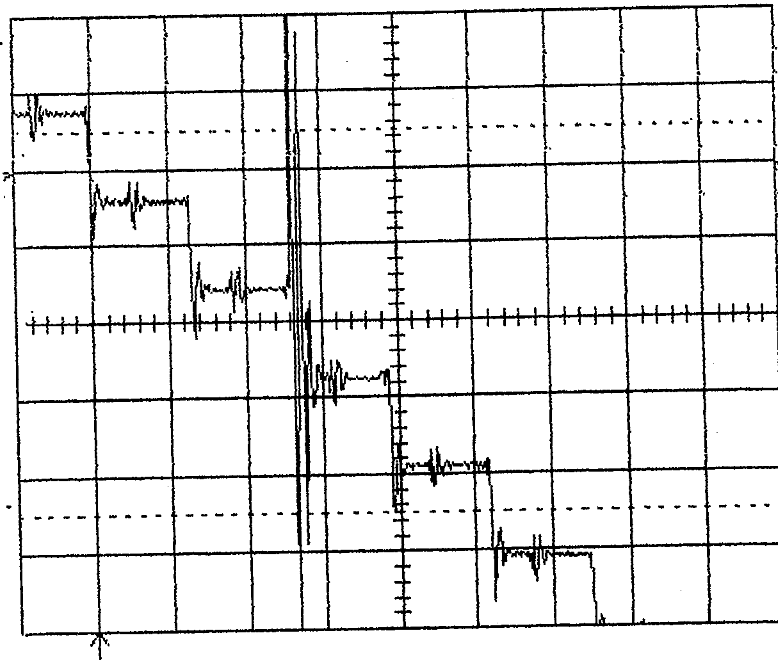
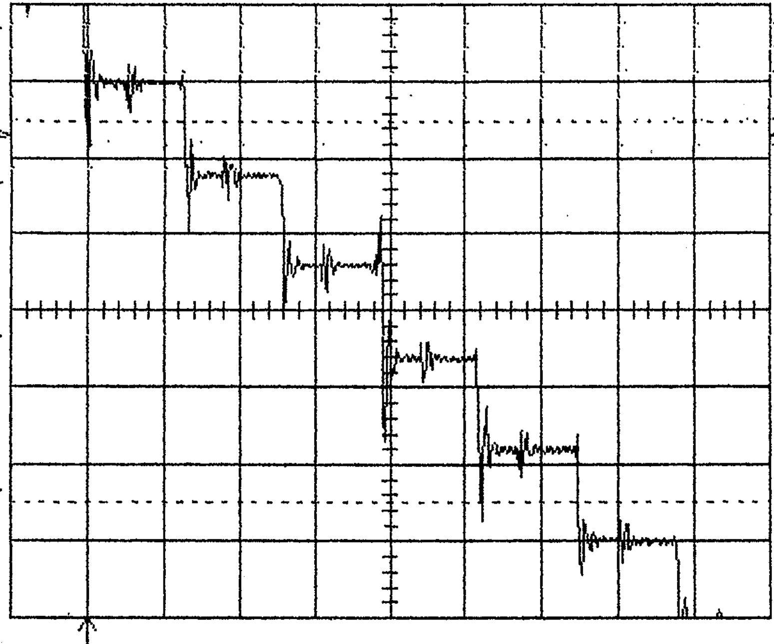


Figure 7.2.7: Hardcopy of the output signal of device #1 as seen on the oscilloscope. Digital inputs were updated at a rate of 150kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). The top picture shows the signal prior to irradiation; note the "glitch" at zero crossing. No change in shape occurred up to 50 krad. After 80 krad the "glitch" was more pronounced (bottom picture). This indicates that at least one current switch showed slower switching speed.



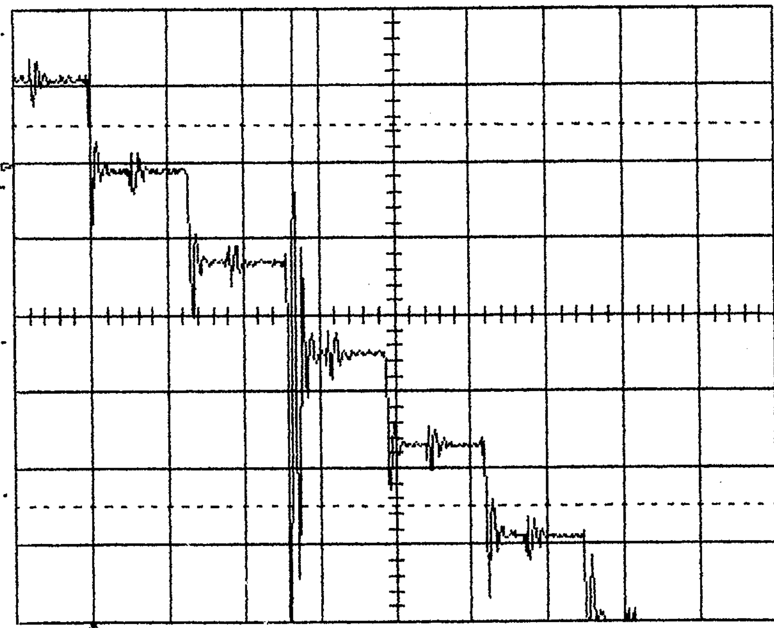


Figure 7.2.8: Same data as in Figure 7.2.7 for device #2. Here the shape of the initial output signal showed almost no glich up to 30 krad (top). After 80 krad a large glitch appeared, indicating slower switching of some switches (bottom).

7.3 ANALOG DEVICES 7845 BD

Brief characterisation: voltage output DAC with input latches and control logic. No internal voltage reference, but including an OP-AMP.

Specifications (according to datasheet):

Integral nonlinearity	max.	+/- 1 LSB
Differential nonlinearity	max.	+/- 1 LSB
Gain error	max.	+/- 3 LSB (*)
Digital input current	max.	+/- 1uA
Positive power supply current	max.	10mA (**)
Negative power supply current	max.	4mA (**)
output voltage settling time	max.	5us (***)

(*) when using internal feedback resistor
(**) V_{out} unloaded
(***) to 0.01% of full scale; load resistor 2k .

General remarks
Table 6.2 shows that 2 devices were irradiated; device #1 (dynamic irradiation bias) up to 20 krad, device #3 (static digital inputs) up to 15 krad. At these doses they had degraded so much that the tests were stopped.These figures are different because due to a technical problem devices #3 was only included in the test after the other devices of the test run had already been subjected to a total irradiation dose of 5 krad.
No analysis as detailed as for current output DACs is possible because the lack of a leakage current measurement eliminated one valueable source of information.

Pre-irradiation characteristics
Both devices exhibited outstanding INL and DNL figures. Electrical specifications and settling time were well within specifications.

Electrical parameters and quasistatic test results

Input current

The evolution of positive supply current figures shows the characteristic shift in threshold voltage for n-MOSFETs. Figure 7.3.1 shows that the current peak moves to ever lower voltages as the total dose increases.

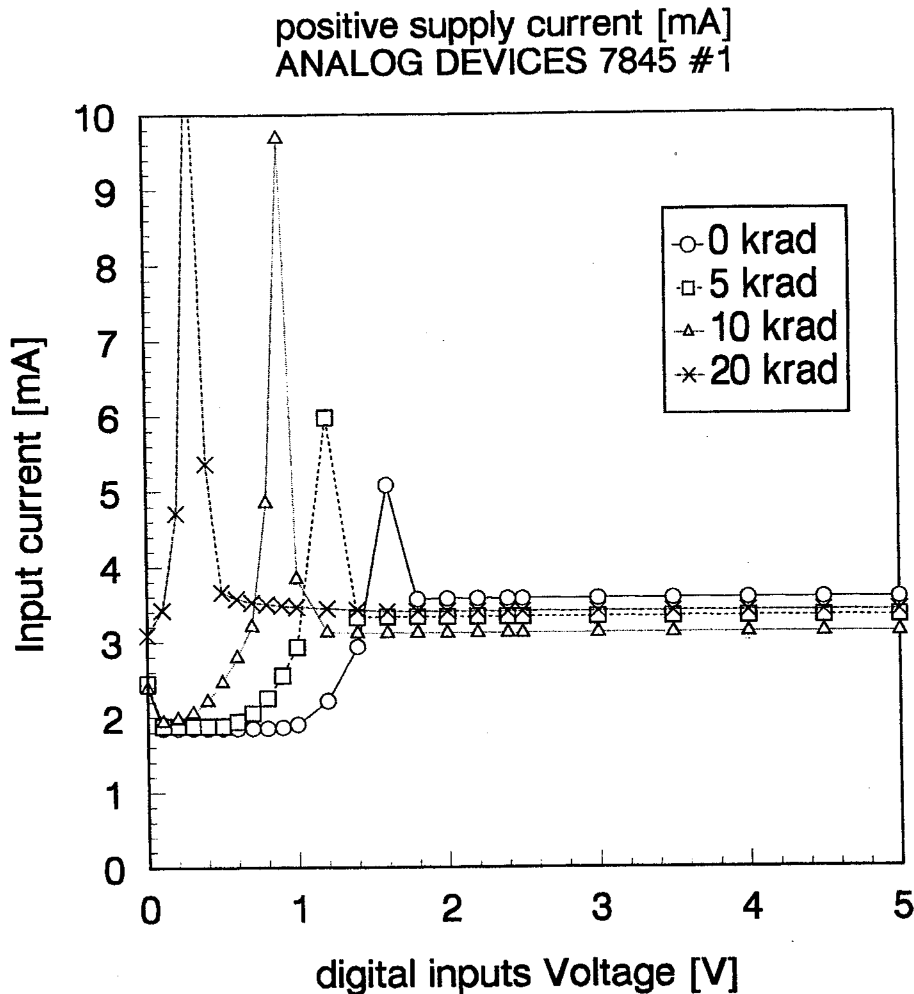


Figure 7.1: Input current vs. digital input voltage for Analog Devices 7845 #1 at different irradiation stages. Note the pronounced shift in the position of the current peak; no increased leakage was noticed for the "flat" parts of the curves (e.g. above 2V).

Device #2 which had been kept under static bias conditions surprisingly showed smaller effects. So the current peak was located at 0.95V after 15 krad, compared to 0.9V after 10 krad for device #1. The general direction was the same, though.
For both devices the "flat" parts of the curve (e.g. above 2V) did not show any increase in leakage; the absoute current value even dropped a bit.

Negative input currents did not display a sharp current peak but were rather independent of the input voltage; again the general tendency was towards a slight decrease in magnitude with increasing total dose.

Discussion

Although device #1 was not functionally destroyed after 20 krad figure 7.3.1 indicates that this point is not too far away. One has to remember that the current peak position approximately coincides with the change in logic state of latches; some 5 krad of irradiation will be sufficient to shift this position below 0V. This means complete logic failure.
As a valid logic "LOW" extends up to 0.8V, a correct performance is not guaranteed as soon as the peak position shifts below that value.
It can be safely assumed that trapped positive charge in the gate oxide is responsible for the large shifts in threshold voltage; leakage caused by poor field oxide quality seems to be a minor problem.

Conclusions

Although the specification value of 10mA was not violated it is obvious from figure 7.3.1 that correct logic levels can only been expected up to 10 krad for device #1 and up to some 15 krad for device #2.

Digital input current

No changes in digital input currents were observed up to 20 krad.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.3.1.

Table 7.3.1: **Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV. (n.e.: not evaluated)**

Analog Devices 7845 #1

dose	5 krad	10 krad	15 krad	20 krad
startpoint	n.e.	-0.2	n.e.	+494.4
endpoint	n.e.	-1.3	n.e.	-284.0
Gain	n.e.	-1.1	n.e.	-778.4

Analog Devices 7845 #3

dose	5 krad	10 krad	15 krad	20 krad
startpoint	+0.4	n.e.	+0.4	n.e.
endpoint	-5.0	n.e.	-286.0	n.e.
Gain	-5.4	n.e.	-286.6	n.e.

Numerical values for INL and DNL are given in Table 7.3.2.

Table 7.3.2: Numerical values of INL and DNL for device #1 and #2. Values are in mV. (n.e.: not evaluated)

Differential nonlinearity

	0 krad	5 krad	10 krad	15 krad	20 krad
7845 #1	1.0	n.e.	1.6	n.e.	43.1
7845 #2	0.9	1.2	n.e.	7.7	n.e.

Integral nonlinearity

	0 krad	5 krad	10 krad	15 krad	20 krad
7845 #1	1.1	n.e.	1.1	n.e.	45.3
7845 #2	1.3	1.6	n.e.	9.6	n.e.

Discussion

Gain figures behave in the same way as for the Burr Brown 7802: In case of "dynamic" digital inputs during irradiation the startpoint and endpoint shift at about the same rate; when digital inputs are kept static, then the startpoint showed almost no shift after 15 krad while the endpoint had already shifted further than it had for device #1 after 20 krad.
Only an output voltage could be observed as the devices had a built-in OP-AMP; nevertheless it seems to be possible to find some striking similarities to the Burr Brown 7802 which indicate identical failure mechanisms. Looking at the results for device #3 it is clear that one current switch transistor (cf. Figure 2.3) was affected to a much greater extent than the other because its gate was biased during irradiation. This transistor suffered a much greater threshold voltage shift and showed a significant leakage current (because its threshold voltage was alredy close to 0V) while the other one was still fully functional. In case of dynamic bias both transistors were affected equally.

The OP-AMP seemingly does not show deterioriation: the output voltage stays the same as long as the current switches can be fully closed and openend. However, this cannot be verified because more error sources are possible which might partially cancel.

INL and DNL figures show that different bits are affected slightly differently; on the other hand device #3 showed a DNL figure of 7.7mV when the total change in gain was already 286mV which is an indication of surprisingly uniform degradation.

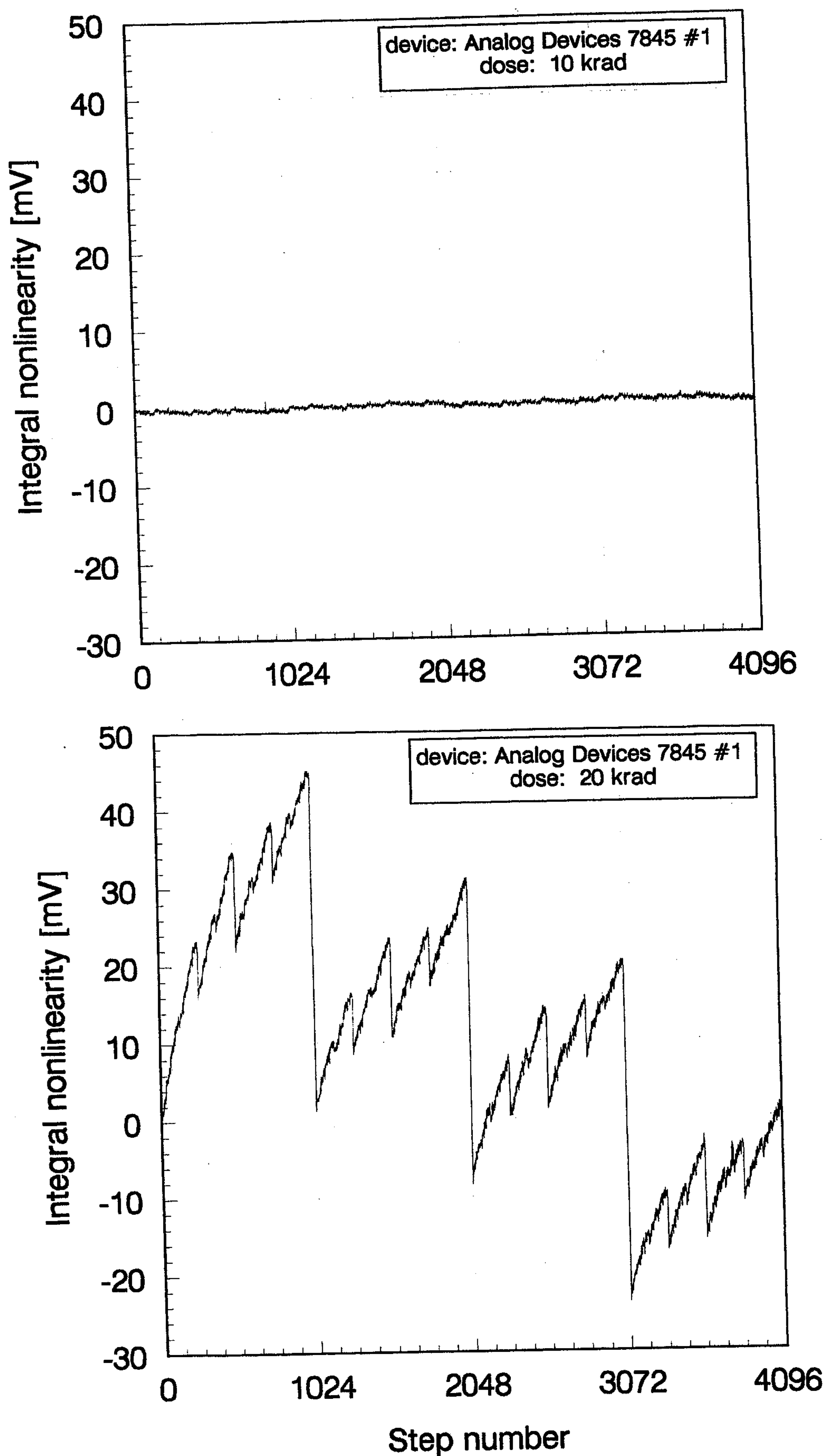


Figure 7.3.2: Evolution of INL of device #1 in response to irradiation. Top figure is after 10 krad and does not show any changes compared to 0 krad; bottom picture is after 20 krad.

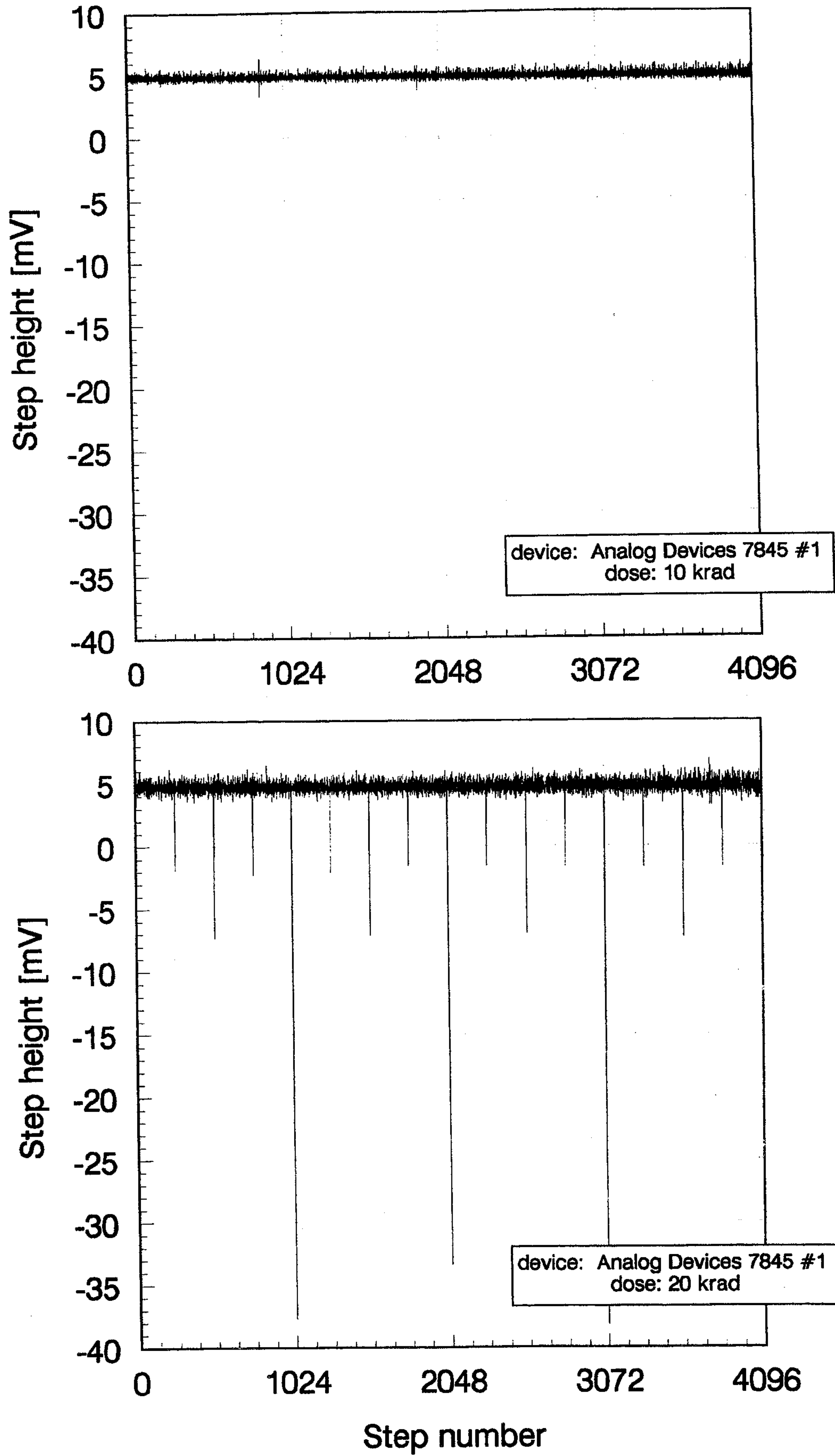
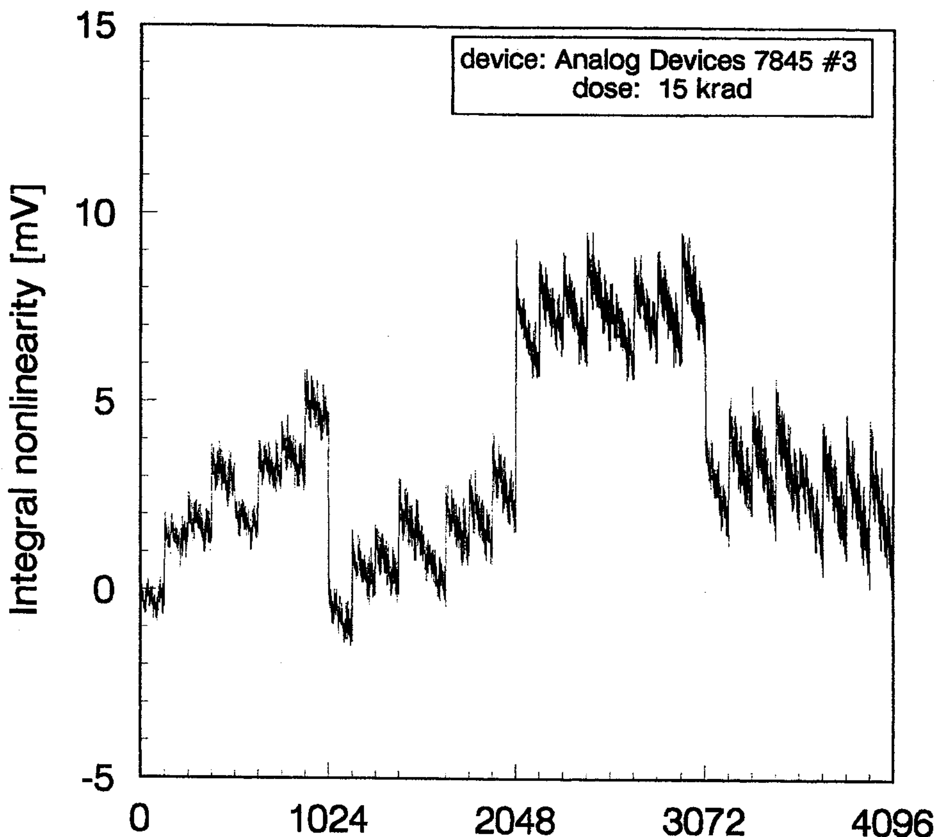


Figure 7.3.3: Evolution of differential nonlinearity with increasing total dose for device #1. After 10 krad no changes had yet taken place.



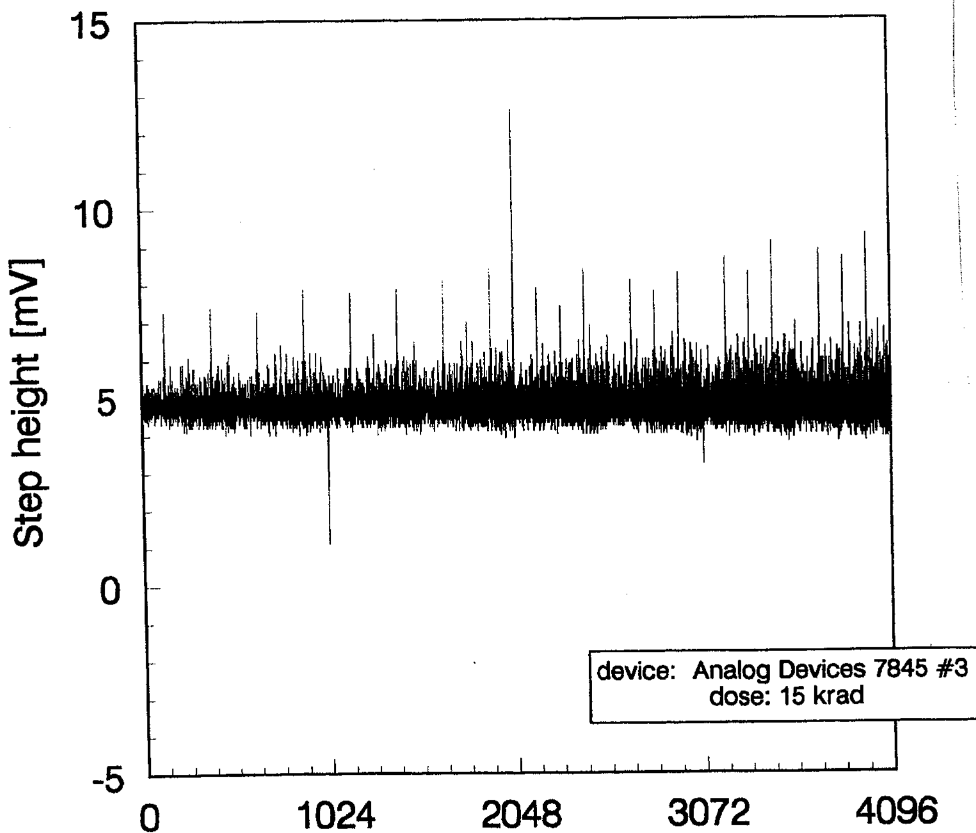


Figure 7.3.4: figures for INL and DNL for device #3 (static bias conditions) after 15 krad. Specifications are not fulfilled any more.

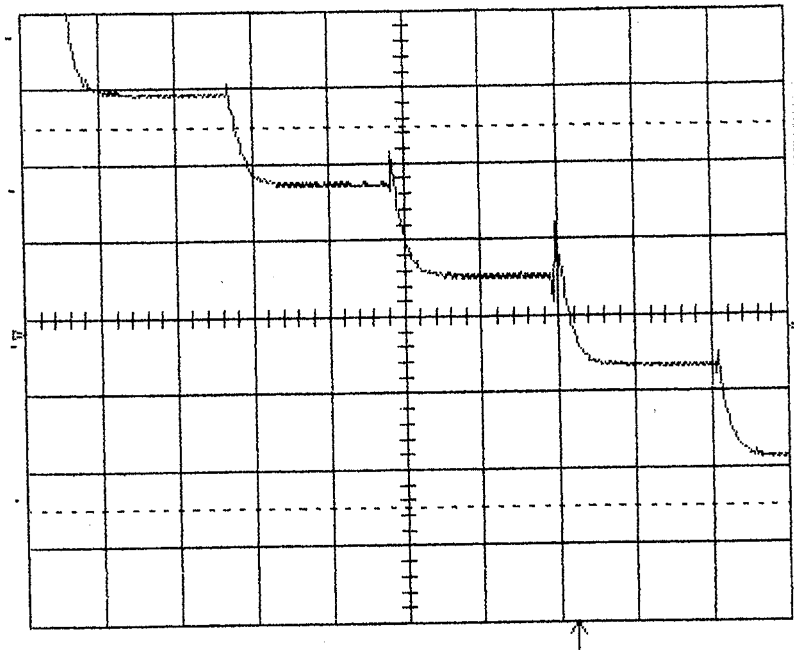
Conclusions
Both devices failed on gain specifications after 12 - 14 krad. Device #1 was still fully functional and within specifications after 10 krad; because of no measurement point was recorded at that dose this cannot be said with certainty of device #2, which was certainly out of gain, INL and DNL specifications after 15 krad.

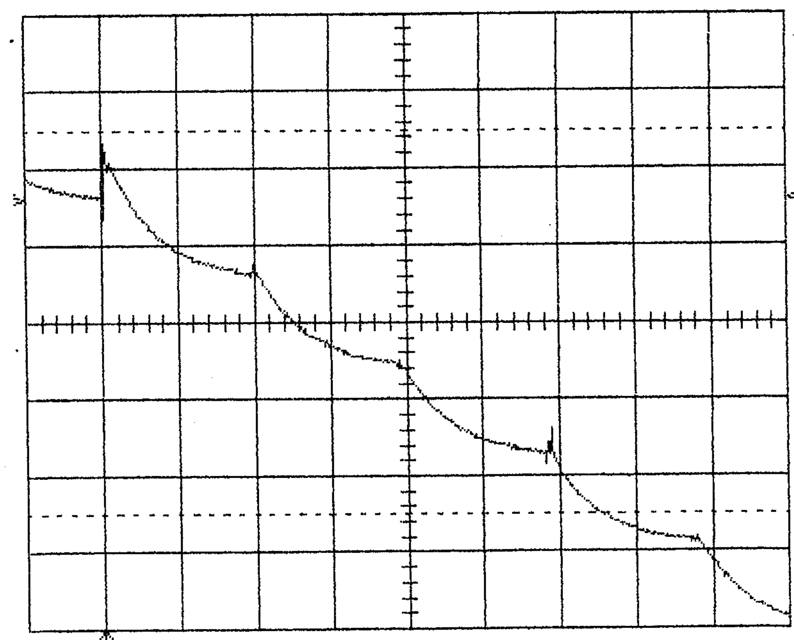
Dynamic parameters

Remark: because of the slower settling time of this device the digital data update rate was reduced to 100kHz

THD and SNR figures had not changed after 10 krad and 5 krad for device #1 and #3, respectively. The changes that were observable after 20 krad and 15 krad are so obvious that the oscilloscope pictures can give the best impression (Figures 7.3.5 and 7.3.6 on next pages).

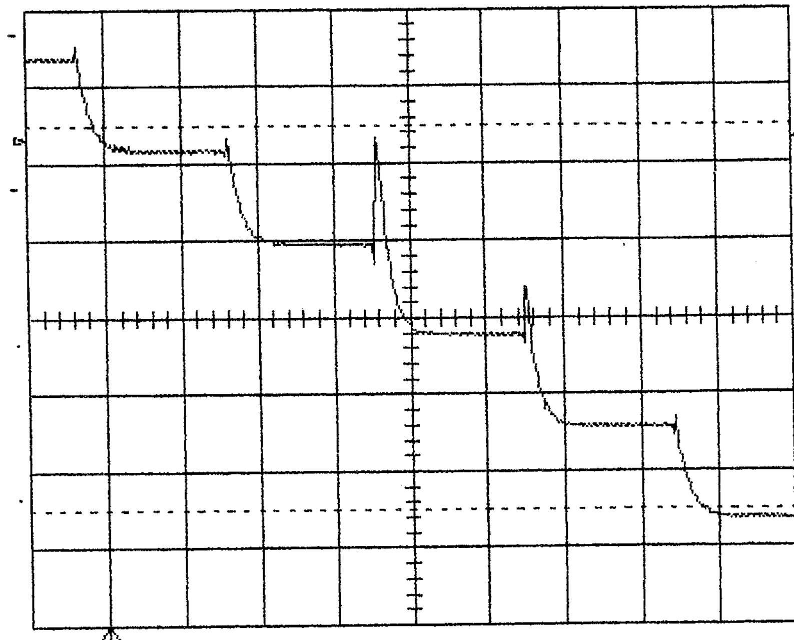
Conclusion
Dynamic parameters are affected very strongly by radiation. However, it seems as if this is only felt at the same time or even after severe degradations in static performance could be detected.

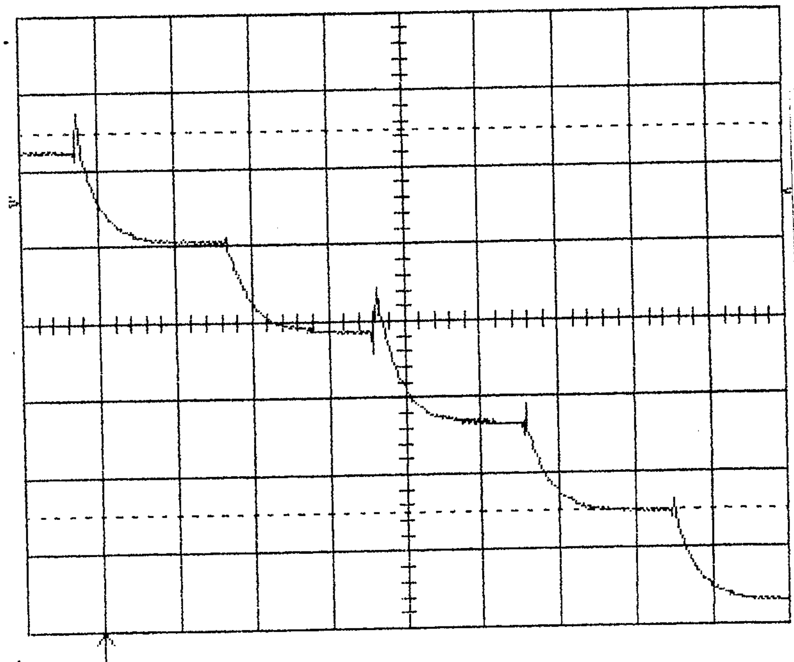




T/div 5μs

Figure 7.3.5: Hardcopy of the output signal of device #1 as seen on the oscilloscope. Digital inputs were updated at a rate of 150kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). The top picture shows the signal prior to irradiation. After 20 krad, however, the signal did not settle to its final value before the digital inputs were updated (bottom picture).





T/div 5μs

Figure 7.3.6: Same data as in Figure 7.12, for device #3. Pre-irradiation signal can be seen in the top picture. After 15 krad the settling time was considerably slower (bottom).

7.4 SIPEX DAC356LPC-12

Brief characterisation: complete voltage output DAC with voltage reference and OP-AMP. No input latches and control logic.

Specifications (according to datasheet):

Integral nonlinearity	max.	+/- 0.5 LSB
Differential nonlinearity	max.	+/- 1 LSB
End point accuracy	max.	+/- 0.1% FSR
Digital input current	max.	+/- 1uA
Positive supply current	max.	3.0mA
Negative supply current	max.	3.0mA
Output voltage settling time	max.	50us (*)

(*) for full scale step; to 0.02% of full scale range

General remarks

Table 6.1 shows that 2 devices were irradiated; device #1 (dynamic irradiation bias) up to 100 krad, device #3 (static digital inputs) up to 12 krad. At these doses they had degraded so much that the tests were stopped. Due to the small number of samples it is not sure if this is a result of different irradiation bias or if there was a flaw in device #3. Their initial performance was almost identical.

No analysis as detailed as for current output DACs is possible because the lack of a leakage current measurement eliminated one valuable source of information.

The internal voltage reference is even one more possible error source. But as a zener diode is rather insensitive to radiation (at least for total doses of the order of 100krad) all that might happen is a small deviation from its nominal value which is negligible compared to other changes.

Pre-irradiation characteristics

For both devices it was found that the negative supply current was more than 2 times as high as allowed by the specifications. This was also found for two other test devices which had served as "guinea pigs" to estimate the rate of degradation.

Integral nonlinearity values were also nonconformal to the specifications: it exceeded 1 LSB for both devices.

The other parameters were in agreement with the specification limits.

Electrical parameters and quasistatic test results

Input current

For these devices no pronounced input current peak was present. Instead both positive and negative supply current remained almost constant when the input voltage at the shorted digital input pins was swept from 0V to 10V. This is somewhat surprising because at higher total doses the point where the output voltage switched from full positive to full negative value was clearly detectable and it shifted to lower values in the course of irradiation.
For device #3 which failed after 12 krad an increase in positive supply current was observed: It rose from the initial value of 2.8mA to 5.6mA after 12 krad for an input voltage of 0.1V. The current did not change for input voltages of more than 2.5V.

Conclusions

No information could be extracted because the characteristic current peak indicating the change in logic state of inverters was missing. Nevertheless a shift of the point where the output voltage changed from positive to negative values was observed. For device #1 this point went down to 0.7V after 100 krad; for device #3 it had already shifted to 0.4V after 8 krad and reached 0.1V after 12 krad. One reason for the increased sensitivity of device #3 should be found in the different bias conditions. On the other hand a discrepancy as big as between these two devices is not understandable.
Even prior to irradiation the negative input current was far exceeding the limit given in the specifications. However, no further increase was noticed during testing.

Digital input current

Observations

Digital input currents were in the order of a few picoamperes at test start. In the course of testing they increased steadily up to about 1nA for device #1 after 100 krad.
For device #2 they reached about 100pA after 12 krad, the same value as for device #1.
This means that no violation of the specifications could be detected.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.4.1.

Table 7.4.1: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV. (ann.: after annealing for 30 days at room temperature; n.e.: not evaluated)

Sipex DAC356 #1

dose [krad]	4	8	12	16	25	40	70	100	ann.
startpoint	+1.2	+7.2	+6.8	+6.3	+6.8	+6.2	+4.7	+2.9	-5.6
endpoint	-3.8	-10.5	-12.6	-14.6	-18.3	-24.4	-33.9	-45.2	-37.4
Gain	-5.0	-17.7	-19.4	-20.9	-25.1	-30.6	-38.6	-48.1	-31.8

Sipex DAC356 #3

dose [krad]	4	8	12	ann.
startpoint	+4.7	+17.4	n.f.	+7.8
endpoint	-6.6	-8.2	n.f.	-1.0
Gain	-11.3	-25.6	n.f.	-8.8

Numerical values for INL and DNL are given in Table 7.4.2.

Table 7.4.2: Numerical values of INL and DNL for device #1 and #3. Values are in mV. (n.e.: not evaluated; n.f: not functional any more; ann.: after annealing at room temperature for 30 days)

Differential nonlinearity

dose [krad]	0	4	8	12	16	25	40	70	100	ann.
DAC356 #1	1.1	n.e.	1.9	2.7	3.2	4.7	6.4	10.8	15.2	14.7
DAC356 #3	1.3	2.2	5.4	n.f.	-	-	-	-	-	5.0

Integral nonlinearity

dose [krad]	0	4	8	12	16	25	40	70	100	ann.
DAC356 #1	6.6	6.2	7.0	7.0	7.2	8.2	9.0	11.3	13.3	13.2
DAC356 #3	5.5	5.8	12.0	n.f.	-	-	-	-	-	11.3

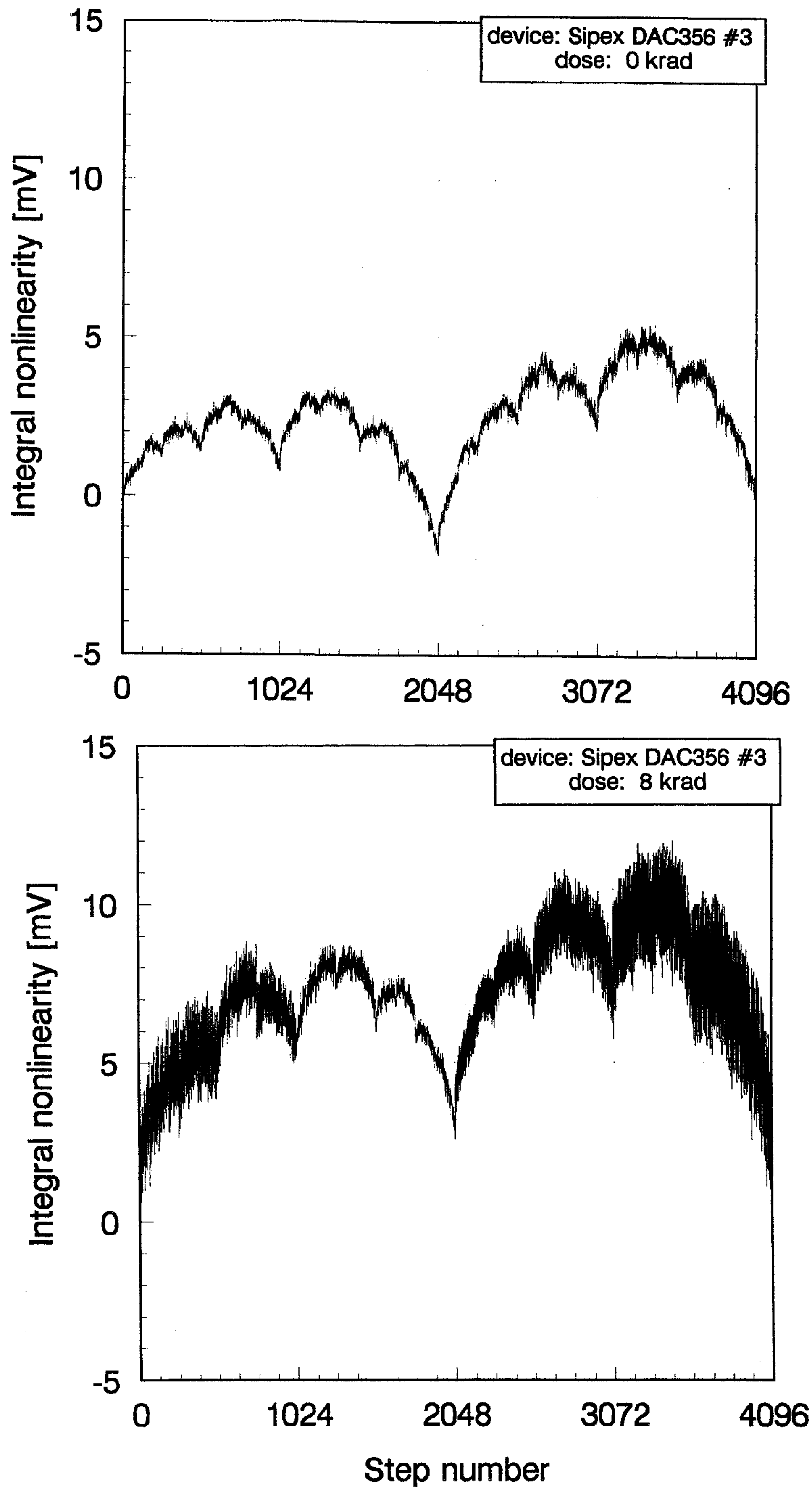


Figure 7.4.1: Evolution of INL of device #3 in response to irradiation. Top figure shows characteristics before irradiation; the device is already outside the specifications. A very similar behaviour was found for device #1. Both devices showed very small DNL figures, though. Bottom picture is after 8 krad. Although there is some deterioriation it was a surprise when this device showed complete failure after 12 krad.

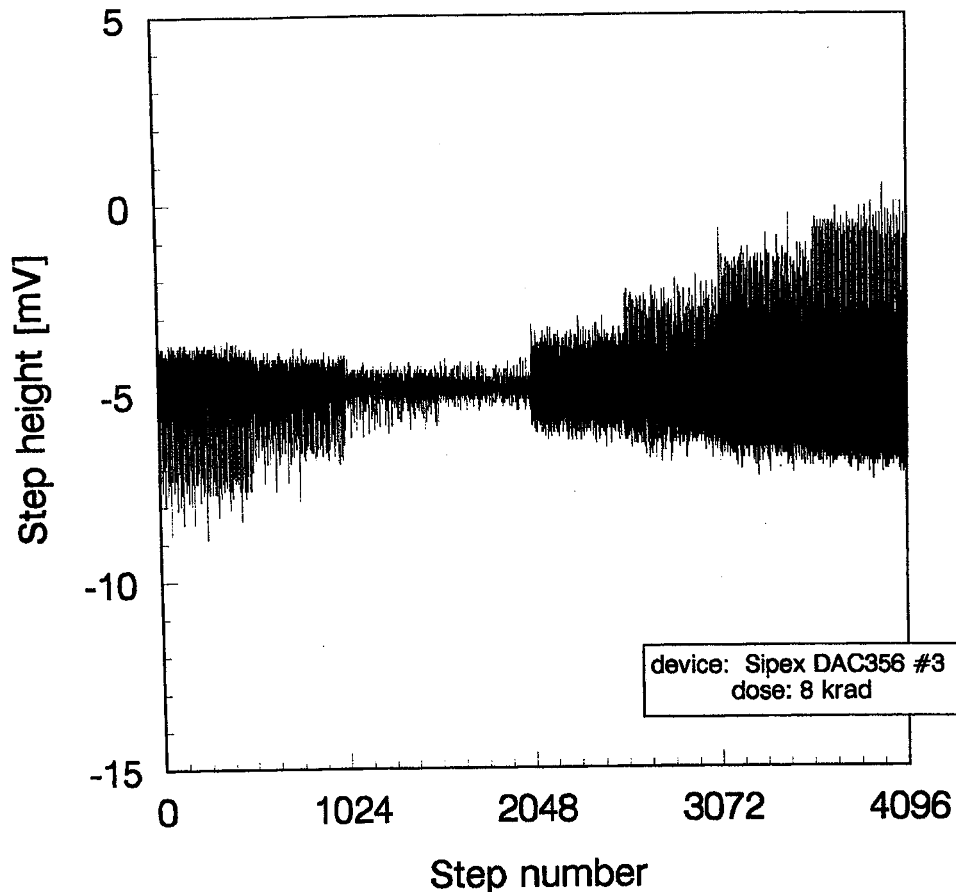
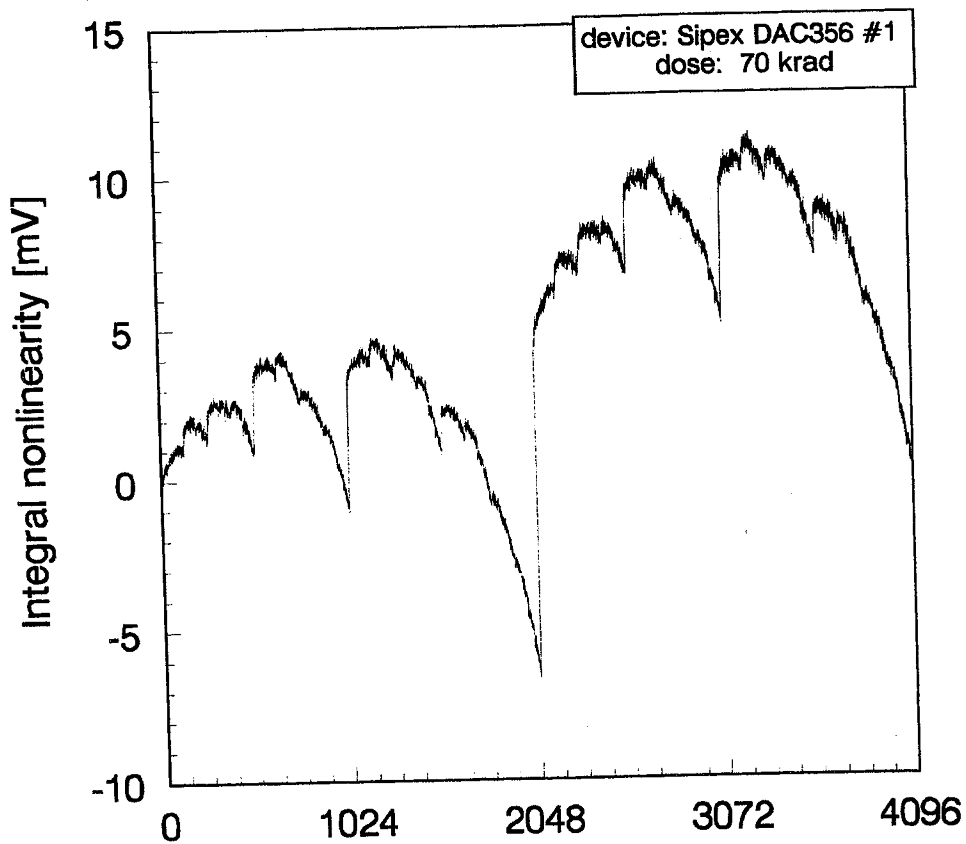


Figure 7.4.2: Differential nonlinearity for device #3 after 8 krad. This behaviour was unique because it shows a code-dependent DNL. As the digital input codes from 0 - 1023 and from 1024 - 2047 are basically identical with the exception of bit 10 which is '0' for the first cast and '1' for the second this is very strange and no explanation has been found which accounts for the observed characteristics.

Discussion

Because of the confusing difference in performance between device #1 and #3 no information as to the failure mechanisms could be extracted. There was some difference in the development of gain figures for "static" and "dynamic" irradiation bias, but it was not as conclusive as for most other devices. The complete functional failure of device #3 after only 12 krad might be a result of a threshold voltage shift. This is supported by the fact that after annealing for 30 days the device came back to life again (The trapped positive charge in the gate oxide can slowly be detrapped, resulting in an increase in threshold voltage). But the fact that nothing comparable happened to device #1 even after 100 krad might indicate that there was a difference in quality between both devices right from the start.



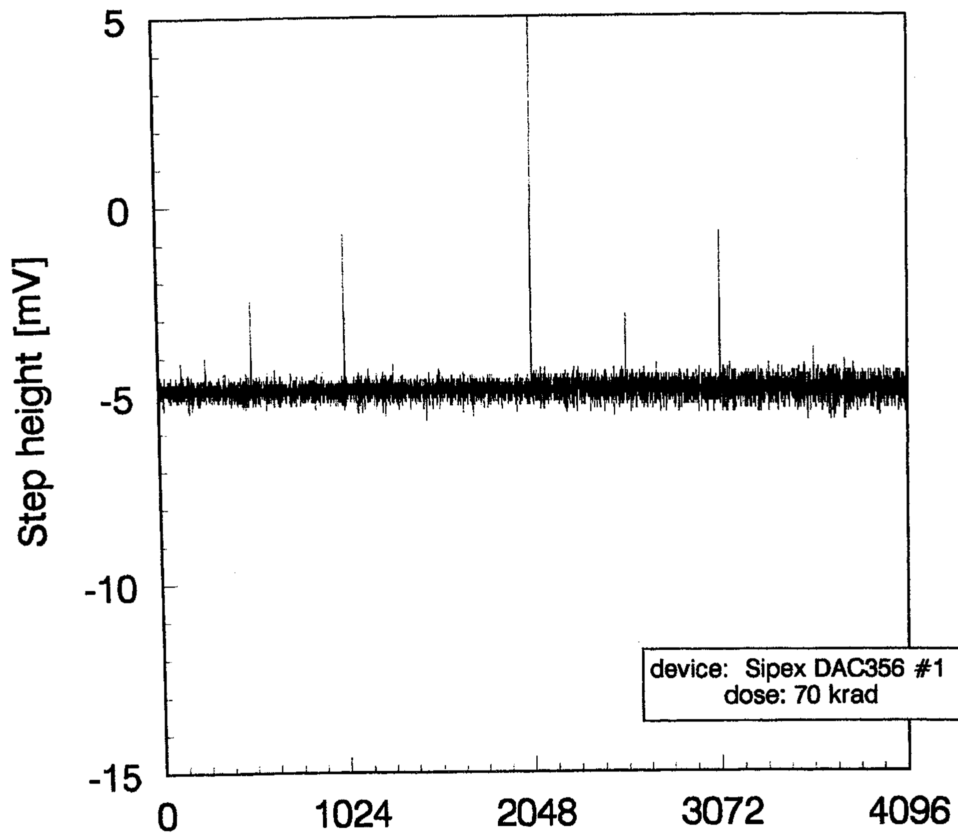


Figure 7.4.3: figures for INL and DNL for device #1 (dynamic bias conditions) after 70 krad. Although the figures became worse during irradiation, the deterioriation is not dramatical. There is one nonmonotonic step at the major bitchange, and INL figures increased from about 1 LSB to 2 LSB.

Conclusions
Both devices did not meet the specification requirement for INL even before irradiation.
Device #1 showed some degradation and failed on DNL after 30 krad and on gain figures after about 16 krad. Degradation was not too bad, though, and it was still functional after 100 krad.
Device #3 showed complete functional failure after 12 krad. Even after 8 krad it was out of INL, DNL and gain specification figures.

Dynamic parameters

Remark: because of the slower settling time of this device the data update rate was reduced to 25kHz

Dynamic figures for device #1 showed a small deterioration in THD and SNR; in absolute terms this amounted to an increase for both parameters of approximately 3 - 5dB after 100 krad. No visible change of the oscilloscope picture could be observed.
Up to 8 krad the figures for device #3 remained constant; after 12 krad no measurement was possible any more. After annealing the device was functional again and showed its pre-irradiation figures.

Conclusion
Dynamic parameters seem to be only slightly affected by radiation.

7.5 BURR BROWN 7541A KP

General remarks
The story of this device is quickly told: after some preliminary tests indicating that it was very quickly damaged by irradiation this finding was confirmed in the "real" test. Only one device was irradiated and its digital inputs were "dynamic" which should give more favourable results than static irradiation bias. Nevertheless it was removed from the test after only 8 krad because of severe degradation.

Brief characterisation: multiplying current output DAC without input latches. No internal voltage reference or OP-AMP ("basic DAC").

N.B.: The following specifications for an 7541A were more almost identical for all manufacturers and will only be specified here.

Specifications (according to datasheet):
(at 25°C for $V_{dd}=+15V$, $V_{ref}=+10V$)

Parameter		Value
Integral nonlinearity	max.	+/- 0.5 LSB
Differential nonlinearity	max.	+/- 0.5 LSB
Gain error	max.	+/- 3 LSB (*)
Output leakage current	max.	10 nA (**)
Digital input current	max.	+/- 1uA
Power supply current	max.	2mA
output current settling time	max.	1.0us (***)

(*) when using internal feedback resistor
(**) for both current output pins
(***) to 0.01% of full scale; load resistor 100Ω.

Pre-irradiation characteristics
Prior to irradiation all parameters were well within specifications.

Electrical parameters and quasistatic test results

Input current
The changes in the input current vs. input voltage at the digital inputs characteristics indicate both a strong shift in threshold voltage for the n-MOSFETs and after 8 krad the current increase in the "flat" region below 0.5V means that leakage becomes a major problem as well. Unfortunately the measurements were restricted to valid logic levels (0V - 0.8V and 2.4V - 5V), but the position of the current peak (which indicates the voltage where the logic states of inverters change) quickly shifts into that region.

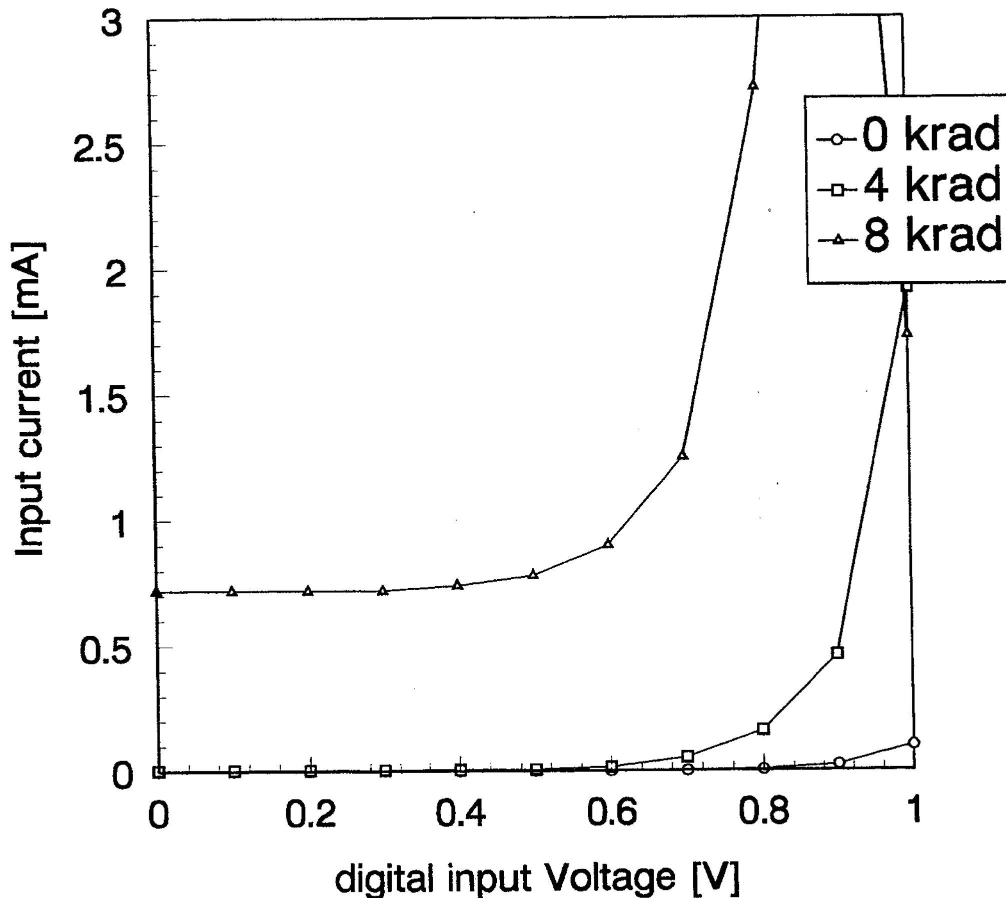


Figure 7.5.1: Input current vs. digital input voltage for several total doses for the device. For reasons of clarity the datapoints have been connected to show the shift to lower voltages. The response to radiation is both a shift in threshold voltage and strongly increased leakage in the region below 0.5V.

Discussion

One should remember to distinguish between the two effects present in this case: The shift of the current peak is most likely due to trapping of positive charge in the gate oxide of MOSFETs, leading to a lower value for the threshold voltage (the voltage where the channel of the transistor becomes conducting). Increased leakage as it is observed in the "flat" part of the curve is a result of leakage current at the borders of the MOSFETs and can most likely be attributed to poor field oxide quality.

Conclusions

Even for the case of dynamic digital inputs during irradiation the input current is larger than the specifications would allow after only 8 krad (for 0.8V applied to the digital inputs) Static irradiation bias probably leads to an even quicker degradation.

Output leakage current

Output leakage current was measured at both current output pins, for logic "LOW" at the digital inputs at output pin 1, for logic "HIGH" at output pin 2. In this way it was possible to see if any of the output current switches (cf. Figure 2.3) was damaged more than the other.

Table 7.5.1.Output leakage current for different total doses. Measurements were taken at both output current pins; input voltage at the digital inputs was 0.2V for determinig the leakage ot pin 1 and 4.5V for pin 2.

	0 krad	4 krad	8 krad
Output pin 1	1.2pA	37nA	2.99uA
Output pin 2	0.2pA	25nA	1.64uA

Observations

The leakage current increases quickly with total dose. The rate of deterioriation is about equal for both outputs; this means that both output switches are affected equally which is in agreement with the fact that irradiation bias was dynamic.

Conclusions

The device failed to comlpy with the specification at less than 4 krad; this is in agreement with findings at preliminary test with other devices of this type.

Digital input current

It increased from about 1pA at 0 krad to some 10pA after 8 krad but was still easily within specifications.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.5.1.

Table 7.5.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV.

Burr Brown 7541A #1

total dose	4 krad	8 krad
startpoint	+0.8	+31.9
endpoint	+2.5	-25.8
Gain	+1.7	-57.7

Table 7.5.3: Numerical values of INL and DNL for Burr Brown 7802 #1 and #2. Values are in mV.

Differential nonlinearity

	0 krad	4 krad	8 krad
7541A #3	1.4	4.9	16.9

Integral nonlinearity

	0 krad	4 krad	8 krad
7541A #3	1.8	4.9	18.7

Discussion

The gain figures prove that both current outputs have been equally affected: "startpoint" and "endpoint" values change at about the same rate. The small increase in endpoint value after 4 krad could mean that even the resistor values are already changing.
A very peculiar observation was made for this device as well as another Burr Brown 7541A: the least significant bit (LSB) shows the biggest relative change: changing its state does not result in a voltage step not of 4.88mV (the ideal value) but of 10mV after 8 krad.
It is also the only bit which increases in value; for all the others the output voltage step size becomes smaller than it used to be prior to irradiation. This must be the result of its design which cannot be explained easily.

Conclusions

The device was just still within specifications after 4krad; after 8 krad INL and DNL figures as well as gain were clearly violating the limits .

Dynamic parameters

The figures obtained by the HP3653A spectrum analyzer show some small degradation after 8 krad. More interesting seems to be the hardcopy of the oscilloscope screen: There is some indication that the switching speed goes down. After a new digital code is applied to the inputs "glitches" can be seen that are most pronounced at major bitchanges. But even for codes where only a few bits are changed they are easily visible. Apparently the opening and closing of the current switches does not take place simultaneously any more.

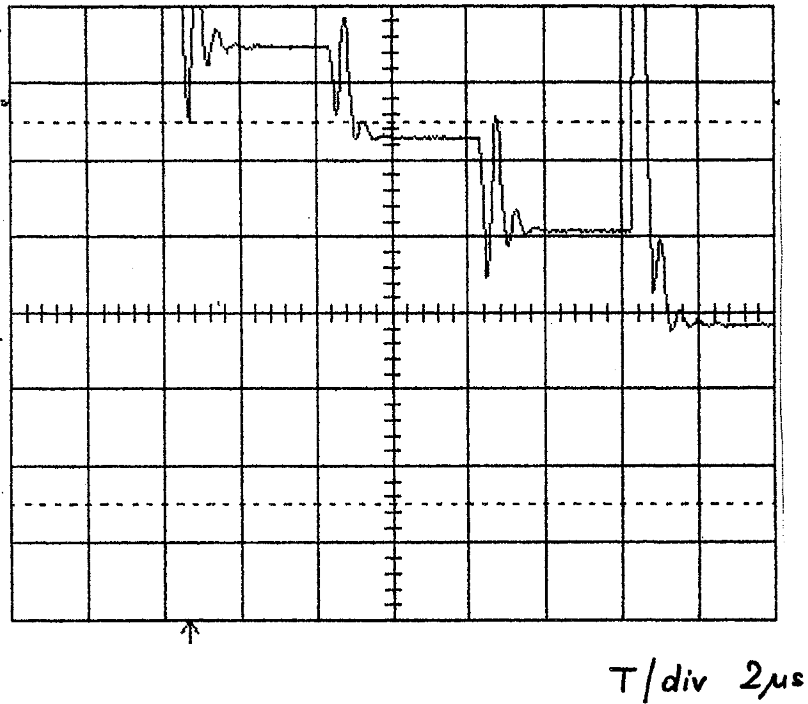


Figure 7.5.2. Hardcopy of the output signal of device #1 as seen on the oscilloscope after 8 krad. Digital inputs were updated at a rate of 250kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). Note the large "gliches" when the input changes; their magnitude increased sharply under irradiation.

7.6 PMI 7541A GP

General remarks

The PMI 7541A turned out to be even more sensitive to irradiation than its Burr Brown counterpart. Therefore the results will be presented in very compressed form. The device was irradiated while its digital inputs were "dynamic" which should give more favourable results than static irradiation bias. Nevertheless it was removed from the test after only 8 krad because of severe degradation.

Pre-irradiation characteristics

Prior to irradiation all parameters were well within specifications.

Electrical parameters and quasistatic test results

Input current

The input current peak was located between 1.0V and 2.5V and could therefore not be detected. No shift to voltages below 1.0V was observed after 8 krad, but the quiescent current in that region increased to 0.6mA after 4 krad and to 2.4mA after 8 krad. The same was observed for input voltages above 2.5V.
This indicates that this device starts leaking heavily (poor field oxide) while the threshold voltage shift played a minor role.

Conclusions

Even for the case of dynamic digital inputs during irradiation the input current is larger than the specifications would allow after only 8 krad (for 0.8V applied to the digital inputs) Static irradiation bias probably leads to an even quicker degradation.

Output leakage current

Output leakage current was measured at both current output pins, for logic "LOW" at the digital inputs at output pin 1, for logic "HIGH" at output pin 2. In this way it was possible to see if any of the output current switches (cf. Figure 2.3) was damaged more than the other.

Table 7.6.1: Output leakage current for different total doses. Measurements were taken at both output current pins; input voltage at the digital inputs was 0.2V for determinig the leakage ot pin 1 and 4.5V for testing pin 2.

	0 krad	4 krad	8 krad
Output pin 1	1.9pA	3.7uA	12.7uA
Output pin 2	0.2pA	2.7uA	7.1uA

Observations

The leakage current increases quickly with total dose. The rate of deterioriation is about equal for both outputs; this means that both output switches are affected equally which is in agreement with the fact that irradiation bias was dynamic.

Conclusions

The device failed to comlpy with the specification at less than 4 krad; as for the evolution of the input current this seems to be due to leakage. Almost identical results were obtained at a preliminary test with a second device of that kind which makes it more unlikely that the tested device was simply an exception.

Digital input current

It increased from about 1pA at 0 krad to some 200pA after 8 krad but was still easily within the specification limit of 1uA.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.6.2.

Table 7.6.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV.

PMI 7541A #4

total dose	4 krad	8 krad
startpoint	+65.4	+139.0
endpoint	-62.9	-136.0
Gain	-128.3	-275.0

Table 7.6.3: Numerical values of INL and DNL for PMI 7541A #4. Values are in mV.

Differential nonlinearity

	0 krad	4 krad	8 krad
7541A #4	1.5	19.5	41.1

Integral nonlinearity

	0 krad	4 krad	8 krad
7541A #4	1.4	17.7	37.3

Discussion

The gain figures prove that both current outputs have been equally affected: "startpoint" and "endpoint" values change at about the same rate. The changes, however, are so big that even after 4 krad the device is already far out of specifications.

Dynamic parameters

Up to 8 krad hardly any change in the figures for the dynamic parameters could be observed. The oscilloscope also did not reveal anything of particular interest.

7.7 ANALOG DEVICES 7541A BQ

General remarks

The AD 7541A turned out to be somewhat more radiation-tolerant than the Burr Brown and PMI devices. But still its performance was not too impressive in preliminary tests, so only one device was irradiated and its digital inputs were kept "dynamic" during irradiation which should give more favourable results than static irradiation bias. After 16 krad it was clear that complete failure was imminent, so it was removed from the test.

Pre-irradiation characteristics

Prior to irradiation all parameters were well within specifications.
Again outstanding INL and DNL figures were observed for all tested Analog Devices parts prior to irradiation.

Electrical parameters and quasistatic test results

Input current

The familiar behaviour of a shift of the input current peak was observed. Unfortunately the measurements were restricted to valid logic levels (0V - 0.8V and 2.4V - 5V), but the position of the current peak (which indicates the voltage where the logic states of inverters change) quickly shifts into that region. It is clearly visible that the current peak moved down below 0.8V after 16 krad, and by looking at the current output figures it was verified that at 0.6V the output current was redirected from pin 1 to pin2; after 12 krad this voltage was about 0.85V, again in agreement with the current peak position.
Leakage was almost negligible: in parts of the curve that were far away from the peak the current remained at pre-irradiation levels (current increase at 0V is a result of the threshold voltage shift).

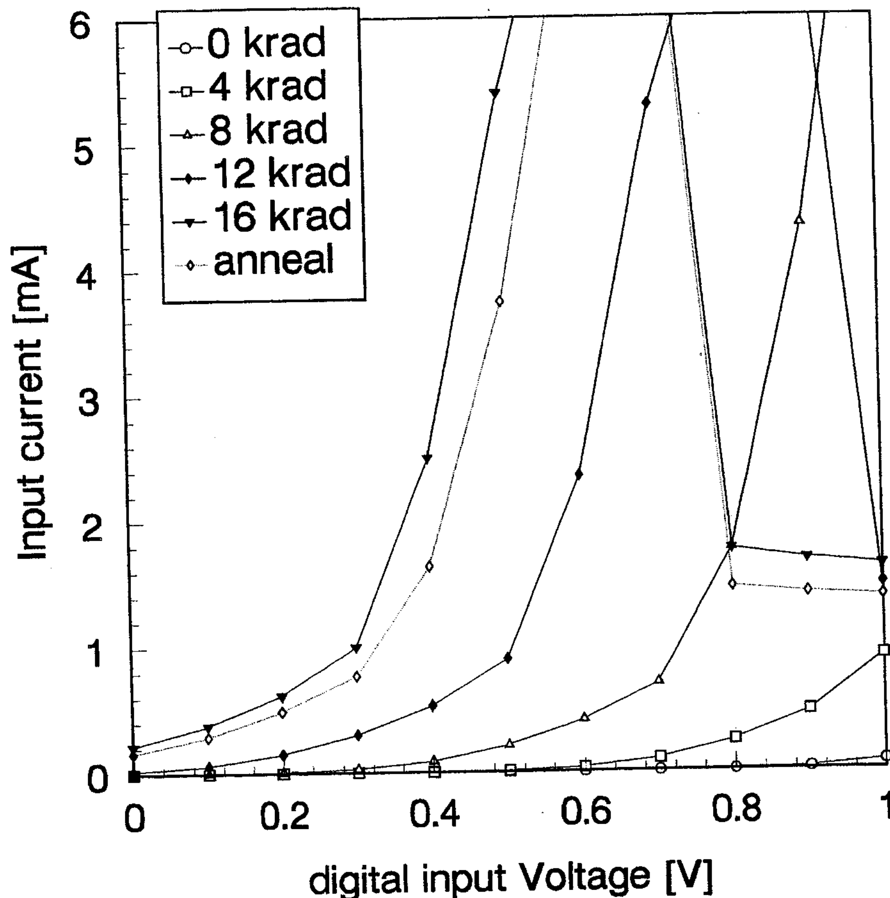


Figure 7.7.1: Input current vs. digital input voltage for several total doses for the device. For reasons of clarity the datapoints have been connected to show the shift to lower voltages. The response to radiation is only a shift in threshold voltage and no strong increase in leakage was observed.

Discussion
The device quickly degraded because of a rapid shift in threshold voltage; probably caused by charge trapping in the gate oxide.

Conclusions
Even for the case of dynamic digital inputs during irradiation the input current is larger than the specifications would allow after only 12 krad (for 0.8V applied to the digital inputs) Static irradiation bias would probably lead to an even quicker degradation.

Output leakage current

Output leakage current was measured at both current output pins, for logic "LOW" at the digital inputs at output pin 1, for logic "HIGH" at output pin 2. In this way it was possible to see if any of the output current switches (cf. Figure 2.3.) was damaged more than the other.

Table 7.7.1: Output leakage current for different total doses. Measurements were taken at both output current pins; input voltage at the digital inputs was 0.2V for determining the leakage of pin 1 and 4.5V for testing pin 2.

	0 krad	4 krad	8 krad	12 krad	16 krad
Output pin 1	13pA	262pA	70nA	3.1uA	23.6uA
Output pin 2	3.9pA	215pA	71nA	2.5uA	11.7uA

Observations

The leakage current increases quickly with total dose. The rate of deterioriation is roughly equal for both outputs; this means that both output switches are affected equally which is in agreement with the fact that irradiation bias was dynamic.

Conclusions

The device failed to comlpy with the specification at a total dose between 4 and 8 krad; this is in agreement with findings at preliminary test with other devices of this type.

Digital input current

It increased from about 1pA at 0 krad to approximately 200pA after 16 krad but was still easily within specifications.

Gain error, differential and integral nonlinearity (DNL and INL)

The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.7.2.

Table 7.7.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV.

Burr Brown 7541A #1

total dose	4 krad	8 krad	12 krad	16 krad
startpoint	-0.3	+1.8	+64.4	+324
endpoint	+0.3	-2.1	-70.0	-327
Gain	+0.6	-3.9	-134.4	-651

Table 7.7.3: Numerical values of INL and DNL for the device. Values are in mV.

Differential nonlinearity

	0 krad	4 krad	8 krad	12 krad	16 krad
7541A #3	0.8	0.8	1.2	2.1	13.9

Integral nonlinearity

	0 krad	4 krad	8 krad	12 krad	16 krad
7541A #3	0.8	0.9	1.4	4.9	11.2

Discussion
The gain figures prove that both current outputs have been equally affected: "startpoint" and "endpoint" values change at about the same rate. According to the output current figures, however, the change in "startpoint" value should be about twice as much as the shift for the endpoint (output pin 1 shows twice as much leakage). These seemingly contradicting findings are an indication that also for this device the resistor values in the R-2R ladder change under irradiation.

The device was still within specifications after 8krad; after 12 krad the gain figures had changed by about 25 LSB (specification limit: 3 LSB).

Dynamic parameters

The figures obtained by the HP3653A spectrum analyzer only show a small degradation after 16 krad (a change of about 1dB on the average with the exception of THD and SNR figures for very high sinewave frequencies in the order of 30kHz). The reason can be directly seen by comparing the output waveforms at 0 krad and 16 krad (Figure 7.7.2)
The output settling slows down considerably; for small steps (= low sinewave frequencies) it might still be possible to (almost) reach the final value within 4us; for bigger steps (= high frequencies) the time is too short.

Discussion
Looking at the waveforms one might get the impression that settling resembles the step response of an R-C combination. It is not clear how either the resistance or the capacitance at the current output could have increased so much. However, this behaviour had already been found in another Analog Devices DAC (see chapter 7.3) and is clearly different from an increase in switching speed which manifests its presence by "glitches" when the digital input code is changed.

Conclusion
The settling speed was exceeding its specification limits probably after 12 krad, but certainly after 16 krad.

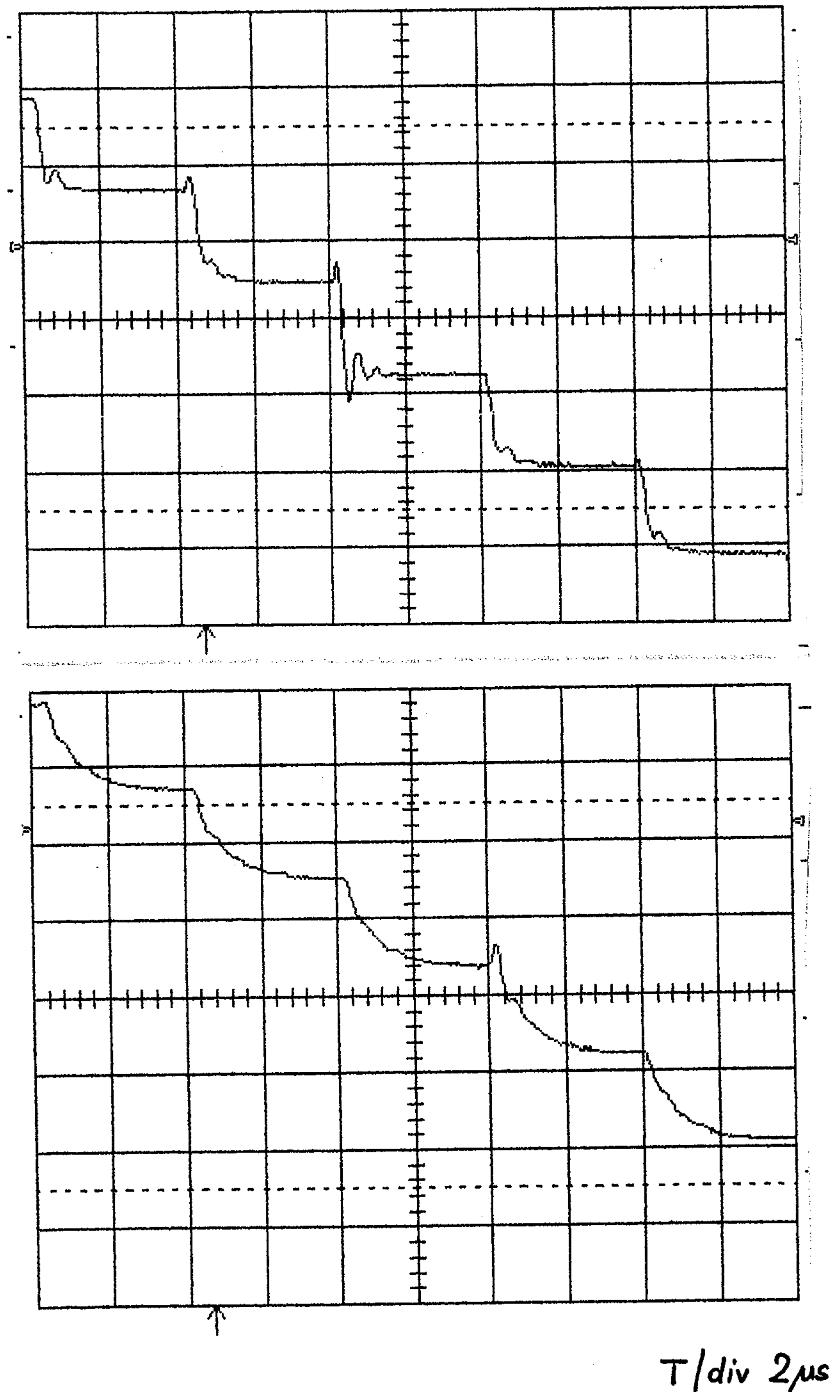


Figure 7.7.2: Hardcopy of the output signal of the device as seen on the oscilloscope. Digital inputs were updated at a rate of 250kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). A clear increase in settling time can be observed when comparing the situation after 4 krad (top) and after 16 krad (bottom).

7.8 HARRIS 7541 LN

General remarks

Two devices were subjected to the final tests after earlier testing had suggested that the Harris 7541 shows much less changes than devices from other companies. During the tests it was once more verified that keeping digital inputs constantly high during irradiation leads to much quicker degradation than dynamic input bias. This was the reason why irradiation of device #5 ("static") was stopped after 25 krad due to degradation while device #4 ("dynamic") was irradiated up to 100 krad. This difference will become apparent especially for the output leakage figures.

Pre-irradiation characteristics

INL figures were slightly above 0.5 LSB for device #4, all other parameters were in accordance with the specifications.

Electrical parameters and quasistatic test results

Input current

Looking at the input current figures gives a first impression of what difference it makes if digital inputs are static or dynamic during irradiating: For device #5 the current peak had shifted to values below 0.8V after 25 krad (see Figure 7.8.1); the same shift was much slower for device #4 and the peak was just about to cross the 1V mark after 100 krad!

In addition, the redirecting of the output current from pin 2 to pin 1 was observed roughly at the corresponding current peak position for device #5; for device #4 this had not yet taken place for voltages below 1.0V even after 100 krad.
Leakage was almost negligeable: in parts of the curve that were far away from the peak the current remained at pre-irradiation levels (current increase at 0V is a result of the threshold voltage shift).
Both devices showed strong annealing when left at room temperature for 30 days.

Discussion

The strong shift in threshold voltage observed for device #5 shows that charge trapping in the gate oxide is strongly enhanced if the MOSFET gates are biased during irradiation; dynamic bias seems to allow for some annealing during irradiation because the effect was much smaller for device #4. Trapped charges are obviously only weakly bound because room temperature annealing for 30 days led to a threshold voltage shift into the opposite direction, indicating that the charge density in the oxide had significantly decreased.

No increased leakage currents were found after irradiation.

Conclusions

Device #4 remained within specifications even after 100 krad.
Device #5 violated them probably at a total dose of 10-12 krad, but certainly after 15 krad.

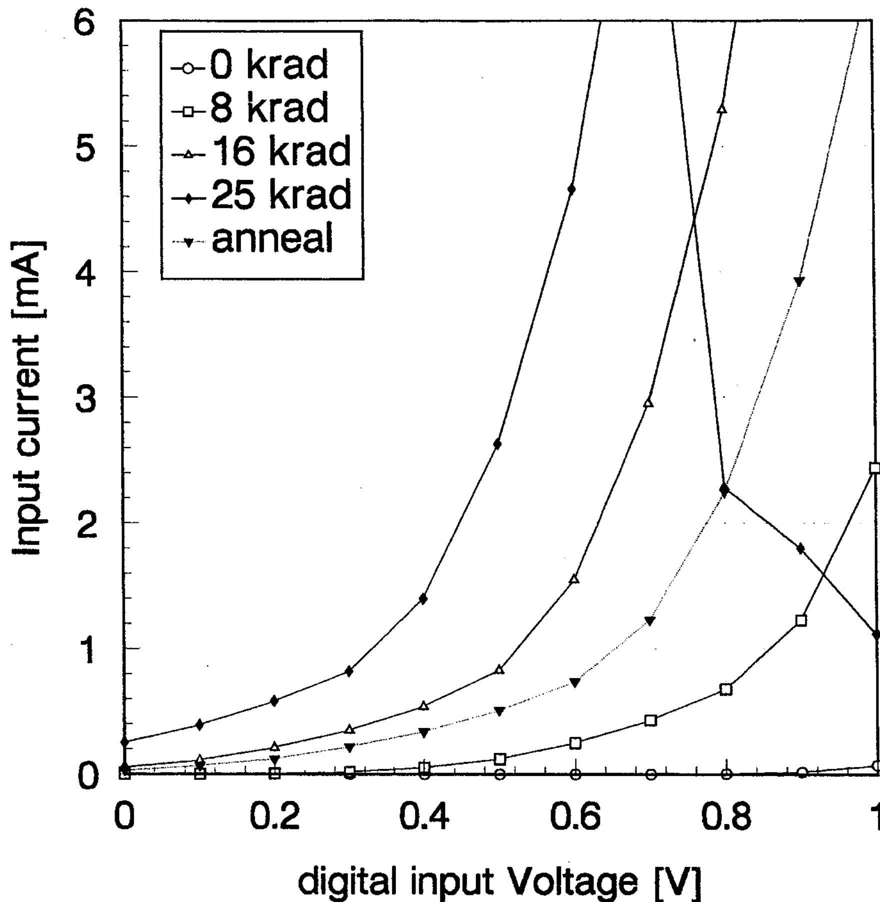


Figure 7.8.1: Input current vs. digital input voltage for several total doses for the device. For reasons of clarity the datapoints have been connected to show the shift to lower voltages. The response to radiation is only a shift in threshold voltage and no strong increase in leakage was observed. The threshold voltage moved back to higher voltages after the device had been annealed for 30 days at room temperature.

Output leakage current

Output leakage current was measured at both current output pins, for logic "LOW" at the digital inputs at output pin 1, for logic "HIGH" at output pin 2. Here the comparison between device #4 and #5 clearly shows the influence of irradiation bias conditions. Note that output leakage is roughly the same for both output FETs in device #4. In device #5 the output FET for pin 2 (FET 8 in Figure 7.1.6) showed almost no leakage after 25 krad while the FET for pin 1 (FET 9 in Figure 7.1.6) showed severe damage. The gate of FET 9 was biased during irradiation, the gate of FET 8 was unbiased....

Table 7.8.1: Output leakage current for different total doses. Measurements were taken at both output current pins; input voltage at the digital inputs was 0.2V for determining the leakage of pin 1 and 4.5V for testing pin 2. (ann.: 30 days of annealing at room temperature)

Harris 7541 #4

dose [krad]	0	8	12	25	40	70	100	ann.
Output pin 1	0.7pA	366pA	3.4nA	63nA	752nA	2.8uA	2.2uA	178nA
Output pin 2	0.3pA	310pA	3.3nA	39nA	652nA	2.4uA	1.7uA	254nA

Harris 7541 #5

dose [krad]	0	4	8	12	16	25	ann.
Output pin 1	2pA	120pA	12nA	289nA	5.6uA	27uA	1.3uA
Output pin 2	0.3pA	10pA	130pA	518pA	1.1nA	2.1nA	1.1nA

Observations

The numbers mostly speak for themselves; striking is the difference in output leakage for device #5 between the two outputs; different irradiation bias conditions are responsible for this. Leakage for device #4 is roughly the same for both output FETs, which is not surprising as both had identical irradiation bias conditions.

Conclusions

Device #5 was out of specifications after 12 krad; but only output pin 1 showed significant leakage.

Device #4 did not meet specifications after 25 krad; both outputs were equally affected.

Digital input current

It increased from about 1pA at 0 krad up to approximately 350pA after 100 krad but was still easily within specifications (device #4). Values were lower for device #5 after 25 krad.

Gain error, differential and integral nonlinearity (DNL and INL)

Table 7.8.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV. (n.e.: not evaluated

Harris 7541A #4

total dose	16 krad	25 krad	40 krad	70 krad	100 krad	ann.
startpoint	n.e.	+0.6	+11.2	+35.5	+29.6	+4.3
endpoint	n.e.	-3.0	-16.0	-42.6	-39.3	-13.2
Gain	n.e.	-3.6	-27.2	-78.1	-68.9	-17.5

Harris 7541A #5

total dose	8 krad	12 krad	16 krad	25 krad	ann.
startpoint	-0.1	+3.1	+23.4	+133.3	+19.2
endpoint	-0.6	-0.4	-0.6	-2.1	-2.8
Gain	-0.5	3.5	24.0	-135.4	22.0

Table 7.8.3: Numerical values of INL and DNL for the device. Values are in mV. (n.e.: not evaluated; ann.: annealing at room temperature for 30 days)

Differential nonlinearity

	0 krad	8 krad	12 krad	16 krad	25 krad	40 krad	70 krad	100 krad	ann.
7541 #4	3.3	n.e.	n.e.	n.e.	3.1	2.9	10.6	11.2	2.8
7541 #5	0.8	1.1	1.0	7.1	28.9	n.e.	n.e.	n.e.	7.0

Integral nonlinearity

	0 krad	8 krad	12 krad	16 krad	25 krad	40 krad	70 krad	100 krad	ann.
7541 #4	3.6	n.e.	n.e.	n.e.	2.6	4.2	9.3	16.1	3.3
7541 #5	1.6	1.6	2.0	5.0	17.8	n.e.	n.e.	n.e.	3.7

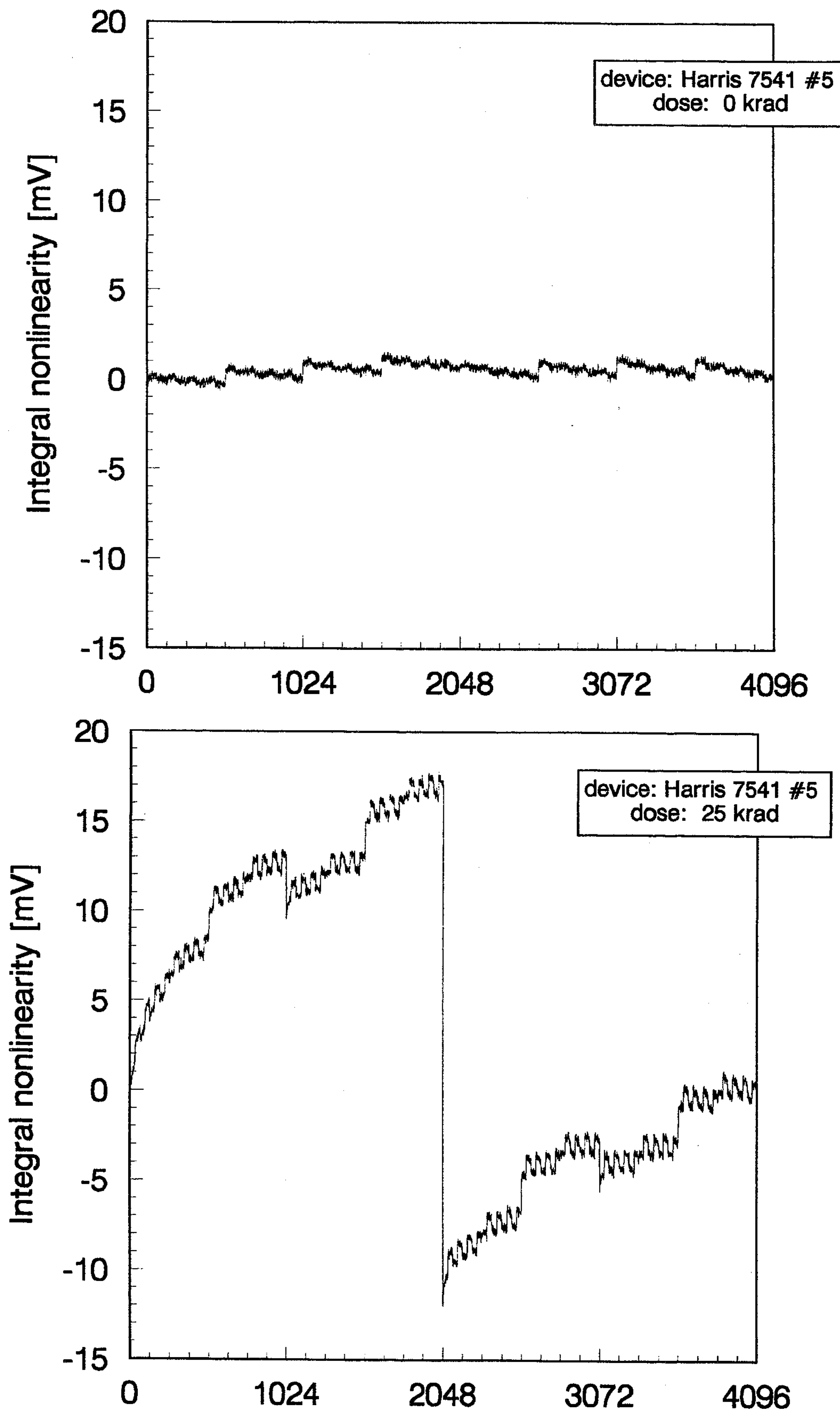


Figure 7.8.2: Evolution of INL for device #5 which showed greater degradation after 25 krad that device #4 after 100 krad.

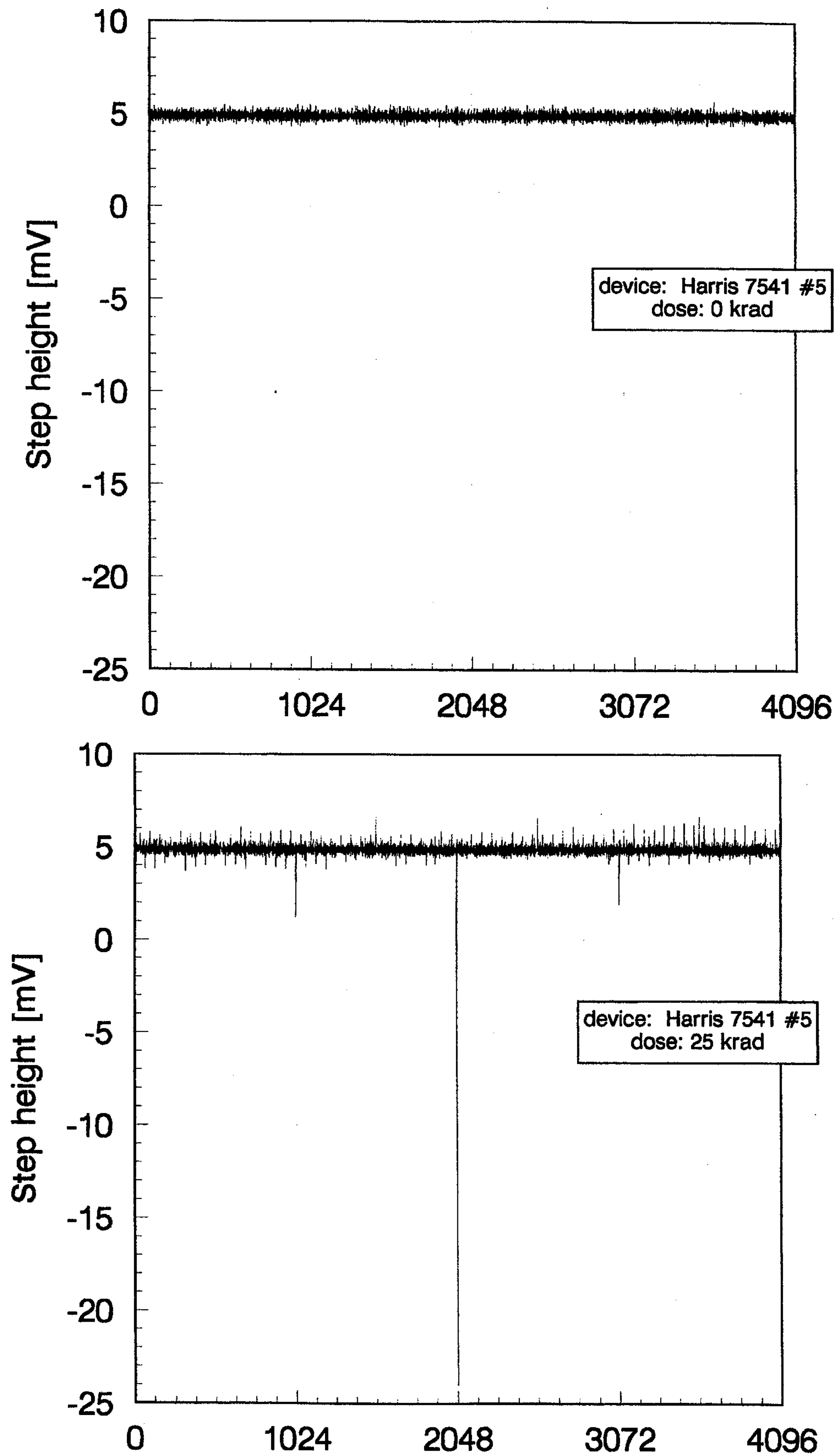


Figure 7.8.3: Evolution of DNL for device #5 which showed greater degradation after 25 krad that device #4 after 100 krad.

Discussion

The gain figures for device #4 prove that both current outputs have been equally affected:

"startpoint" and "endpoint" values change at about the same rate.
As expected after looking at the output current figures the "endpoint" values for device #5 remained almost unchanged while the "startpoint" figures changed much more than for device #4.
INL and DNL figures reflected the degradation much less than the gain figures which is an indication that all bits are affected at the same rate.

Conclusions

The specifications for gain figures allow for an unusually high tolerance (12 LSB), therefore the devices stayed within this limit up to rather high doses. Taking a more conservative number of 3 LSB would mean that device #4 failed after 40 krad, device #5 at about 13-14 krad.

Dynamic parameters

All tested Harris devices showed very high "glitches" after a new digital code was applied to the inputs (Figure 7.8.4). Of course these steep pulses distorted the signal even more than usual when it had passed through the anti-aliasing filter of the spectrum analyzer. The result was very bad and widely varying numbers for THD and SNR which were regarded as completely unreliable.
This behaviour must have been a result of unsynchronized opening and closing of the MOSFET switches and irradiation made matters even worse.

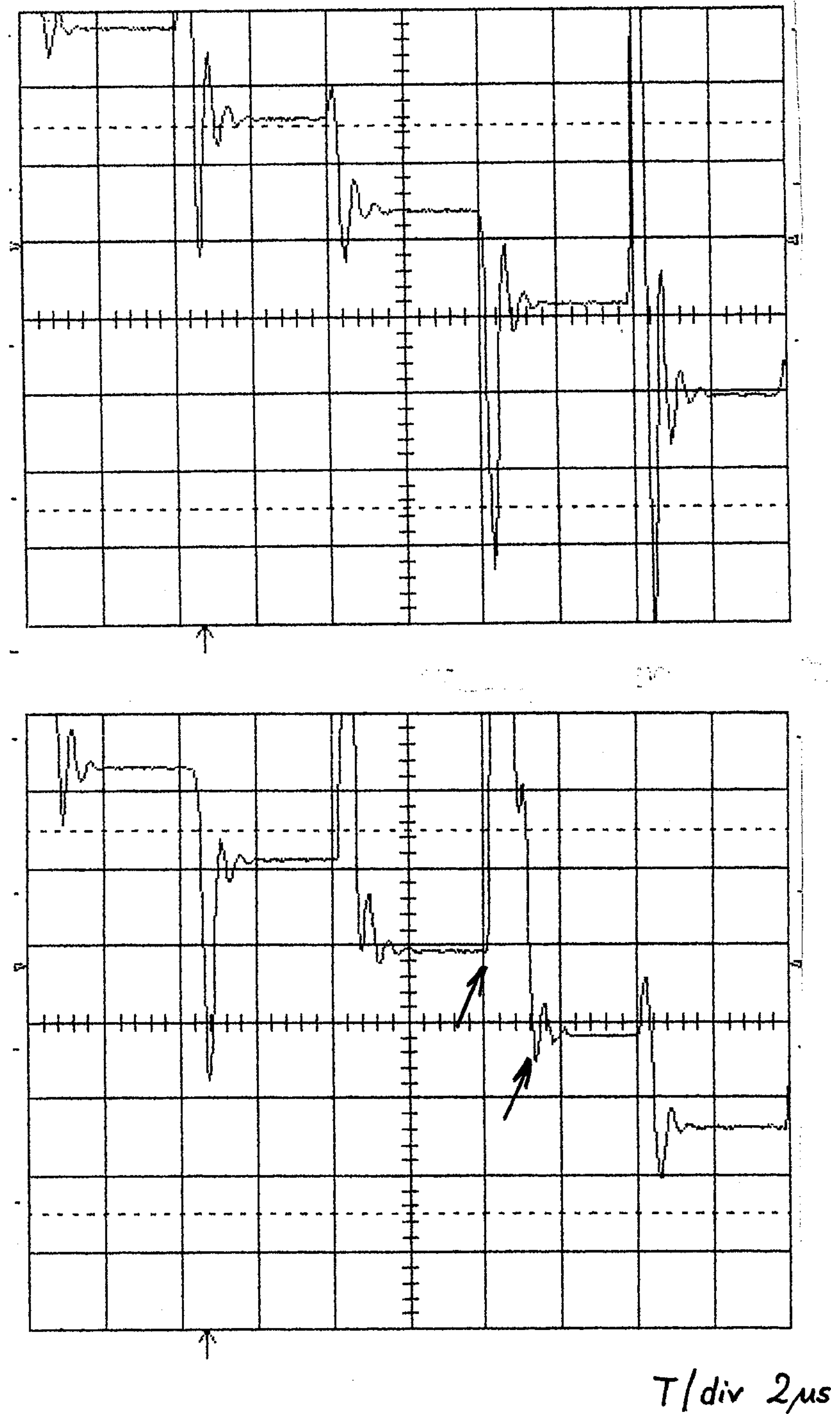


Figure 7.8.4: Hardcopy of the output signal of the device as seen on the oscilloscope . Digital inputs were updated at a rate of 250kHz, and the figure shows a detail of a bipolar sinewave around 0V. Stepheight is largest in that part of the curve, and as it crosses 0V most bits of the digital input word change state, among them the MSB. Gain is 200mV per division, with a resolution of 5mV (or 1 LSB). Even prior to irradiation there were considerble "glitches" (top); after 25 krad their magnitude increased even further and the settling time as well, as it can best be seen at the major bitchange (see arrows in bottom picture)

Conclusion

Settling speed was probably not exceeded. But nevertheless some deterioriation in switching speed can be observed which might be due to increased interface state density.

7.9 SIPEX 7541A BQ

General remarks

Two devices (#2 and #3; see Table 6.1) were subjected to the final tests after earlier testing had suggested that the Sipex 7541 shows almost no degradation up to comparably high total doses. Both devices were irradiated to 100 krad and showed very interesting results: Different irradiation bias conditions did not lead to different results; both devices were within specifications after 70 krad. After 100 krad, however, they were not operational any more.

Pre-irradiation characteristics

Both devices showed parameters that were in accordance with the specifications.

Electrical parameters and quasistatic test results

Input current

Both devices showed a rather unique behaviour and therefore it is a pity that testing was restricted to valid logic levels. Figure 7.9.1 shows the characteristics of device #2 which were identical for device #3:

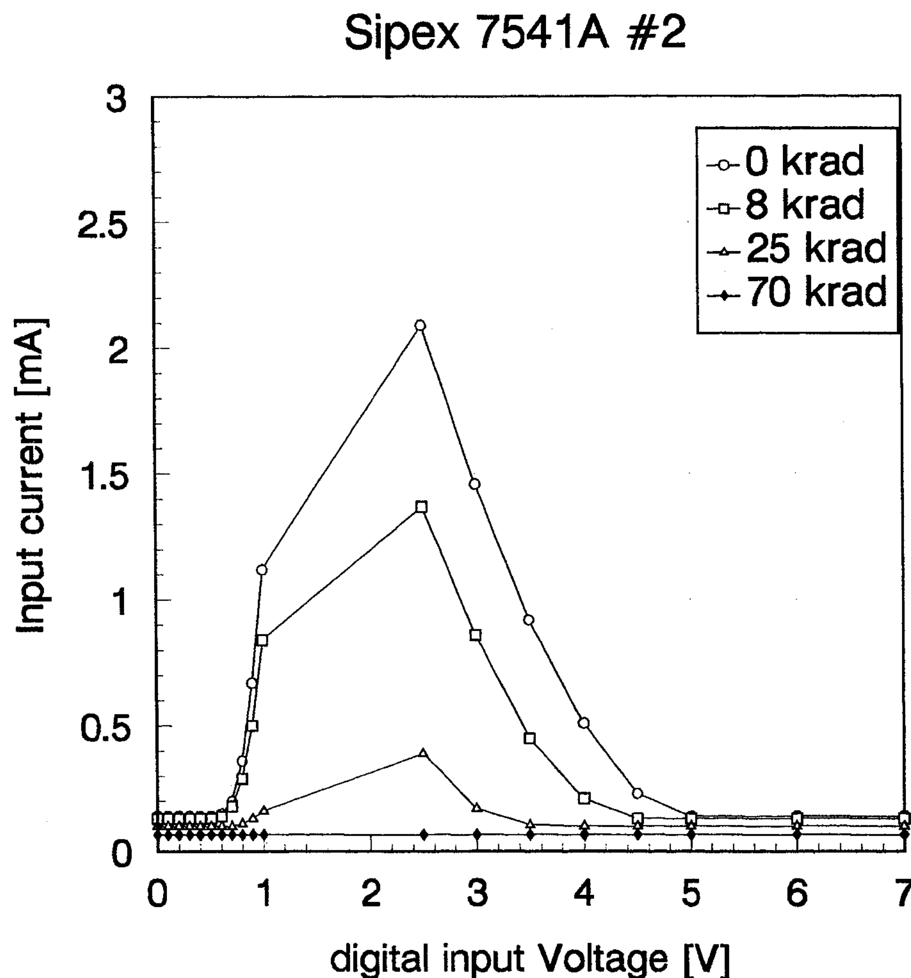


Figure 7.9.1: Input current vs. digital input voltage for several total doses for device #2. For reasons of clarity the datapoints have been connected.

With increasing total dose the input current became smaller and smaller. The current peak which can be imagined in the region between 1.0V and 2.5V was flattened out as far as can be seen (maybe a small rest could have been found somewhere in this voltage range). Leakage seems to be nonexistent as the quiescent current decreases for **all** voltages.

Discussion

No likely explanation for the observed behaviour could be found. Maybe the p-MOSFETs in the devices showed a much stronger threshold voltage shift than the n-MOSFETs so that finally the latter had not yet turned "ON" at an input voltage when the p-channel transistors were already turned "OFF". This exotic explanation would also explain final failure: at a certain point the resistance of the p-MOSFETS would always be smaller than the resistance of their n-type counterparts, no matter what the input voltage might be. This, of course, would make a change in the logic state of an inverter (which is nothing else than a voltage divider) impossible.

No increased leakage currents were found after irradiation.

Conclusions

No violation of the specifications was observed for the input current.

Output leakage current

Output leakage current was measured at both current output pins, for logic "LOW" at the digital inputs at output pin 1, for logic "HIGH" at output pin 2. Both devices showed almost identical behaviour in spite of their different bias conditions during irradiation.
After 100 krad the output current could not be redirected to output 1 any more, which of course meant complete failure of both devices.

Table 7.9.1: Output leakage current for different total doses. Measurements were taken at both output current pins; input voltage at the digital inputs was 0.2V for determining the leakage of pin 1 and 4.5V for testing pin 2.

Sipex 7541A #2

dose [krad]	0	12	25	70	100
Output pin 1	17pA	18pA	20pA	23pA	20pA
Output pin 2	268nA	268nA	272nA	262nA	1.1mA

Sipex 7541A #3

dose [krad]	0	12	25	70	100
Output pin 1	16pA	15pA	15pA	47pA	40pA
Output pin 2	273nA	272nA	288nA	281nA	1.1mA

Observations
No increase in leakage currents were detected. But after 100 krad the MOSFET switches were obviously not able to switch the current to output pin 1. It appears that this is rather due to logic failure of the driving inverters than to sudden leakage.

Conclusions
Both devices did not show any significant changes up to 70 krad. After 100 krad they were not operational any more.

Digital input current

For both devices it increased from about 1pA at 0 krad up to approximately 350pA after 100 krad but was still easily within specifications

Gain error, differential and integral nonlinearity (DNL and INL)

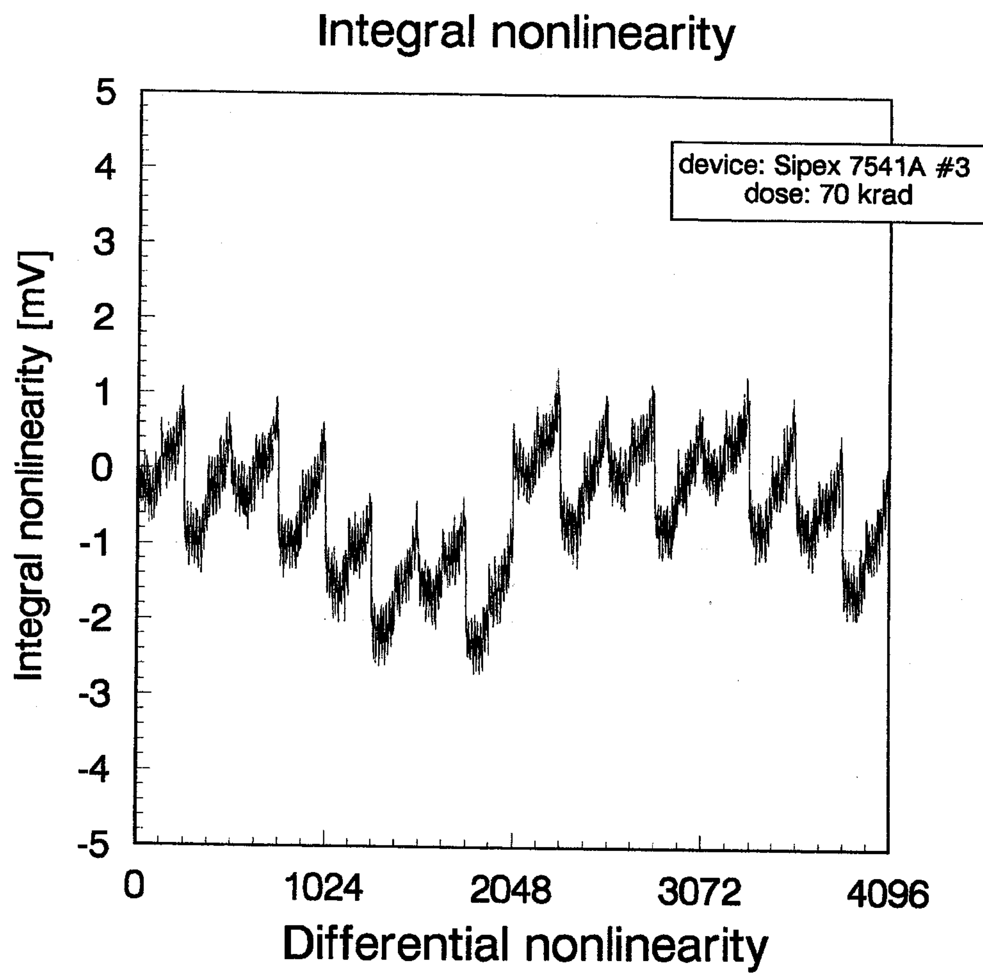
The evolution of the "startpoint" and the "endpoint" output voltage as well as the change in gain (difference "endpoint" minus "startpoint") is given in table 7.9.2.
Some results for INL and DNL are shown in figure 7.9.1.in graphical form just to show that these parameters did not change.

Table 7.9.2: Changes in analog output voltage for binary input codes 00..00 (startpoint) and 11..11 (endpoint) and corresponding change in gain. Numbers are in mV, for device #2. Device #3 behaved identical (n.e.: not evaluated; n.f.: not functional any more)

Sipex 7541A #2

total dose	16 krad	25 krad	40 krad	70 krad	100 krad
startpoint	-0.2	n.e.	+0.2	0.0	n.f.
endpoint	+1.1	n.e.	+1.5	+2.9	n.f.
Gain	+1.3	n.e.	+1.3	+2.9	n.f.

Conclusions
Up to 70 krad the device performance did not seem to be affected by the irradiation at all. No violations of specification figures were observed until after 100 krad both devices were suddenly functionally dead.



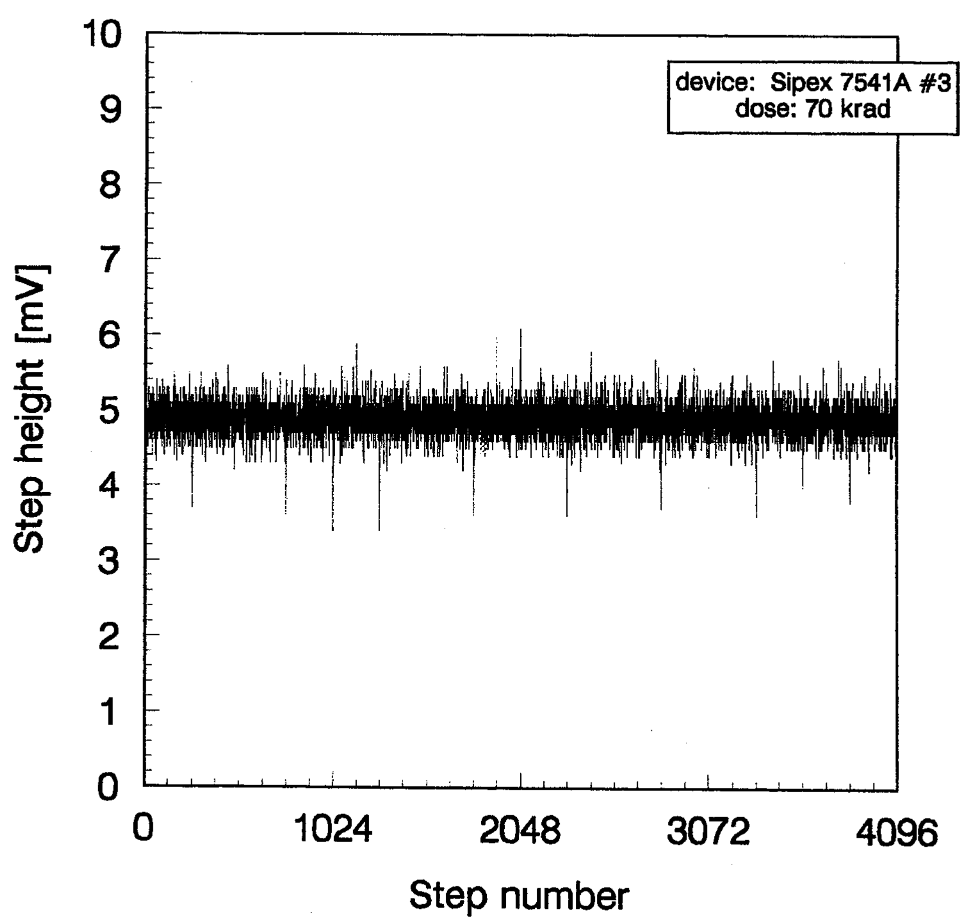


Figure 7.9.2: INL and DNL figures for device #2 after 70 krad. Both parameters are still smaller than 0.5 LSB and appear hardly unchanged when compared to pre-irradiation figures._

Dynamic parameters

Because of the equipment problems already described earlier (see Section 5.3) the absolute measurement values for the dynamic parameters Signal/Noise Ratio (SNR) and Total Harmonic Distortion (THD) are not reliable. For low digital sinewave frequencies (a full period of the sinewave is represented by many points, so the stepheight from one point to the next is small) the numbers should be quite accurate; for higher frequencies only the relative change of the results for different total doses will give some qualitative information; the numbers itself are meaningless.

The following table shows the results obtained with the HP3653A Spectrum Analyzer; digital data was updated at a rate of 250kHz, and sinewaves of different frequencies were fed into the DAC under test (f_{in}=125Hz and 9.875kHz). It was avoided to test frequencies that are a multiple of 50Hz because of possible mains noise pickup.

Table 7.9.3: Figures for THD and SNR for two different input frequencies. Numbers are in dB.

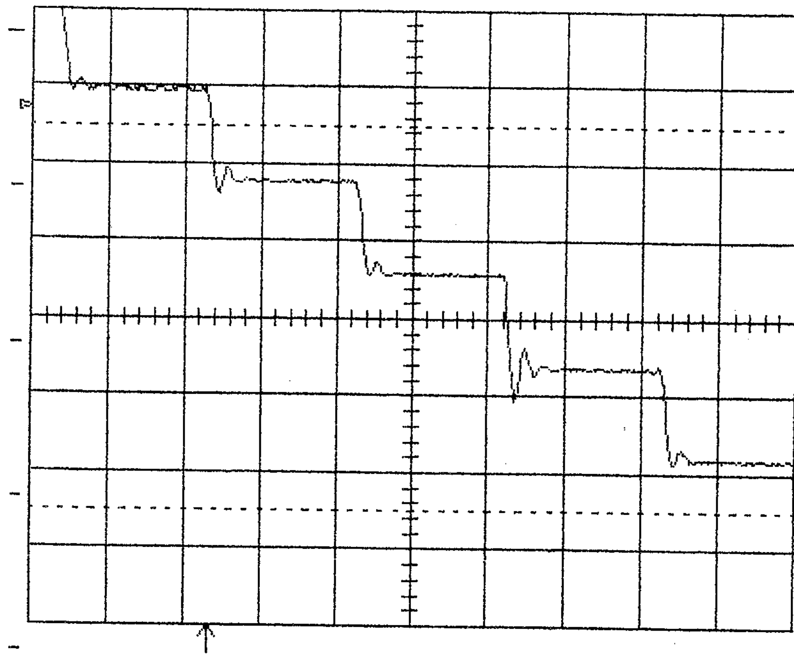
Total Harmonic Distortion

f_{in}= 125 Hz	0 krad	8 krad	16 krad	25 krad	40 krad	70 krad
7541A #2	-80.7	-81.9	-81.0	-80.3	-79.8	-64.7
7541A #3	-77.2	-77.3	n.e.	-76.3	-75.3	-60.8
f_{in}= 9.875 kHz						
7541A #2	-67.6	-67.6	-67.3	-67.5	-60.8	-34.2
7541A #3	-67.5	-67.7	n.e.	-62.1	-49.5	-31.2

Signal/Noise Ratio

f_{in}= 125 Hz	0 krad	8 krad	16 krad	25 krad	40 krad	70 krad
7541A #2	-68.0	-68.2	-67.8	-68.3	-68.0	-63.0
7541A #3	-67.9	-67.8	n.e.	-67.6	-67.2	-60.1
f_{in}= 9.875 kHz						
7541A #2	-60.0	-59.8	-59.7	-59.8	-56.3	-33.0
7541A #3	-59.9	-59.9	n.e.	-57.7	-48.2	-30.3

The figures are almost identical up to 25 krad. After 40 krad (especially for high frequency sinewaves at the inputs) device #3 shows faster degradation than device #2.
A look at the oscilloscope screen gives the explanation (Figure 7.9.3): after having been subjected to ever increasing total doses the output of the DACs showed "glitches" that became bigger and bigger. Again the most pronounced "glitch" could be found at the major bitchange. Device #3 was more affected than device #2; this might be due to the different bias conditions at irradiation, but the number of test samples is too small to give definitive answers.
The apparently unsynchronized opening and closing of switches after higher total doses was the first indication of degradation for these devices. This could have been caused by creation of interface states which are known to slow down switching speed.
Nevertheless the appearance of "glitches" seems to indicate that functional failure is not far away, an observation that had also been made with samples during preliminary tests.



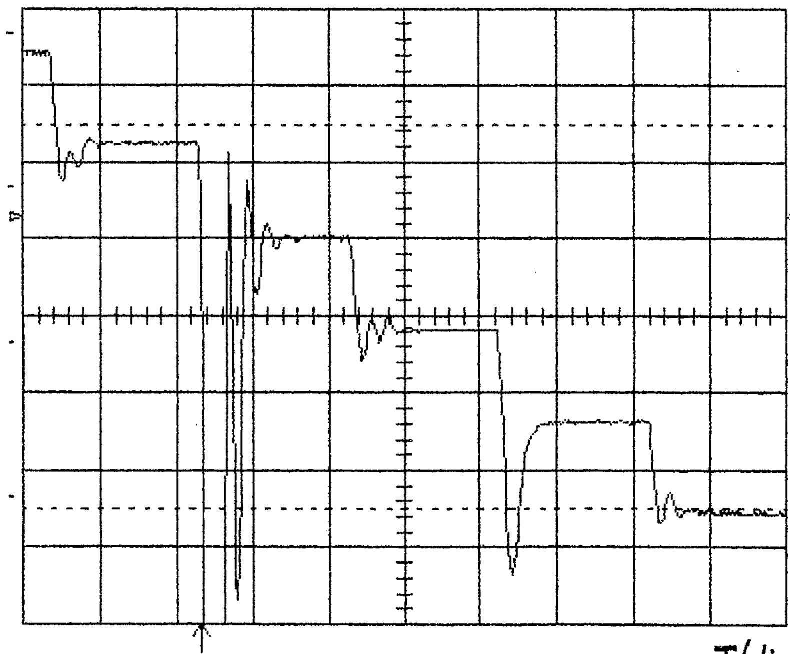


Figure 7.9.3 Comparison of output signal at 0 krad (top) and 70 krad for device #3. Device #2 showed the same effects but they were less pronounced. The big "glitch" at the major bitchange can be clearly seen (bottom picture).

Conclusion

Settling speed limits were probably not exceeded. But nevertheless some deterioriation in switching speed can be observed which might be due to increased interface state density.

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