ESA RADIATION REPORT

ESA_QCA008901S_C

TITLE

Radiation Latch-up Screening of FPGA from Lucent, Lattice and QuickLogic

EUROPEAN SPACE AGENCY
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Distribution
Complete :
Summary :

Class : Host System : Microsoft Word 97 for Windows, SE Macro Rev 3.0
Contract No : Host File : ...\D-P-REP-1083-SE.doc

SUMMARY

Heavy Ion induced Latch-up tests of Lucent, Lattice and Quicklogic have been performed. All device types indicated Latch-up under heavy ion irradiation.

The Lucent and Quicklogic indicated latch-up at a LET of 14 MeV/cm^2/mg. The Lucent device showed some kind of permanent damages with increased supply currents, after a few latch-ups.

The Lattice device showed a LET threshold somewhere between 34 and 48 MeV/cm^2/mg. The ^{252}Cf tests indicated that SEU in control registers of the device might give functionality upsets. No indications of upset in the PROM storage element have been observed.

DOCUMENT CHANGE RECORD

Changes between issues are marked with a left-bar.

Issue	Date	Paragraphs affected	Change information
1	23 Aug 2001	All	New document

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1. ABSTRACT

This document presents ^{252}Cf and heavy ion induced latch-up tests of three FPGA candidates for space application, Lattice, Lucent and Quicklogic. The results indicate that all three device types are susceptible to Latch-up.

2. FACILITIES

2.1 ^{252}Cf

A dedicated vacuum system for SEL test (and SEU) by ^{252}Cf at Saab Ericsson Space/Components Lab was used for SEL tests. The ^{252}Cf source consist of a thin evaporated layer of Californium on metal backing. The source activity was at time of test 16 kBq. The average nominal stopping power value for the fission fragments is LET=43 MeV/cm^2/mg. However, due to low penetration depth in Silicon (~13um), metal and polysilicon layers, the real stopping power value would be much lower depending on the technology of the device under test.

2.2 Heavy Ion Facility

Latch-up tests have been performed at the Heavy Ion Facility in UCL, Belgium. Ion types and fluence used are reported in the chapter for each device type.

3. LATTICE IspLSI5384V(A)

Lattice Semiconductor is a manufacturer that has a non-volatile technology. The ispLSI5000V Family is an In-System Programmable CPLDs. Utilising Lattice's patented E^2CMOS® technology, ispLSI5000V devices provide non-volatile in-system programming specified up to 10,000 program/erase cycles and 20 years data retention. The technology makes it possible for the devices to be programmed and reprogrammed while soldered on-board.

The initial series includes the ispLSI 5256V, 5384V, and 5512V, with logic densities ranging from 256 to 512 macro cells / registers. The I/O pins are compatible with both 3.3- and 2.5V logic levels and with input tolerance of 5V.

	IspLSI 5384VA-70LQ208	IspLSI 5384V-125LQ208ES
Lattice Family	IspLSI 5000V	IspLSI 5000V
Chip revision	A	-
F_{max}	70 MHz	125 MHz
Usable PLD gates:	18,000	18,000
Macro cells:	384	384
Registers	384	384
Inputs+I/O	144	144
Vcc	3.3V	3.3V
I/O	5 V (input)/3.3V /2.5 V	5 V (input)/3.3V /2.5 V

3.1 Test Samples

TEST SAMPLE DETAILS

PART TYPE	: IspLSI5384VA-70LQ208
	: IspLSI5384V-125LQ208ES
FUNCTIONAL ASSIGNMENT	: CPLD / FPGA
MANUFACTURER	: Lattice
QUALITY LEVEL	: Commercial
DATE CODE	: IspLSI5384VA ....- 9934
	IspLSI5384V ....- 9913
PACKAGE	: PQ208 (Plastic Quad Flat Package)
SPEED GRADE	: IspLSI5384VA ....- 70 (Low Power)
	IspLSI5384V ....- 125 (Low Power)
SERIAL NUMBER	: IspLSI5384VA ....- #21
	IspLSI5384V ....- #1

IspLSI5384VA is a later chip revision of IspLSI5384V.

	Marking *Top side*	**Marking** *Bottom Side*	**Marking** *Chip*
IspLSI5384V Lattice #21	Lattice Logo IspLSI 5384V 125LQ208 ENG SAMP	9913 7800104B4	Chip marking isn't visible behind scraps of plastic.
IspLSI5384VA Lattice #01	Lattice Logo IspLSI 5384VA 70LQ208 B935A04	9934 7840125A1	M-logo 1998 HD5385V-00 LATTICE Lattice-logo

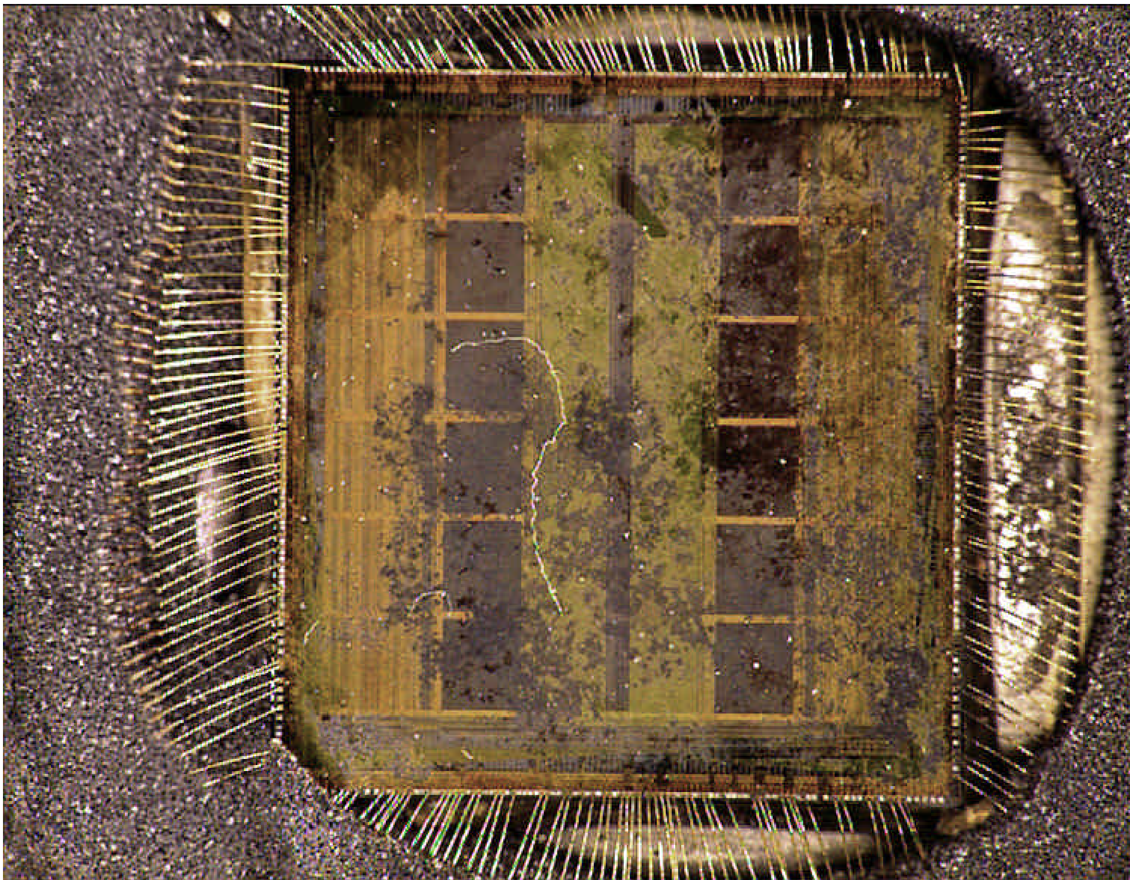

Figure 3.1 Chip photo of Lattice sn#01 after etching of plastic. The size of the chip is 10 x 10 mm.

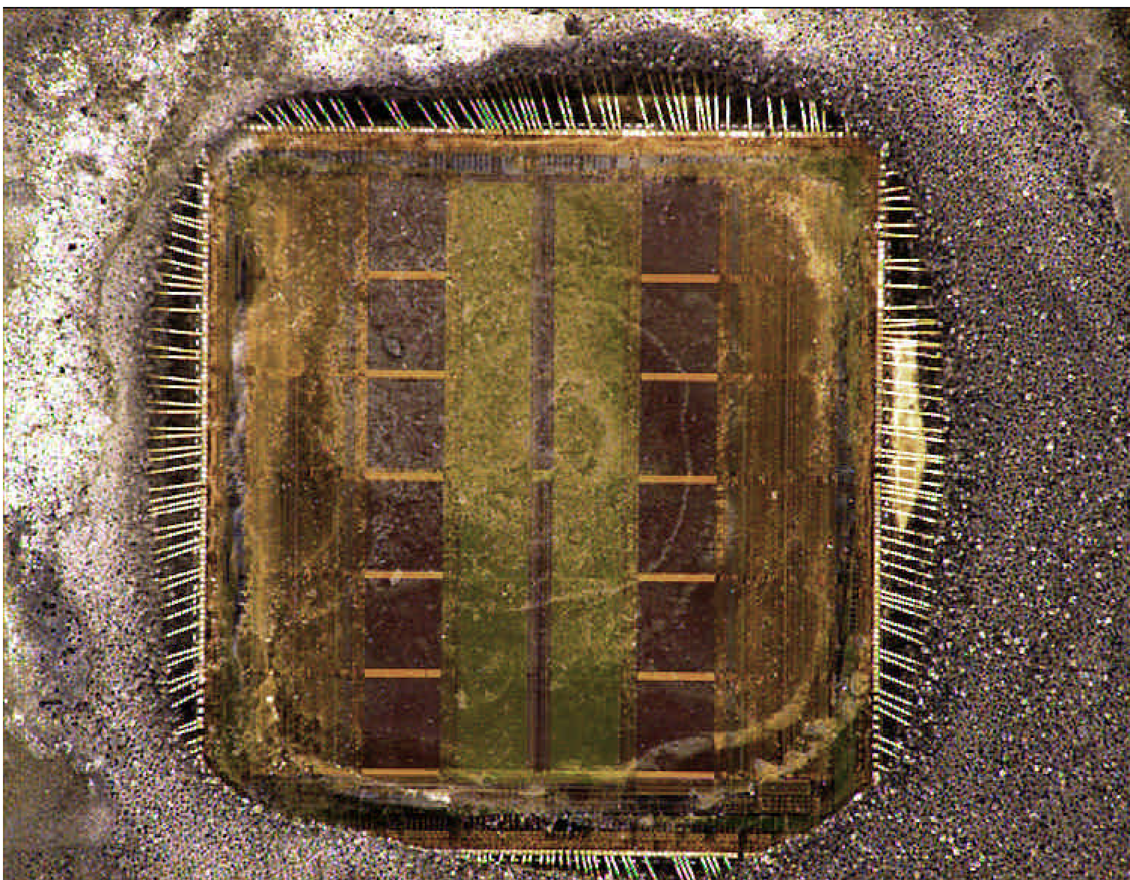

Figure 3.2 Chip photo of Lattice sn#21 after etching of plastic.

3.2 Test Techniques

Single Event Latch-up tests have been performed using a test board connecting power pins and the clock pin of the DUT to external power source and clock generator. Two samples have been delidded and prepared for SEL tests. Functionality test, supply current measurement and program verification by the JTAG interface was performed after delidding, confirming that the devices still were in normal function. The DUT are individually biased and any SEL will result in immediate (within 200 µs) shut down of the power.

3.2.1 Test Methods

Table 3.1 Electrical Test Conditions

TEST PARAMETER	TEST CONDITIONS
Icc	Vcc = 3.3 V
Test Mode	Static Mode*

* The ^{252}Cf-tests were performed in a dynamic mode with f_{CLK} = 25 MHz.

3.2.2 Design of Device

The devices were programmed with a design implementing one shift register utilising 66% of available register cells. With this design functionality of the device could easily be confirmed with a function generator and an oscilloscope.

3.2.3 Test Flow

Table 3.2 Test Flow for Latch-up tests

Step No.	Description
1	Programming of Device
2	JTAG verification of Program
3	Function Test of Device
4	Irradiation with In Situ Icc measurement and SEL detection
5	JTAG verification of Program
6	Function Test of Device

The programming and JTAG verification is performed with Lattice's IspDCD software and a download cable connected between a PC and the test board. At UCL we couldn't connect this cable to the test board and only step 1-3 were performed outside the chamber before start of the first test run.

3.3 SEL Results

3.3.1 ^{252}Cf Results

IRRADIATION DETAILS

TEST FACILITY	:	Saab Ericsson Space
IRRADIATION SOURCE	:	^{252}Cf
BIAS CONDITIONS	:	Vcc = 3.3V
TEST TEMPERATURE	:	Room Temperature
TEST MODE	:	f_{CLK} = 25 MHz

The DUT was clocked with 25 MHz during irradiation.

The fluence for the test is calculated from known activity of the source, distance (r) between source and DUT and time of irradiation.

No SEL was detected for any of the tested devices. In Table 3.3 fluence and cross sections for each tests are presented.

During test run #1 & #2 the standby current was stable through the whole tests at ~120mA. Test run #5, however, the current changed in abrupt steps during irradiation (see Fig. 3.3). Post-irradiation JTAG verification resulted in return to initial current value. This could indicate on SEU in configuration registers used by the JTAG procedure. No errors in program or functionality were detected. However, the function test was performed after the JTAG verification test, and very likely the device was out of function before the JTAG verification. Function test during irradiation at the various current levels has not been performed.

Table 3.3 Test Result for SEL tests at ^{252}Cf source for Lattice IspLSI devices.

Run#	SN#	Device Type	r	Flux	Runtime	Fluence	SEL Cross Section
			[mm]	[ions/(s·cm^2)]	[hours]	[ions/cm^2]	[cm^2/device]
1	01	IspLSI5384V	28	8.1	234.13	6.8 10^6	<1.5 10^{-7}
2	01	IspLSI5384V	16	20.9	185.83	1.4 10^7	<7.2 10^{-8}
5	21	IspLSI5384VA	16.5	20.6	162.17	1.2 10^7	<8.4 10^{-8}

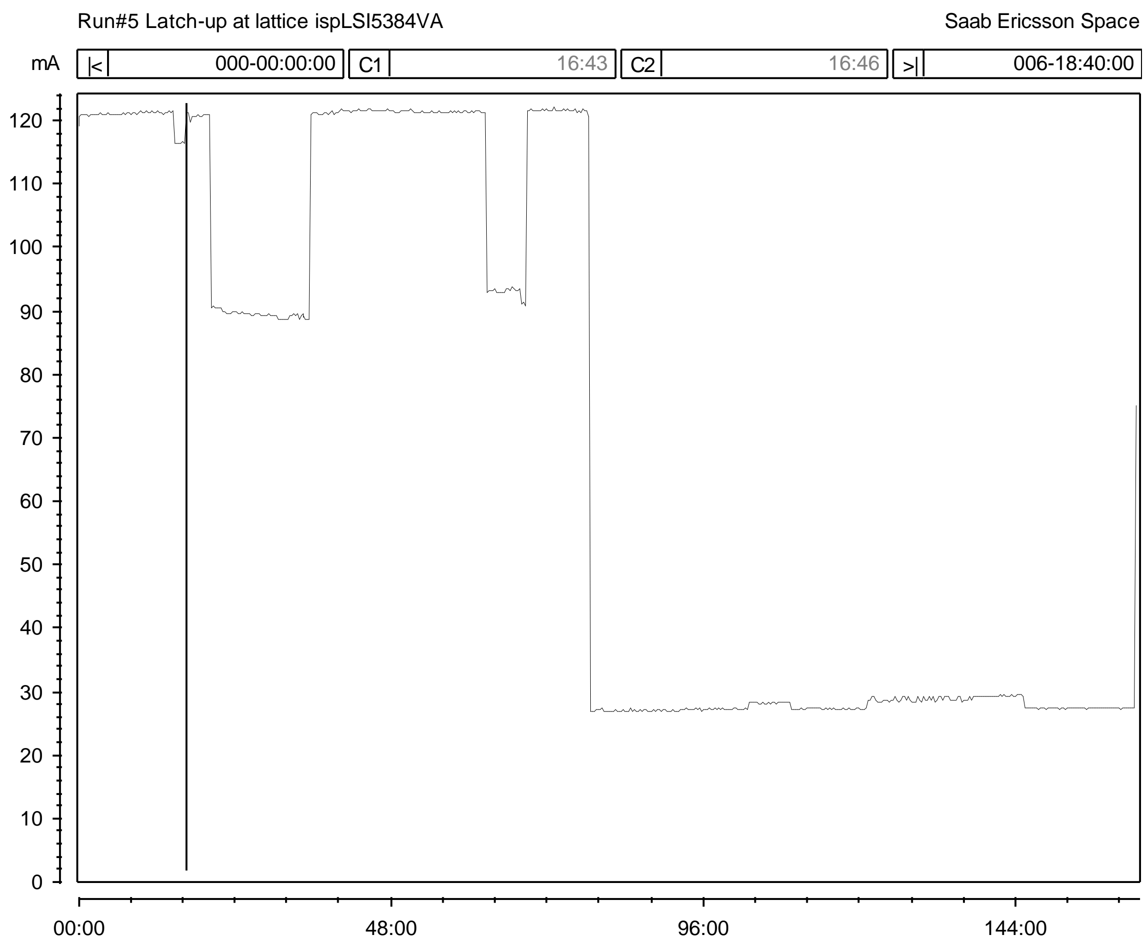

Figure 3.3 Icc measurement vs. elapsed time in hours for Run #5. 16:43 hours after test start had the whole test a power-down due to a power failure in the building.

3.3.2 Heavy Ion Results

IRRADIATION DETAILS

TEST FACILITY : UCL
IRRADIATION SOURCE : Selected Heavy Ions
BIAS CONDITIONS : Vcc = 3.3V
TEST MODE : Static Mode

The SEL tests at Heavy Ion Facility were only performed on the IspLSI5384VA (SN#21) device (latest chip revision). The device was static biased during all heavy ion tests.

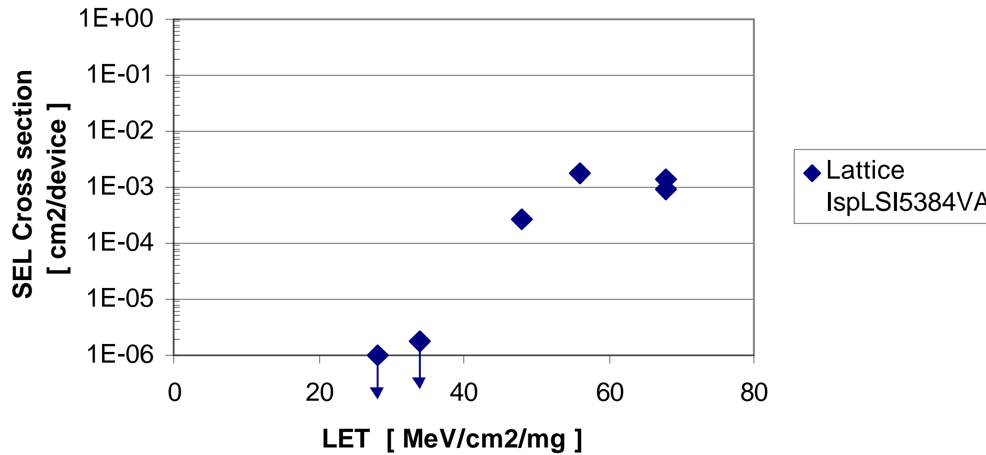

Figure 3.4 Graph showing Cross Section for Latch-up as a function of LET value for the Lattice IspLSI5384VA device.

Table 3.43 Heavy Ion data form UCL tests.

Run#	Ion	LET MeV/cm^2/mg	Tilt	LET$_{Eff}$ MeV/cm^2/mg	Flux Ions/cm^2/s	Fluence Ions/cm^2	SEL #	SEL Cross Section cm^2/device
45	Ar	14,1	60°	28,2	2500	1,0 10^6	0	<1,0 10^{-6}
46	Xe	55,9	0°	55,9	1500	1,1 10^5	199	1,8 10^{-3}
47	Kr	34	60°	68	400	6,0 10^4	56	9,4 10^{-4}
48	Kr	34	60°	68	400	3,4 10^4	48	1,4 10^{-3}
49	Kr	34	45°	48,08326	800	2,0 10^5	52	2,6 10^{-4}
50	Kr	34	0°	34	1400	5,7 10^5	0	<1,8 10^{-6}

4. LUCENT OR2C06A

Lucent OR2C06A belongs to the ORCA serie2 of Lucent technologies. It is an SRAM based FPGA. This makes it easy to implement the device for small experimental projects. You only have to have access to a PROM-programmer where the bitstream file is downloaded.

4.1 Test Object

The OR2CxxA Family is 5V FPGA manufactured in 0,35 µm CMOS technology. The family have devices from 11k to 100k usable gates and up to 480 I/Os. The architecture consists of Lockup tables (LUT), on chip SRAM and flip-flop registers.

	OR2C06A- T 144
Usable PLD gates:	15,900
LUT :	576
Registers	576
Inputs+I/O	114
Vcc	5,0V

4.2 Test Samples

TEST SAMPLE DETAILS

PART TYPE	:	LUCENT OR2C06A-2 T 144
FUNCTIONAL ASSIGNMENT	:	CPLD / FPGA
MANUFACTURER	:	LUCENT
QUALITY LEVEL	:	Commercial
DATE CODE	:	9815S
PACKAGE	:	TQ144 (Plastic Thin Quad Flat Package)

	Marking *Top side*	Marking *Bottom Side*	Marking *Chip*
OR2C06A Sn #01 & #02	ORCA Logo - - 9815S	37914882 2C06A 9810S	M-logo LUCENT Chip marking isn't visible behind scraps of plastic

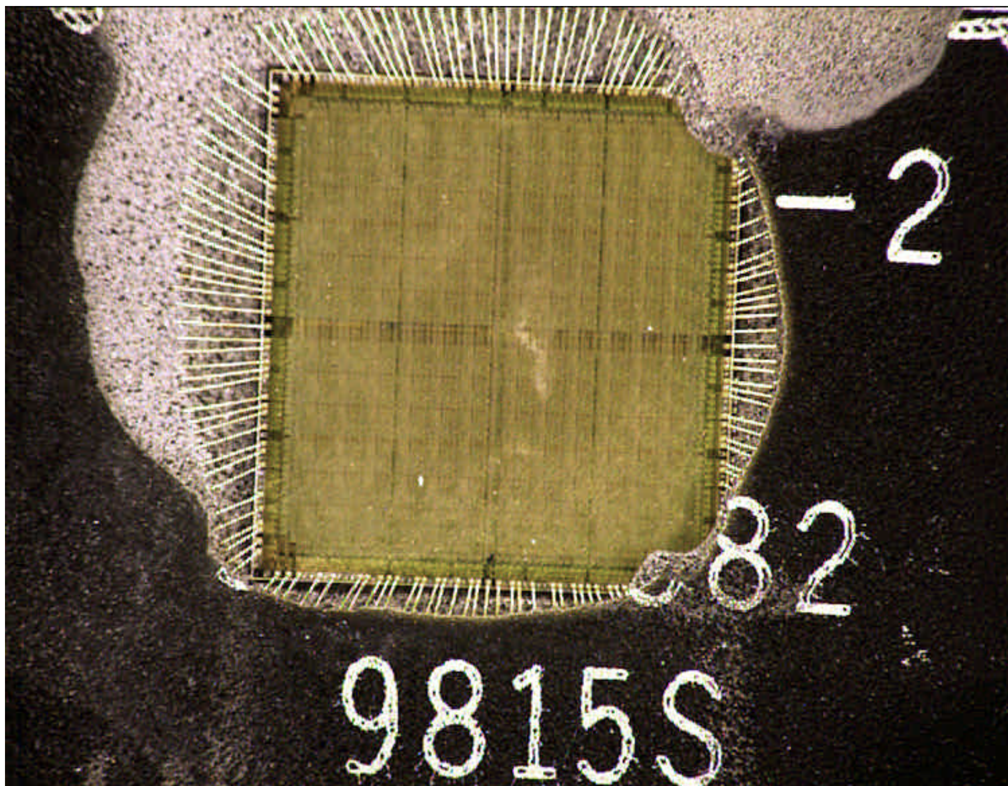

Figure 4.1 Chip photo of Lucent sn#1 after etching of plastic. The size of the chip is 6,6 x 6,6 mm.

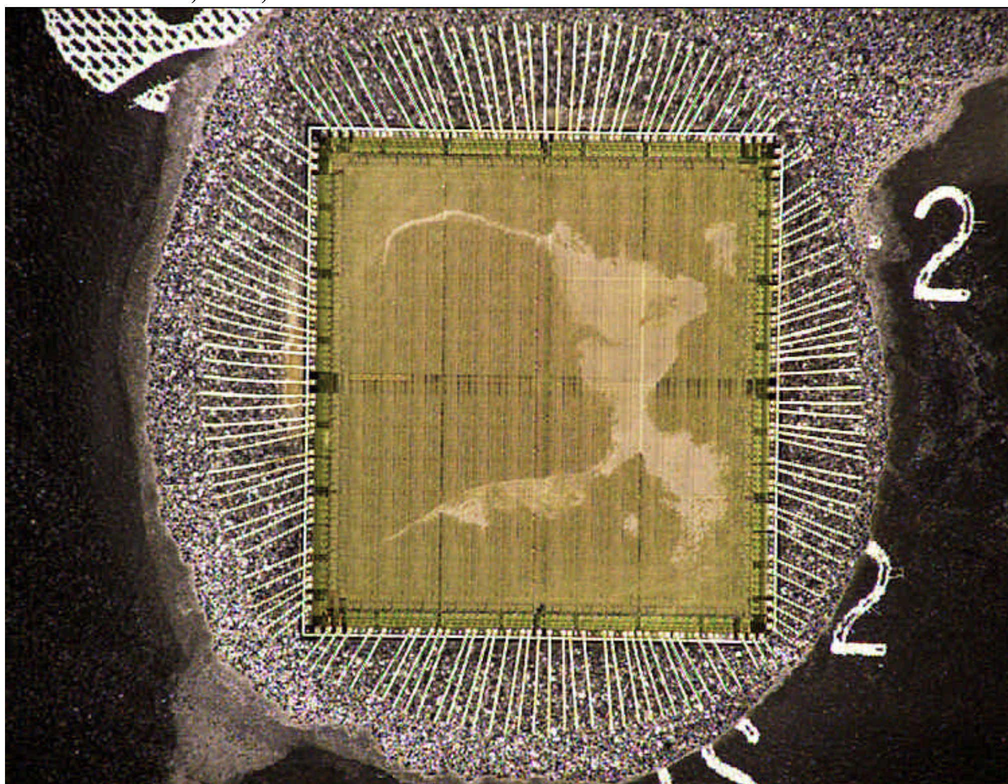

Figure 4.2 Chip photo of Lucent sn#2 after etching of plastic.

4.3 Test Techniques

Single Event Latch-up tests have been performed using a test board connecting power pins and the input pins of the DUT to external power source and pull-downs. The test board has a PROM with bitstream data for the DUT. The PROM and the DUT use the same power source. This means that each time the power is cycled will the PROM be reset and the DUT will automatically read bitstream into the DUT at start-up.
The plastic encapsulation on top of the device has been etched down to the chip on two samples. Functionality test and supply current measurements were performed after etching. The power is connected to a latch-up detection circuit and any SEL will result in immediate (within 200 µs) shut down of the power.

4.3.1 Test Methods

Table 4.1 Electrical Test Conditions

TEST PARAMETER	TEST CONDITIONS
Icc	Vcc = 5,0 V
Test Mode	Static Mode

4.3.2 Design of Device

The device was programmed with a design implementing one shift register utilising 20% of available register cells. Also some direct connections between inputs and outputs were implemented. With this design it could easily be confirmed that the device had been correctly initialised.

4.3.3 Test Flow

Table 4.2 Test Flow for Latch-up tests

Step No.	Description
1	Power-up
2	DUT read bitstream data from external PROM through Master Parallel interface
3	Irradiation with In Situ Icc measurement and SEL detection

4.4 SEL Results

4.4.1 ^{252}Cf Results

IRRADIATION DETAILS

TEST FACILITY	:	Saab Ericsson Space
IRRADIATION SOURCE	:	^{252}Cf
BIAS CONDITIONS	:	Vcc = 5,0V
TEST TEMPERATURE	:	Room Temperature
TEST MODE	:	Static Mode
SAMPLE	:	SN#01

Californium tests showed a SEL cross section of $\sim 3 \cdot 10^{-4}$ cm^2/device and a few latch-up gave permanently damages. The current didn't return to normal value after the latch-up protection circuit powered down the device.

4.4.2 Heavy Ion Results

IRRADIATION DETAILS

TEST FACILITY	:	UCL
IRRADIATION SOURCE	:	Selected Heavy Ions
BIAS CONDITIONS	:	Vcc = 5,0V
TEST MODE	:	Static Mode
SAMPLE	:	SN#02

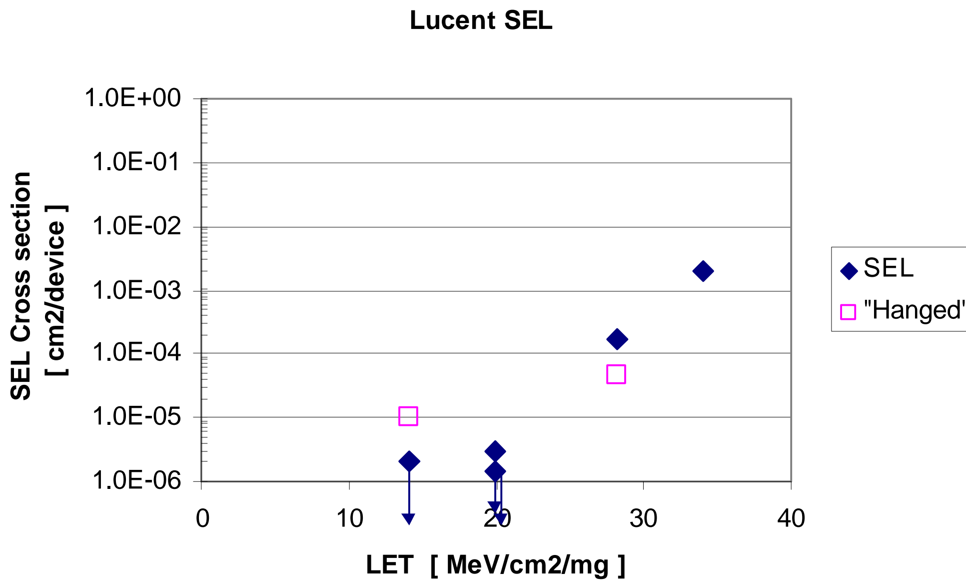

Figure 4.3 Graph showing Cross Section for Latch-up as a function of LET value for the Lucent OR2C06A-2 device.

Table 4.3 Heavy Ion data from UCL Tests

Run#	Ion	LET MeV/cm²/mg	Tilt	LET_{Eff} MeV/cm²/mg	Flux Ions/cm²/s	Fluence Ions/cm²	SEL #	SEL Cross Section cm²/device
51	Kr	34	0°	34	800	$1,8\ 10^{4}$	36	$2,0\ 10^{-3}$
13	Ar	14,1	0°	14,1	700	$9,9\ 10^{4}$	1*	$1,0\ 10^{-5}$
14	Ar	14,1	0°	14,1	400	$5,0\ 10^{5}$	0	$<2,0\ 10^{-6}$
15	Ar	14,1	45°	19,9	2000	$3,4\ 10^{5}$	0	$<3,0\ 10^{-6}$
16	Ar	14,1	45°	19,9	2000	$6,9\ 10^{5}$	0	$<1,5\ 10^{-6}$
17	Ar	14,1	60°	28,2	1100	$2,1\ 10^{4}$	1*	$4,8\ 10^{-5}$
18	Ar	14,1	60°	28,2	1100	$1,8\ 10^{5}$	30	$1,7\ 10^{-4}$

* The supply current didn’t return to normal value (“Hanged”) after the latch-up protection circuit powered down the DUT. In Run#13 current increased from 10mA to 30mA and in run#17 to 50mA.

5. QUICKLOGIC QL4090

Quicklogic QuickRAM QL4090 is an antifuse FPGA with embedded RAM modules. Quicklogic offer a big military program with many ceramic packages available which makes it to a good candidate for space use.

5.1 Test Object

QuickRAM in the QuickLogic's ESP family is an FPGA with embedded dual port SRAM modules. The family includes devices from 9k to 90k PLD gates with 8 to 22 RAM modules of 1,152 bits. The I/O may interface with 3,3 and 5 V devices. QuickRAM is fabricated on a 0.35 µm four-layer metal process.

	QuickRAM QL4090 CQ208
Quicklogic Family	QuickRAM ESP
Usable PLD gates:	90,000
RAM Modules:	22 blocks of 1,152 bits
Logic Cells:	1,584
Vcc	3.3V / 5,0V
I/O	5 V/3.3V

5.2 Test Samples

TEST SAMPLE DETAILS

PART TYPE	: QL4090
FUNCTIONAL ASSIGNMENT	: ESP FPGA
MANUFACTURER	: QUICKLOGIC
QUALITY LEVEL	: Commercial
DATE CODE	: 0015
PACKAGE	: CQ208 (Ceramic Quad Flat Package)
SERIAL NUMBER	: #01, #02

	Marking *Top side*	Marking *Bottom Side*	Marking *Chip*
QL4090 Sn #01 & 02		00620A02 D31010.00 0025BJ	XL36210 QUICKLOGIC 1998 QL-logo C-logo M-logo

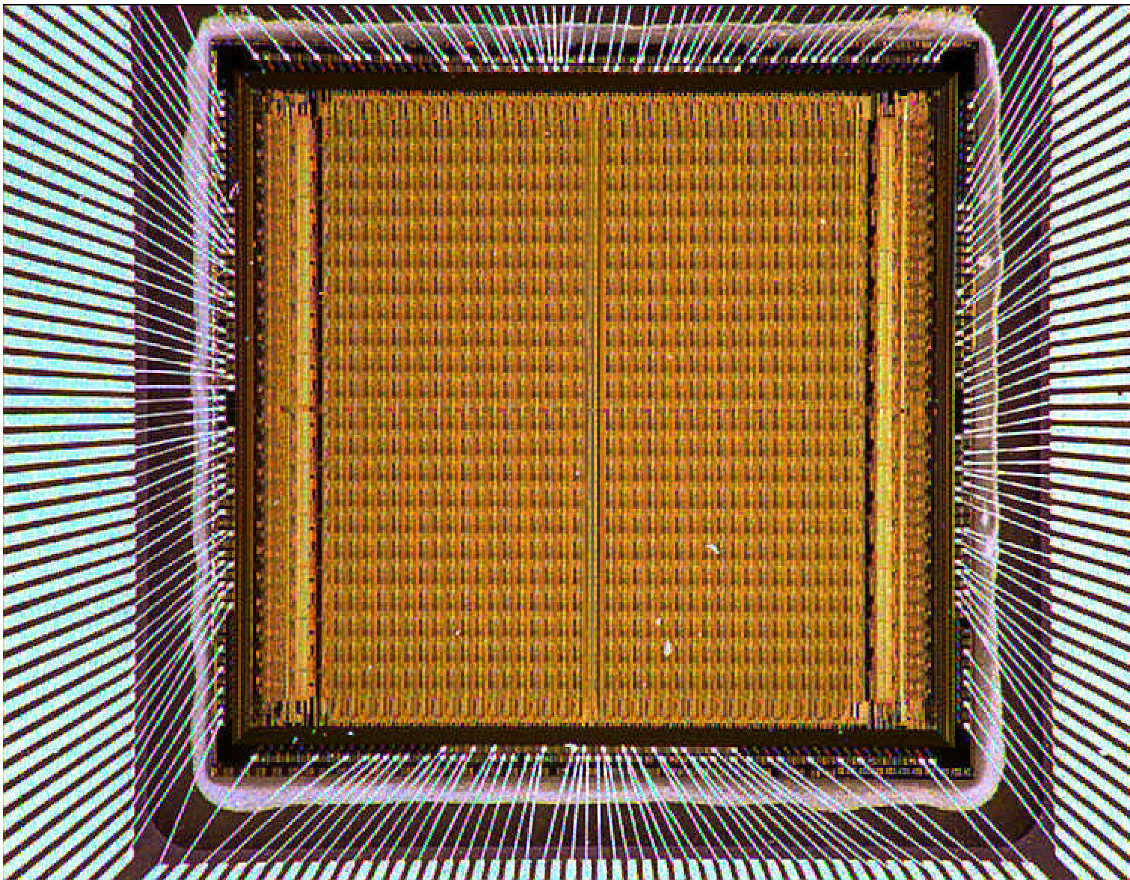

Figure 5.1 Chip photo of Quicklogic sn#01. The size of the chip is 9,4 x 9,1 mm.

5.3 Test Techniques

Single Event Latch-up tests have been performed using a test board connecting power pins and the input pins of the DUT to external power source and pull-downs.
Two samples were carefully delidded before testing. Functionality test and supply current measurement was performed after delidding, confirming that the devices still were in normal function. The power is connected to a latch-up detection circuit and any SEL will result in immediate (within 200 µs) shut down of the power.

5.3.1 Test Methods

Table 5.1 Electrical Test Conditions

TEST PARAMETER	TEST CONDITIONS
Icc	V_{CC} = 3.5 V V_{CCIO} = 3.5 V
Test Mode	Static Mode

5.3.2 Design of Device

The devices were programmed with a design implementing shift registers utilising more than 90% of available register cells and I/O registers. No of the RAM modules were implemented. The devices were programmed by the manufacturer before delivery to Saab Ericsson Space.

5.4 SEL Results

5.4.1 Heavy Ion Results

IRRADIATION DETAILS

TEST FACILITY : UCL
IRRADIATION SOURCE : Selected Heavy Ions
BIAS CONDITIONS: : V_{CC} = 3.5 V
V_{CCIO} = 3.5 V
TEST MODE : Static Mode
SAMPLE : SN#02

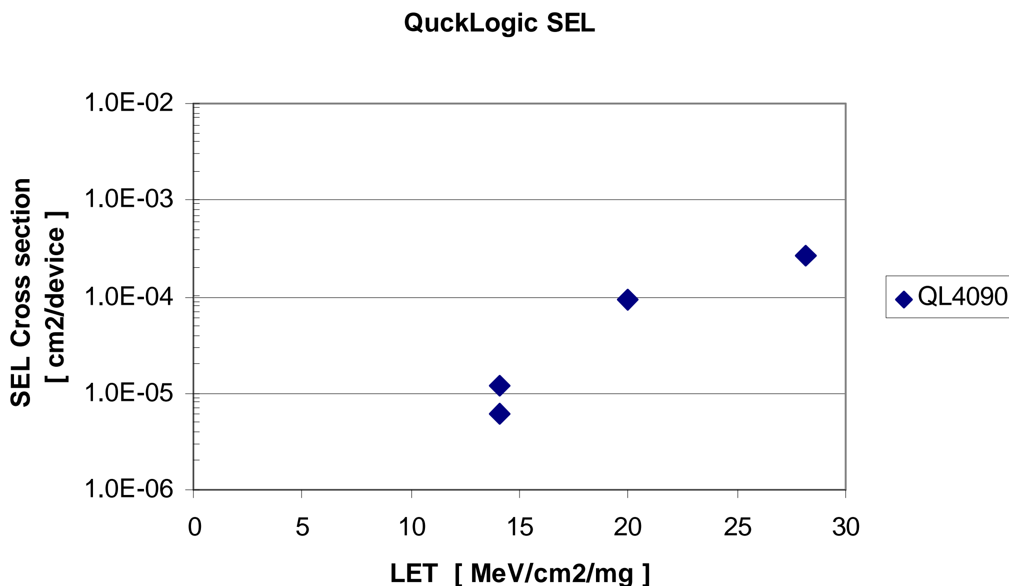

Figure 5.2 Graph showing Cross Section for Latch-up as a function of LET value for the QuickLogic QL4090 device.

Run#	Ion	LET $MeV/cm^2/mg$	Tilt	LET_{Eff} $MeV/cm^2/mg$	Flux $Ions/cm^2/s$	Fluence $Ions/cm^2$	SEL #	SEL Cross Section $cm^2/device$
41	Kr	14,1	0°	34	1000	$1,0\ 10^6$	12	$1,2\ 10^{-5}$
42	Ar	14,1	0°	14,1	5000	$1,0\ 10^6$	6	$6,0\ 10^{-6}$
43	Ar	14,1	45°	14,1	3200	$5,3\ 10^5$	49	$9,3\ 10^{-5}$
44	Ar	14,1	60°	19,9	2000	$2,0\ 10^5$	52	$2,6\ 10^{-4}$

6. CONCLUSION

None of the tested devices have survived the Latch-up tests. The Lucent and Quicklogic indicated latch-up at a LET of 14 MeV/cm^2/mg. The Lucent device showed some kind of permanent damages with increased supply currents, after a few latch-ups.

The Lattice device showed a LET threshold somewhere between 34 and 48 MeV/cm^2/mg. The ^{252}Cf tests indicated that SEU in control registers of the device might give functionality upsets. No indications of upset in the PROM storage element have been observed.

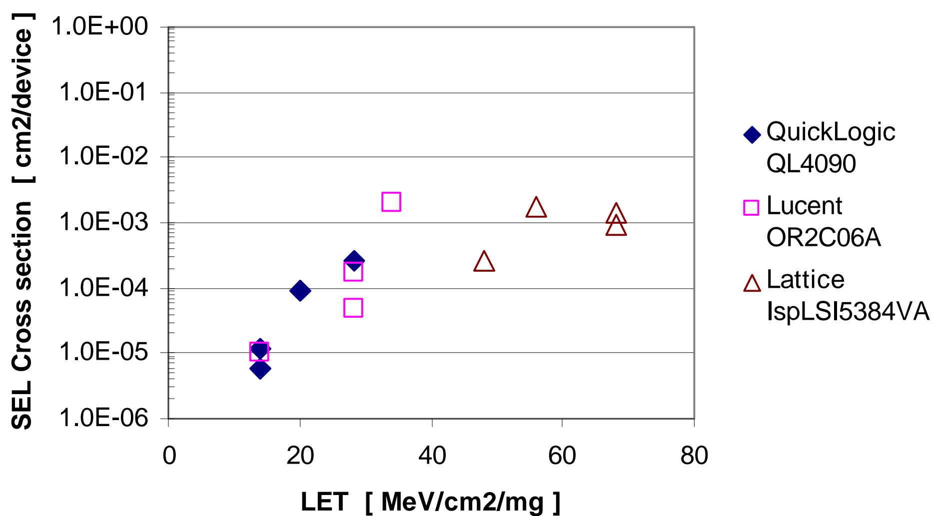

Figure 6.1 Graph showing Latch-up Cross sections as function of LET value for all three tested parts performed at the heavy ion facility at UCL, Belgium.