ESA-QCA0084S-C

RADIATION TEST REPORT

Heavy Ions Testing of

54HC08
54HC157
54HC273
54HC4040
54HC4053

from SGS Thomson

ESA Purchase Order No 171720 dated 22/07/97

European Space Agency Contract Report

The work described in this report was done under ESA contract.
Responsibility for the contents resides in the author or organization that prepared it

Ref. : HRX/97.2770
Issue : 1 Rev. -
Date : October 3, 1997

This test report has been prepared by:

Name	Function	Date	Signatures
H Constans/ C Tizon	Development Engineers	29/09/97	
FX Guerre	Study Manager	29/09/97	

ESTEC Technical Officer:

R. Harboe Sorensen

HIREX Engineering - 117, rue de la Providence - 31500 Toulouse, France
Tél. (0)5 61 80 64 89 - Fax : (0)5 61 80 65 66 - E-mail : HirexEngineering@compuserve.com
S.A. au capital de 250.000 F - RCS Toulouse B 389 715 525

TABLE OF CHANGES

Issue 1 October 3, 1997
Original issue

TABLE OF CONTENTS

PAGE

1. INTRODUCTION 5

2. APPLICABLE DOCUMENTS 5

2.1 REFERENCE DOCUMENTS 5

3. ORGANIZATION OF ACTIVITIES 5

4. DEVICE AND MANUFACTURER INFORMATION 6

5. TASK DESCRIPTION 11

5.1 PROCUREMENT OF TEST SAMPLES 11
5.2 PREPARATION OF SAMPLES 11
5.3 PREPARATION OF TEST HARDWARE AND PROGRAM 11
5.4 SAMPLES CHECK OUT 11
5.5 ACCELERATOR TEST 11

6. DESCRIPTION OF TEST FACILITIES 12

6.1 CYCLOTRON ACCELERATOR 12

7. TEST PATTERN DEFINITION FOR HEAVY ION TEST 12

7.1 54HC08 - QUAD 2-INPUT AND GATE 12
7.1.1 Test configuration 12
7.1.2 Device connection diagram 13
7.1.3 Device Test set up 14
7.2 54HC157 - QUAD 2-CHANNEL MULTIPLEXER 15
7.2.1 Test configuration 15
7.2.2 Device connection diagram 15
7.2.3 Device Test set up 16
7.3 54HC273 - OCTAL D TYPE FLIP-FLOP WITH CLEAR 17
7.3.1 Test configuration 17
7.3.2 Device connection diagram 17
7.3.3 Device Test set up 18
7.4 54HC4040 - 12-STAGE BINARY COUNTER 19
7.4.1 Test configuration 19
7.4.2 Device connection diagram 19
7.4.3 Device Test set up 20
7.5 54HC4053 - ANALOG MUX/DEMUX, TRIPLE 2 CHANNEL 21
7.5.1 Test configuration 21
7.5.2 Device connection diagram 21
7.5.3 Device Test set up 22

8. EXPERIMENTAL TEST SET-UP 23

8.1 ION BEAM SELECTION 23
8.2 FLUX RANGE 23
8.3 PARTICLE FLUENCE LEVELS 23
8.4 DOSIMETRY 23
8.5 ACCUMULATED TOTAL DOSE 23
8.6 TEST TEMPERATURE RANGE 23

9. RESULTS 23

10. CONCLUSION 27

TABLES

Table 1 - Organization of activities 5
Table 2 - Identification of the test samples 11
Table 3 - Heavy ions tests results....24

FIGURES

Figure 1 - M54HC08D - External and Internal Photos....6
Figure 2 - M54HC157D - External and Internal Photos....7
Figure 3 - M54HC273D - External and Internal Photos....8
Figure 4 - M54HC4040D - External and Internal Photos....9
Figure 5- M54HC4053D - External and Internal Photos....10
Figure 6 - Logic Gate Test Principle....13
Figure 7 - D Type Flip-Flop Test Principle....17
Figure 8 - 12 Stage Binary Counter Test Principle....19
Figure 9 - Analog Mux/Demux Test Principle....21
Figure 10 - 54HC273 SEU Test Results....26
Figure 11 - 54HC4040 SEU Test Results....26
Figure 12 - 54HC4053 SEU Test Results....27
Figure 13 -54HC4053 Scope observation of SEUs....27

APPENDICES

Appendix 1 28

1. INTRODUCTION

This report presents the results of a heavy ion Single Event Effects (SEEs) test program carried out for the XMM project on 5 types of the 54HC logic family (54HC08, 54HC157,54HC273, 54HC4040, 54HC4053).
Flight lot devices were tested at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.
The main aims of these tests were to assess the susceptibility of these 5 types to Single Event Upsets (SEUs) and Single Event Latch-ups (SELs) by heavy ion. Tests were performed in such a way that the SEU cross sections can be plotted over a wide LET range in order to allow computation of the SEU rates in XMM orbit.

This work was performed for ESA/ESTEC under P.O. No 171720 dated 20/07/97.

2. APPLICABLE DOCUMENTS

The following documents are applicable:

- XMM SOW QCA/RHS-XMM.DOC July 97 (fax dated 11 July, 97),
- Test Set-up Specification for heavy ion testing of XMM devices - Hirex Doc No HRX/97.2598 Issue 1 Rev. A dated 7 August 1997 -

2.1 REFERENCE DOCUMENTS

- SGS Thomson 54HC data sheet.
- Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
- The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

3. ORGANIZATION OF ACTIVITIES

The different tasks performed during this evaluation have been conducted in the order shown in Table 1 by the relevant company.

Table 1 - Organization of activities

Para. 5.1	Procurement of Test Samples (Hi-rel serialized devices)	ESA / SGS
Para. 5.2	Preparation of Test Samples (mounting and delidding)	Hirex
Para. 5.3	Preparation of Test Hardware and Test Program	Hirex
Para. 5.4	Samples Check out	Hirex
Para. 5.5	Accelerator Test	Hirex
	Heavy Ion Test Report	Hirex

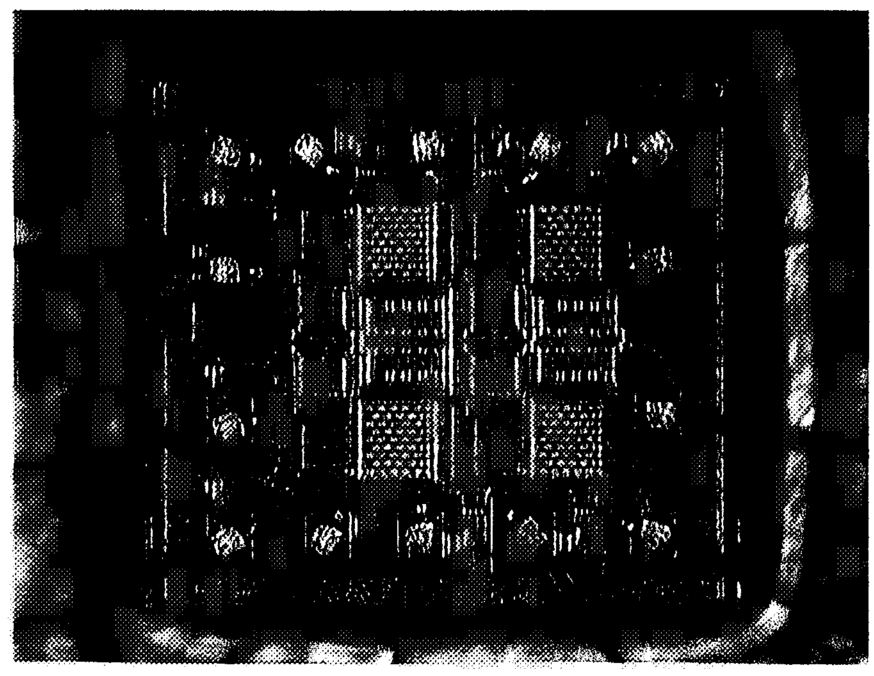
4. DEVICES AND MANUFACTURER INFORMATION

6 test samples of M54HC08D have been procured by ESA and provided to HIREX by SGS Thomson for this heavy ions evaluation test.

Description of the devices is as follows:

Part type :	M54HC08D
Manufacturer :	SGS Thomson
SGS Configuration :	PSL9766
Package :	Sidebraze 14-Pin DIL
Quality Level :	SCC B
Date Code :	9702
Serial Number :	#48, #49, #50, #51, #52, #53
Die Technology :	CMOS
Die Size :	1.3 mm x 1.2 mm approximately
Die Marking :	R008 [2]
Tested samples :	1 (#51)

Figure 1 - M54HC08D : External and Internal Photos

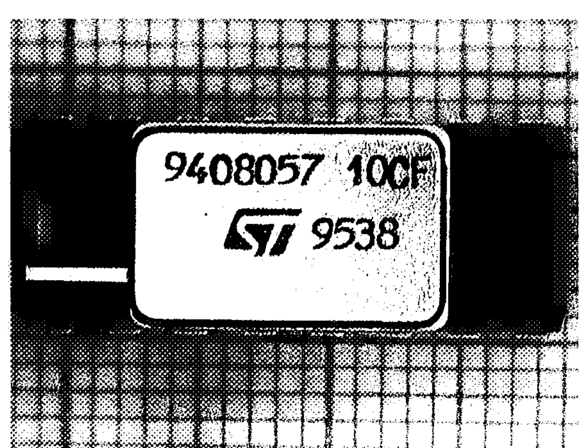


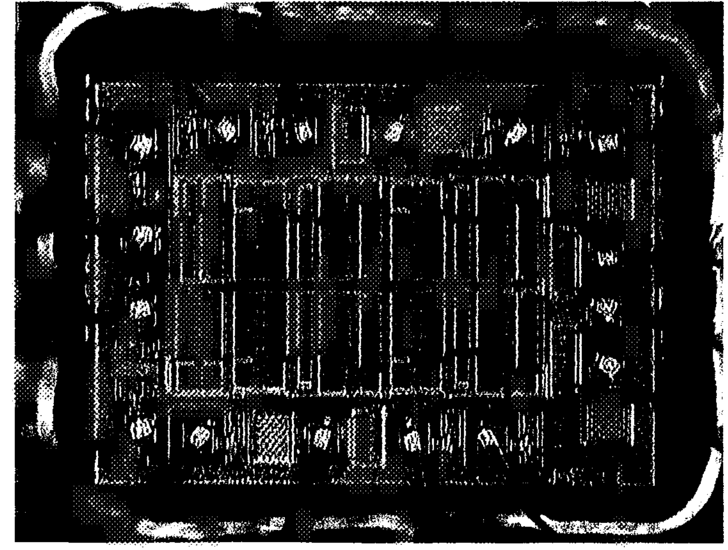
5 test samples of M54HC157D have been procured by ESA and provided to HIREX by SGS Thomson for this heavy ions evaluation test.

Description of the devices is as follows:

Part type :	M54HC157D
Manufacturer :	SGS Thomson
SGS Configuration :	PSL8177
Package :	Sidebraze 14-Pin DIL
Quality Level :	SCC B
Date Code :	9538
Serial Number :	#1, #2, #3, #4
Die Technology :	CMOS
Die Size :	1.9 mm x 1.35 mm approximately
Die Marking :	R157 $_2$
Tested samples :	1 (#1)

Figure 2 - M54HC157D : External and Internal Photos



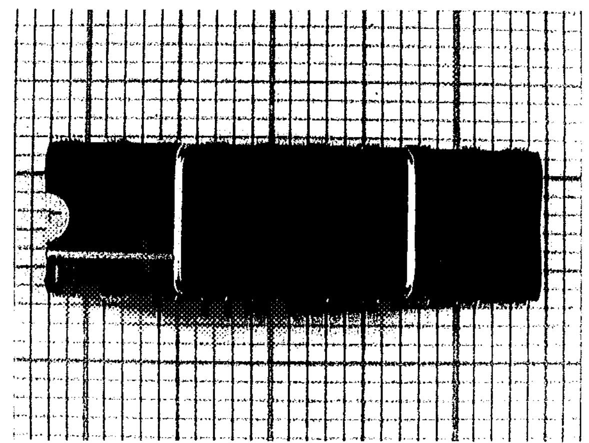


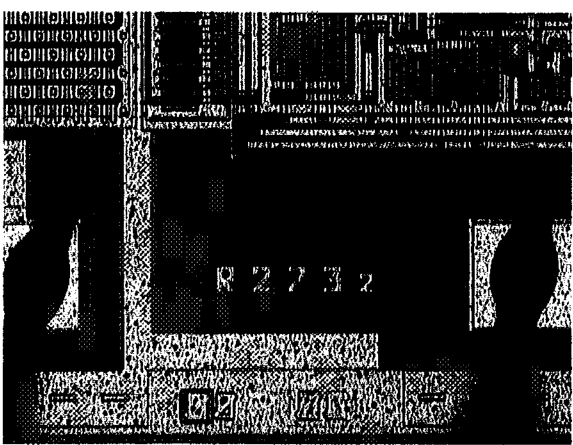
7 test samples of M54HC273D have been procured by ESA and provided to HIREX by SGS Thomson for this heavy ions evaluation test.

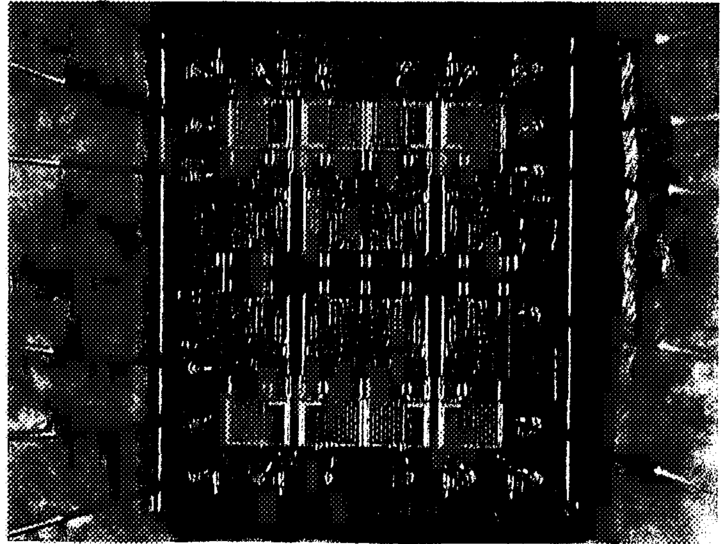
Description of the devices is as follows:

Part type :	M54HC273D
Manufacturer :	SGS Thomson
SGS Configuration :	PSL9540
Package :	Sidebraze 14-Pin DIL
Quality Level :	SCC B
Date Code :	9644A
Serial Number :	#93, #96, #97, #98, #99, #100, #101
Die Technology :	CMOS
Die Size :	1.8 mm x 2.5 mm approximately
Die Marking :	R273 2
Tested samples :	2 (#96, #97)

Figure 3 - M54HC273D : External and Internal Photos





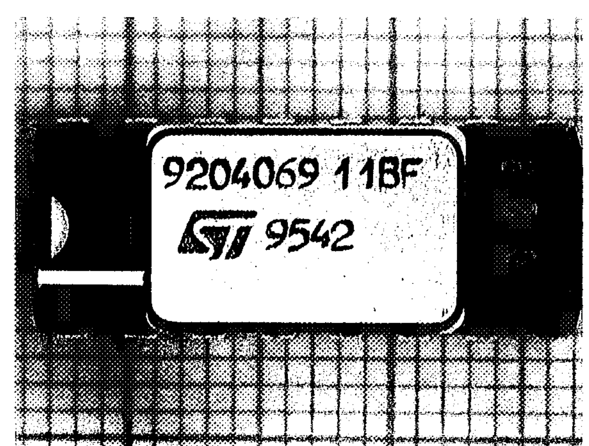


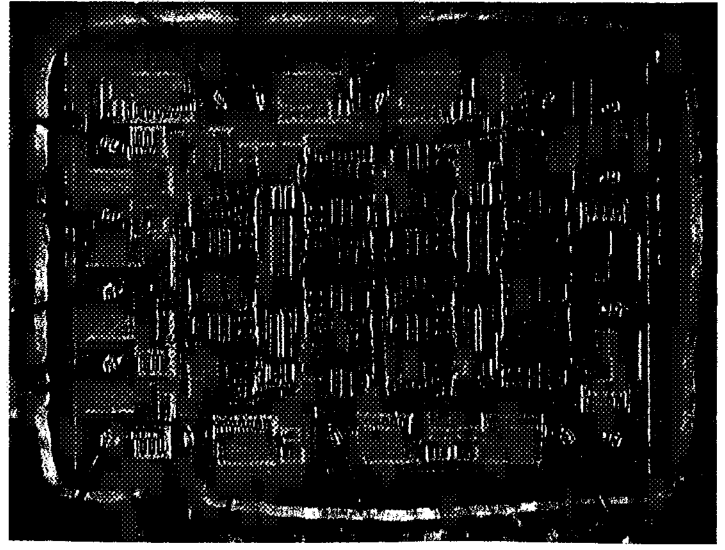
6 test samples of M54HC4040D have been procured by ESA and provided to HIREX by SGS Thomson for this heavy ions evaluation test.

Description of the devices is as follows:

Part type :	M54HC4040D
Manufacturer :	SGS Thomson
SGS Configuration :	PSL7643
Package :	Sidebraze 14-Pin DIL
Quality Level :	SCC B
Date Code :	9542
Serial Number :	#26, #27, #28, #29 / #26, #27
Die Technology :	CMOS
Die Size :	2.5 mm x 1.75 mm approximately
Die Marking :	2440 $_3$
Tested samples :	2 (#26, #27)

Figure 4 - M54HC4040D : External and Internal Photos



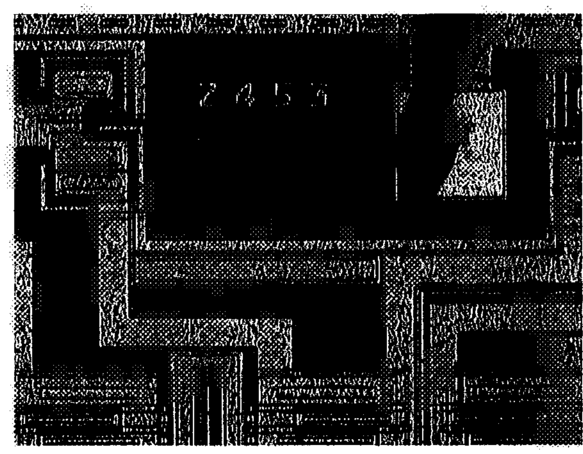


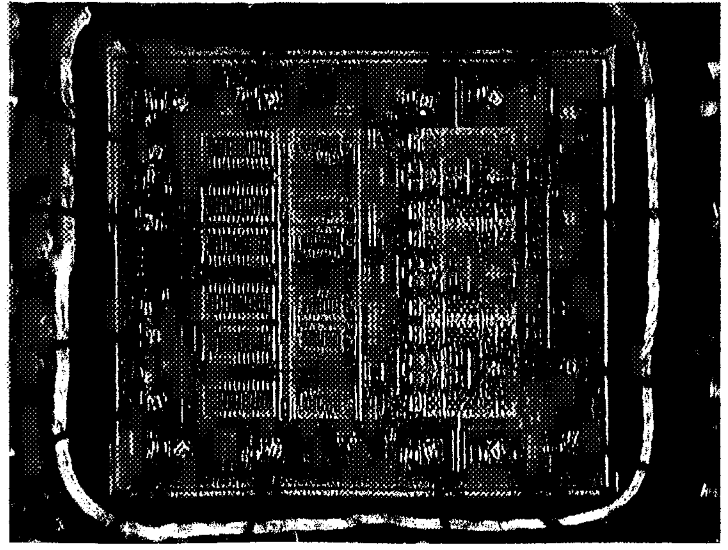
4 test samples of M54HC4053D have been procured by ESA and provided to HIREX by SGS Thomson for this heavy ions evaluation test.

Description of the devices is as follows:

Part type :	M54HC4053D
Manufacturer :	SGS Thomson
SGS Configuration :	PSL7744
Package :	Sidebraze 14-Pin DIL
Quality Level :	SCC B
Date Code :	9451
Serial Number :	#26, #27, #28, #29
Die Technology :	CMOS
Die Size :	2.1 mm x 1.8 mm approximately
Die Marking :	2453
Tested samples :	2 (#26, #27)

Figure 5 - M54HC4053D : External and Internal Photos





5. TASK DESCRIPTION

5.1 PROCUREMENT OF TEST SAMPLES

Hi-rel samples have been procured by ESA, and provided to HIREX by SGS Thomson.

Table 2 - Identification of the test samples

Type	Quantity	#s	SGS configuration	Delidded #s	
				Tested	Back-up
M54HC08D	6	48, 49, 50, 51, 52, 53	PSL9766	51	52, 53
M54HC157D	4	1, 2, 3, 4	PSL8177	1	2, 3
M54HC273D	7	93, 96, 97, 98, 99, 100, 101	PSL9540	96, 97	98, 93*
M54HC4040D	4+2	26, 27, 28, 29 + 026, 027	PSL8292+PSL7643	26, 27	28
M54HC4053D	4	26, 27, 28, 29	PSL7744	26, 27	28

* #93 has been damaged during opening: 1 bond pulled

5.2 PREPARATION OF SAMPLES

The devices delidded by HIREX lab are identified in Table 2.
1 sample has been mechanically damaged during this operation.

5.3 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and an application specific test board.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

The detailed principle of the test is described in §7, while an overall description of the in-house test equipment and interface board is given in appendix 1.

5.4 SAMPLES CHECK OUT

A functional test sequence has been performed on delidded samples to check that devices have not been degraded by the delidding operation.

5.5 ACCELERATOR TEST

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la neuve (Belgium) under HIREX Engineering responsibility.
Identification of the tested device samples is given in Table 2.

6. DESCRIPTION OF TEST FACILITIES

6.1 CYCLOTRON ACCELERATOR

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.

CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$$110\ Q^2/M$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

7. TEST PATTERN DEFINITION FOR HEAVY ION TEST

Details on both motherboard and DUT boards are provided in HRX/97.2829 document "Specific Hardware and Software Definition".

7.1 54HC08 - QUAD 2-INPUT AND GATE

7.1.1 Test configuration

As the device is combinatorial, the device is tested under static conditions

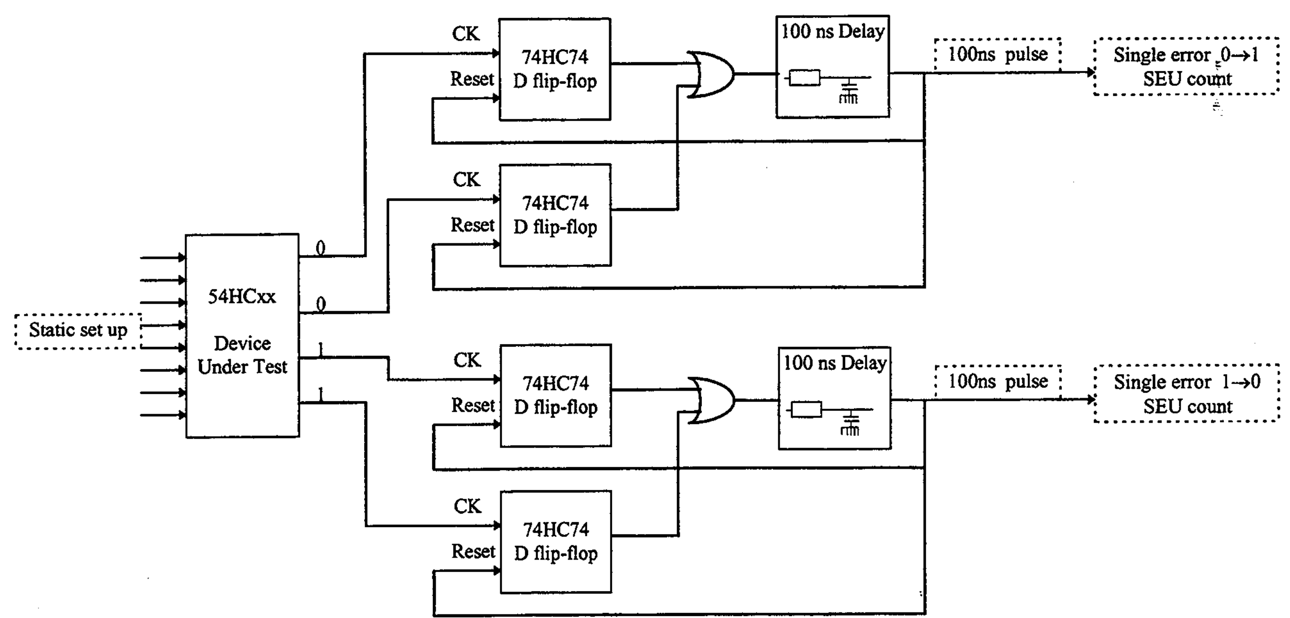
A latch of the same technology (54HC family) is used to capture the event, i.e., using the sensitivity in terms of amplitude and time which characterizes this logic family. The selection of the clock input of a D latch is representative of current design practice.

2 outputs of the DUT are set to 0 and the two other ones are set to 1.
Errors are discriminated between 0 and 1 transitions and counted separately.

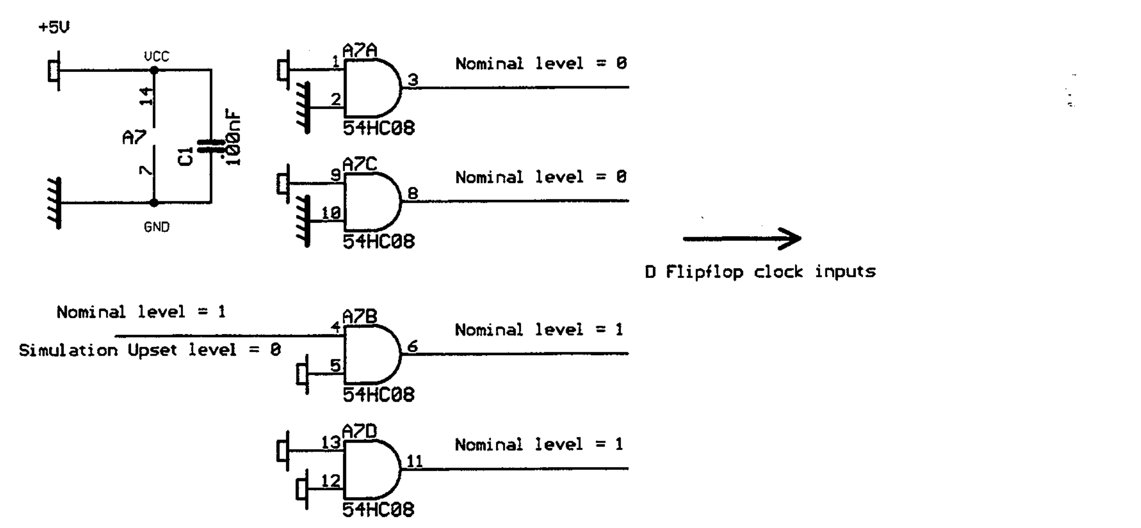
Figure 6 gives the test principle which has been used for 54HC08.

Figure 6 - Logic Gate Test Principle

54HC08 & 54HC157 Logic gate SEU test functional diagram



7.1.2 Device connection diagram



7.1.3 Device Test set up

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8	+5V	20mA	5mA	0.2mA	1mA	Vcc DUT
V_{A+}	9	+5V	20mA				Vcc D latch
V_{A-}	10						nc

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4			
CK2	4			
CK3	5			
CK4	6	0.5s	6.4µs	simulation
HOLD				

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	10ns	100ns	SEU 0→1
CT2	18	10ns	100ns	SEU 1→0
CT3	20			not used
CT4	22			not used

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

Check test

nominal state check	
upset detection check	CK4 periodically introduce a pulse at one of the logical DUT input This produces a simulated SEU 1→0 and increments the corresponding event counter CT2

Test board

Ref. : IL043-01	**Dim.** : 141mm x 50m	**slot** : DUT 1	

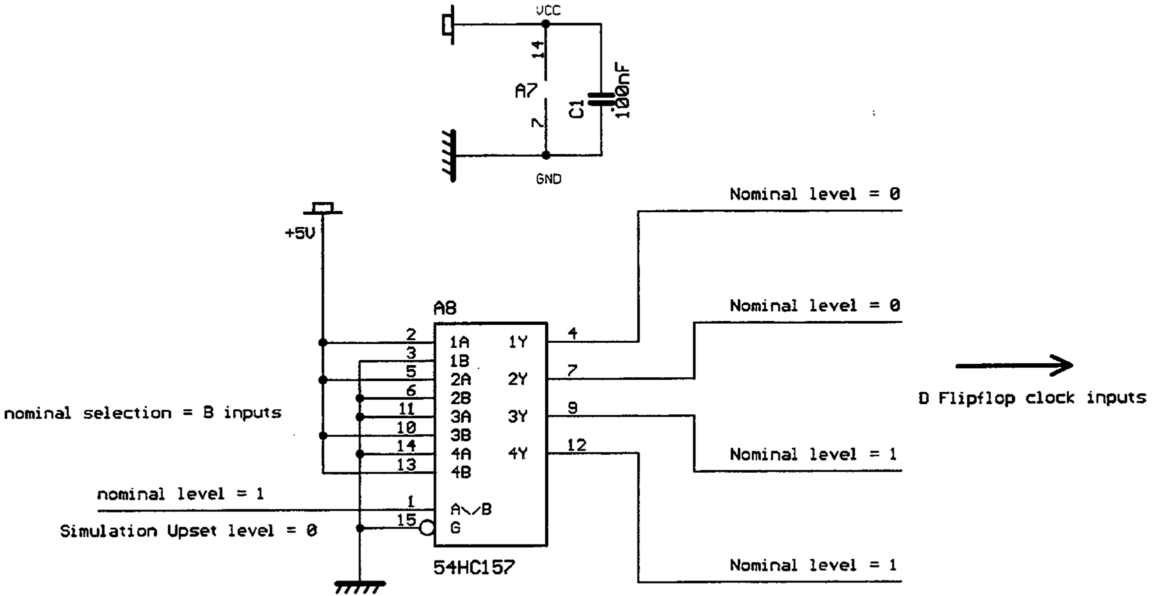
7.2 54HC157 - QUAD 2-CHANNEL MULTIPLEXER

7.2.1 Test configuration

As the device is combinatorial, the device is tested under static conditions.

The same test principle than for 54HC08 has been used (see Figure 6 - Logic Gate Test Principle).

7.2.2 Device connection diagram



7.2.3 Device Test set up

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8	+5V	20mA	5mA	3.2mA	2mA	Vcc DUT
V_{A+}	9	+5V	20mA		12mA	5mA	Vcc D latch
V_{A-}	10						nc

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4	4MHz	50%	DUT clock
CK2	4			
CK3	5			
CK4	6	0.5s	12µs	simulation
HOLD				

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	250ns	100ns	Single SEU 1→ 0
CT2	18	250ns	100ns	Multiple SEU 1→ 0
CT3	20	250ns	100ns	Multiple SEU 0→ 1
CT4	22	250ns	100ns	Single SEU 0→ 1

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

Check test

nominal state check	
upset detection check	CK4 periodically forces input data bit DO to 0 This produces a simulated single SEU 1 → 0 and increments the corresponding event counter CT2

Test board

Ref. : IL043-03	**Dim.** : 141mm x 50m	**slot** : DUT 2	

7.3 54HC273 - OCTAL D TYPE FLIP-FLOP WITH CLEAR

7.3.1 Test configuration

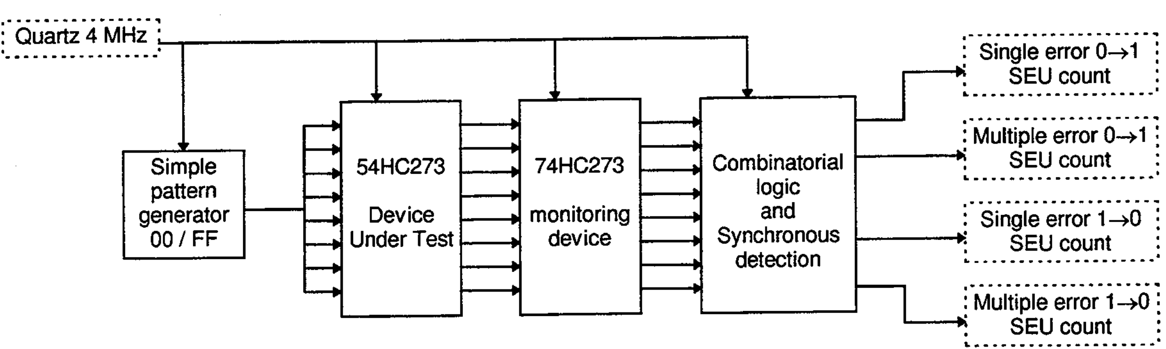
It has been decided to test the device in the way it is currently used, i. e. as a latch of dynamic data :
A permanent flux of data (00 or FF) goes thru the DUT at a frequency of 4 MHz. These data then go to the next circuit which is the same type of device (54HC273) and a logic comparison with the input pattern is performed synchronously.
The following different errors can then be directly detected and counted :

- single error 0 to 1
- multiple error 0 to 1
- single error 1 to 0
- multiple error 1 to 0

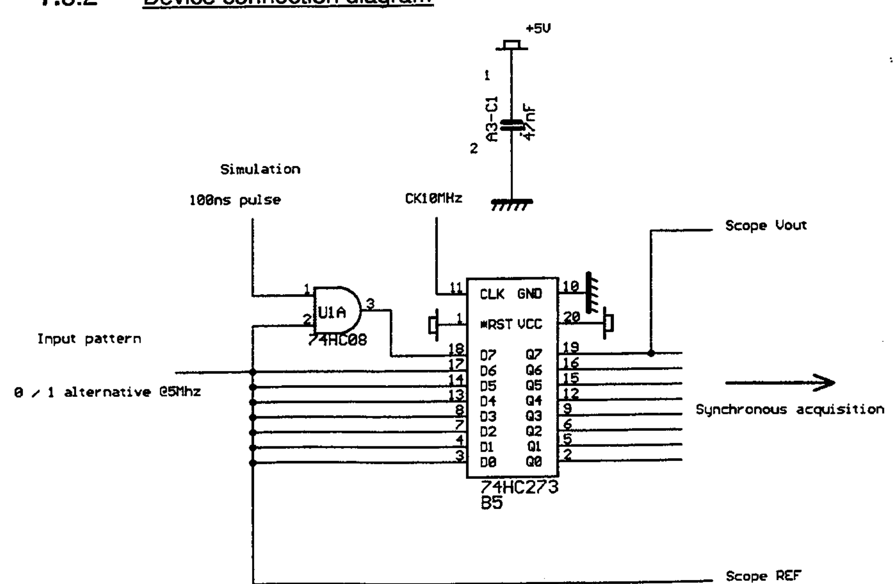
The acquisition of an error is done by a device (54HC273) whose performance characteristics are representative of the 54HC family.

Figure 7 - D Type Flip-Flop Test Principle

54HC273 Octal D flip-flop SEU test functional diagram



7.3.2 Device connection diagram



7.3.3 Device Test set up

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8	+5V	20mA	5mA	3.2mA	2mA	Vcc DUT
V_{A+}	9	+5V	20mA		12mA	5mA	Vcc D latch
V_{A-}	10						nc

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4	4MHz	50%	DUT clock
CK2	4			
CK3	5			
CK4	6	0.5s	12µs	simulation
HOLD				

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	250ns	100ns	Single SEU 1→ 0
CT2	18	250ns	100ns	Multiple SEU 1→ 0
CT3	20	250ns	100ns	Multiple SEU 0→ 1
CT4	22	250ns	100ns	Single SEU 0→ 1

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

Check test

nominal state check	
upset detection check	CK4 periodically forces input data bit DO to 0 This produces a simulated single SEU 1→ 0 and increments the corresponding event counter CT2

Test board

Ref. : IL043-03	**Dim.** : 141mm x 50m	**slot :** DUT 2	

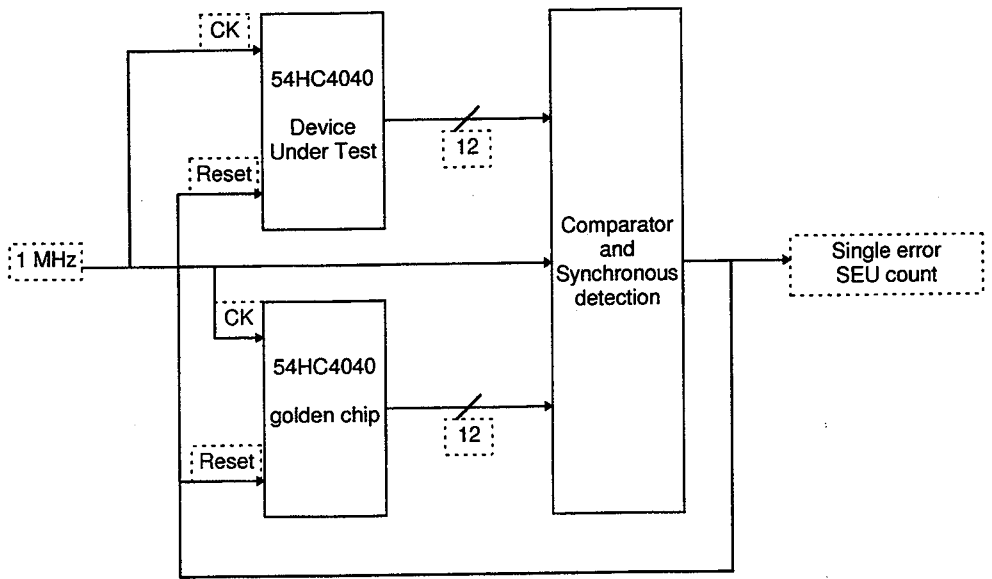
7.4 54HC4040 - 12-STAGE BINARY COUNTER

7.4.1 Test configuration

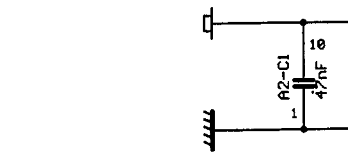
The test principle is based on golden chip.
A comparison of the 12-bits output word of both DUT and golden device, is performed synchronously at each clock period.
Each time a difference is detected, an error is counted and both devices are reset.
Working frequency is fixed at 1 MHz to comply with ripple counter total delay.

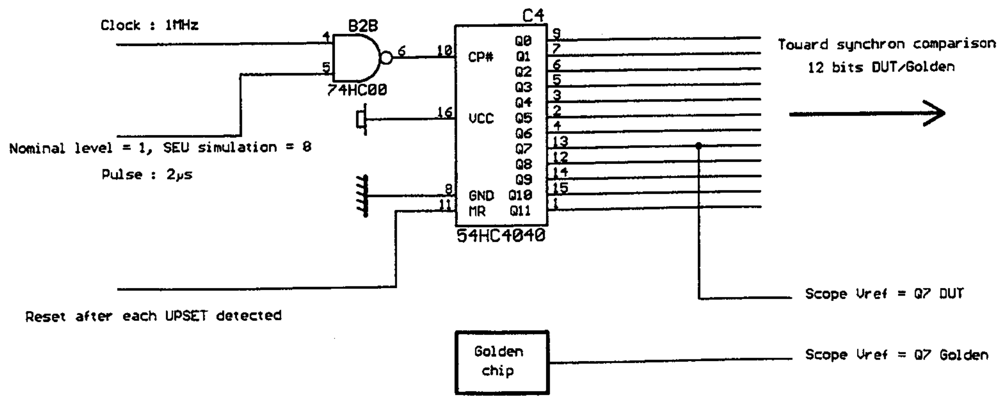
Figure 8 - 12 Stage Binary Counter Test Principle

54HC4040 12 bit ripple counter SEU test functional diagram



7.4.2 Device connection diagram





7.4.3 Device Test set up

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8	+5V	20mA	5mA	0.2mA	1mA	Vcc DUT
V_{A+}	9	+5V	20mA				Vcc control
V_{A-}	10						nc

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4			
CK2	4	1 MHz	50%	DUT clock
CK3	5			
CK4	6	0.5s	12µs	simulation
HOLD				

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	250ns	100ns	SEU
CT2	18			
CT3	20			
CT4	22			

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

Check test

nominal state check	
upset detection check	CK4 periodically interrupt during a few cycles the golden chip clock. This produces an error on the 12 bits count and increments the event counter CT1

Test board

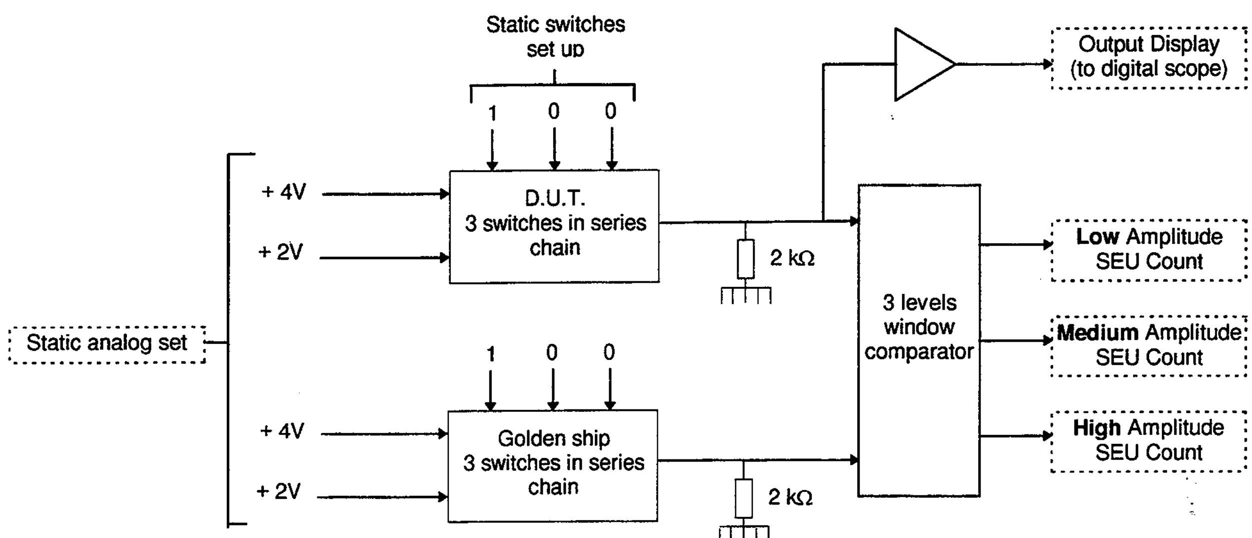
Ref. : IL043-05	**Dim.** : 141mm x 50m	**slot :** DUT 3	

7.5 54HC4053 - ANALOG MUX/DEMUX, TRIPLE 2 CHANNEL

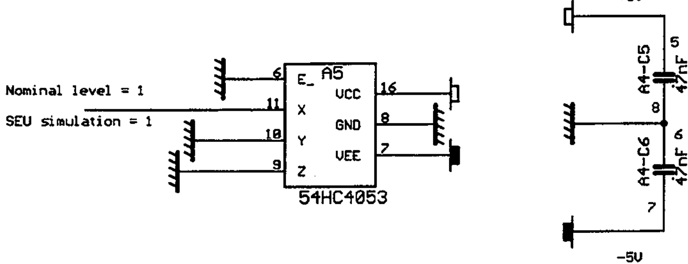
7.5.1 Test configuration

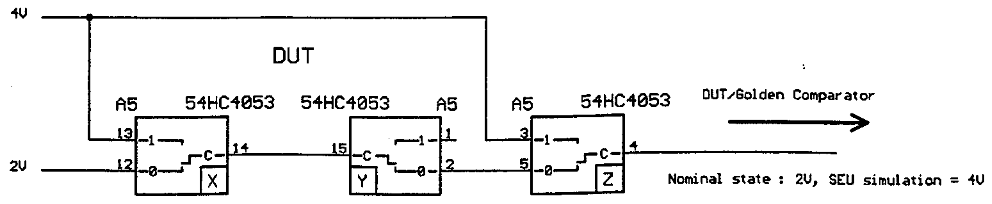
The three switches are chained in series, to form a 2 input multiplexer, and the output voltage of the chain is compared with the awaited voltage thanks to a fast analog comparator. This allows for the counting of three different amplitude errors (low, medium and high).Golden chip method allows accurate output level comparison, because voltage level is dependent of "on state " switches resistor.

Figure 9 - Analog Mux/Demux Test Principle



7.5.2 Device connection diagram





7.5.3 Device Test set up

Appendix 1 gives a generic description of the test set-up with the meaning of the different symbols of the parameters specified here below.

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8	+5V	20mA	18mA	1.5mA	0.4mA	V+ resistor divider
V_{A+}	9	+5V	20mA	5mA	≈0mA	0.4mA	V+ DUT & Golden
V_{A-}	10	-5V	20mA	20mA	≈0mA	0.4mA	V+ DUT & Golden

Latch Up timing

T_{wait}	T_{off}	$T_{set up}$ x 3	T_{LU}
20ms	100ms	10ms	150ms

Clocks & commands

signal	module	period	pulse width	function
CK1	4			not used
CK2	4			not used
CK3	5			not used
CK4	6	420ms	12.8µs	simulation

Event counters

signal	module	pulse min.	Hold Off	function
CT1	16	50ns	2µs	windows analog comparator SMALL absolute amplitude > 5mV
CT2	18	50ns	2µs	windows analog comparator MEDIUM absolute amplitude > 78mV
CT3	20	50ns	2µs	windows analog comparator LARGE absolute amplitude > 1.25V
CT4	22			not used

Oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref	5MHz	DUT output	1/2 **1.25V ⇔ 2.5V**	800mV
Vout	50MHz	DUT output	1/2 **1.25V ⇔ 2.5V**	800mV

Functional test

nominal state check	output ≈ 800mV
upset detection check	CK4 periodically change one of the switch state. This produces a simulated LARGE SEU with an amplitude of 0.8V + ≈1.5V and increments the corresponding event counter CT3

Test board

Ref. : IL043-11	**Dim.** : 141mm x 50m	**slot :** DUT 4	

8. EXPERIMENTAL TEST SET-UP

8.1 ION BEAM SELECTION

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.

Table 3 provides the ions which were used to determine the LET threshold and the asymptotic cross section within the LET range for this heavy ion characterization. In addition this table includes the ion energy, the LET, the range and the tilt angle if any.

8.2 FLUX RANGE

Particle flux was comprised between 1. x10E3 and 4. x10E4 ions/cm²/sec under normal operations (tilt 0°).

8.3 PARTICLE FLUENCE LEVELS

Fluence level was comprised between 1 x10E5 and 5 x10E5 ions/cm² under normal operations (tilt 0°).

8.4 DOSIMETRY

The current UCL Cyclotron dosimetry system and procedures were used.

8.5 ACCUMULATED TOTAL DOSE

The equivalent total dose (rad(Si)) received by each device under test is given in Table 3.

8.6 TEST TEMPERATURE RANGE

All the tests performed were conducted at ambient temperature.

9. RESULTS

All tests results are given in Table 3 hereafter for the 5 types. All samples tested for the 5 types have received an equivalent dose below 5 krads.

No SEL has been seen during the whole set of runs.

54HC08 and 54HC157 experienced no upset for LETs up to 111 MeV/mg/cm².

54HC273: few upsets have been observed and heavy ion SEE results are plotted as SEU cross section (cm²/device) versus LET for the total number of errors in Figure 10. The asymptotic cross section is about 3.5 E-5 cm² with an LET threshold between 34 and 48 MeV/mg/cm². Most of the errors were 0 to 1 transitions.

54HC4040: Again, few upsets have been observed and heavy ion SEE results are plotted as SEU cross section (cm²/device) versus LET for the total number of errors in Figure 11. The asymptotic cross section is about 3.5 E-5 cm² with an LET threshold between 48 and 55 MeV/mg/cm².

54HC4053: Only "small" transient errors (5mV-78 mV) have been observed and heavy ion SEE results are plotted as SEU cross section (cm²/device) versus LET for the total number of errors in Figure 12. The asymptotic cross section is about 2.5 E-4 cm² with an LET threshold between 28 and 34 MeV/mg/cm². A typical waveform is shown in Figure 13.

Table 3 - Heavy ions tests results

Run #	Type	S/N	Ion	Energy	LET	Tilt Angle	Range Effective	LET Effective	Time	Flux	Fluence	SEU's Error type (*) 1	2	3	4	Total	Cross Section	Dose /run	Cumulative dose /SN	Comments
				MeV	Mev/mg/cm²	°	µm (Si)	Mev/mg/cm²	s	p/cm²/s	p/cm²						cm²	rads(Si)	rads(Si)	
62	54HC08	051	Xe	459	55,9	60	21,5	111,80	1343	5,59E+02	696305	0	0			0		1,25E+03	2,51E+03	
63	54HC08	051	Xe	459	55,9	60	21,5	111,80	575	5,59E+02	300000	0	0			0		5,37E+02	3,05E+03	
51	54HC08	051	Xe	459	55,9	45	30,4	79,05	1206	7,91E+02	1000825	0	0			0		1,27E+03	1,27E+03	
47	54HC157	1	Xe	459	55,9	60	21,5	111,80	360	5,59E+02	501563	0	0			0		8,97E+02	1,98E+03	
38	54HC157	1	Xe	459	55,9	45	30,4	79,05	1009	7,91E+02	708527	0	0			0		8,96E+02	1,08E+03	
37	54HC157	1	Xe	459	55,9	0	43,0	55,90	184	1,12E+03	206723	0	0			0		1,85E+02	1,85E+02	
46	54HC273	96	Xe	459	55,9	60	21,5	111,80	407	5,59E+02	501162	17	0	0	2	19	3,79E-05	8,96E+02	2,16E+03	
39	54HC273	96	Xe	459	55,9	45	30,4	79,05	1170	7,91E+02	1000712	6	0	0	0	6	6,00E-06	1,27E+03	1,27E+03	
48	54HC273	96	Xe	459	55,9	0	43,0	55,90	122	1,12E+03	500404	7	0	0	0	7	1,40E-05	4,48E+02	2,61E+03	
162	54HC273	96	Kr	316	34	45	30,4	48,08	150	1,30E+03	1011294	9	0	0	0	9	8,90E-06	7,78E+02	3,39E+03	
163	54HC273	96	Kr	316	34	0	43,0	34,00	196	1,84E+03	1001645	0	0	0	0	0		5,45E+02	3,93E+03	
58	54HC273	97	Xe	459	55,9	60	21,5	111,80	844	5,59E+02	500467	11	0	0	5	16	3,20E-05	8,95E+02	2,04E+03	
52	54HC273	97	Xe	459	55,9	45	30,4	79,05	724	7,91E+02	905753	11	0	0	0	11	1,21E-05	1,15E+03	1,15E+03	
59	54HC273	97	Xe	459	55,9	0	43,0	55,90	518	1,12E+03	500052	9	0	0	0	9	1,80E-05	4,47E+02	2,49E+03	
158	54HC273	97	Kr	316	34	45	30,4	48,08	381	1,30E+03	1000632	1	0	0	0	1	9,99E-07	7,70E+02	3,26E+03	

*Error types:

1	54HC08 &54HC157	0 to 1	54HC273	0 to 1 single
2	54HC08 &54HC157	1 to 0	54HC273	0 to 1 multiple
3	54HC08 &54HC157	not used	54HC273	1 to 0 single
4	54HC08 &54HC157	not used	54HC273	1 to 0 multiple

Table 3 - Heavy ions tests results (Cont'd)

Run #	Type	S/N	Ion	Energy	LET	Tilt Angle	Range Effective	LET Effective	Time	Flux	Fluence	SEU's Error type (*)				Total	Cross Section	Dose /run	Cumulative dose /SN	Comments
				MeV	Mev/mg/cm²	°	µm (Si)	Mev/mg/cm²	s	p/cm²/s	p/cm²						cm²	rads(Si)	rads(Si)	
45	54HC4040	026	Xe	459	55,9	60	21,5	111,80	353	5,59E+02	500798	20				20	3,99E-05	8,96E+02	2,21E+03	
40	54HC4040	026	Xe	459	55,9	45	30,4	79,05	905	7,91E+02	640660	13				13	2,03E-05	8,10E+02	8,10E+02	
41	54HC4040	026	Xe	459	55,9	45	30,4	79,05	428	7,91E+02	400622	8				8	2,00E-05	5,07E+02	1,32E+03	
49	54HC4040	026	Xe	459	55,9	0	43,0	55,90	113	1,12E+03	502056	3				3	5,98E-06	4,49E+02	2,66E+03	
164	54HC4040	026	Kr	316	34	45	30,4	48,08	133	1,30E+03	1003728	0				0		7,72E+02	3,43E+03	
57	54HC4040	027	Xe	459	55,9	60	21,5	111,80	273	5,59E+02	500804	18				18	3,59E-05	8,96E+02	2,54E+03	
53	54HC4040	027	Xe	459	55,9	45	30,4	79,05	292	7,91E+02	299505	4				4	1,34E-05	3,79E+02	3,79E+02	
54	54HC4040	027	Xe	459	55,9	45	30,4	79,05	626	7,91E+02	1001626	13				13	1,30E-05	1,27E+03	1,65E+03	
60	54HC4040	027	Xe	459	55,9	0	43,0	55,90	500	1,12E+03	500843	0				0		4,48E+02	2,99E+03	
159	54HC4040	027	Kr	316	34	45	30,4	48,08	199	1,30E+03	1003354	0				0		7,72E+02	3,76E+03	
44	54HC4053	026	Xe	459	55,9	60	21,5	111,80	310	5,59E+02	501417	75	0	0		75	1,50E-04	8,97E+02	2,15E+03	
42	54HC4053	026	Xe	459	55,9	45	30,4	79,05	833	7,91E+02	486056	135	0	0		135	2,78E-04	6,15E+02	6,15E+02	
43	54HC4053	026	Xe	459	55,9	45	30,4	79,05	437	7,91E+02	502085	95	0	0		95	1,89E-04	6,35E+02	1,25E+03	
50	54HC4053	026	Xe	459	55,9	0	43,0	55,90	115	1,12E+03	500128	78	0	0		78	1,56E-04	4,47E+02	2,59E+03	
165	54HC4053	026	Kr	316	34	45	30,4	48,08	317	1,30E+03	1003492	93	0	0		93	9,27E-05	7,72E+02	3,37E+03	
166	54HC4053	026	Kr	316	34	0	43,0	34,00	224	1,84E+03	1003177	7	0	0		7	6,98E-06	5,46E+02	3,91E+03	
195	54HC4053	026	Ar	150	14,1	60	21,0	28,20	479	2,22E+03	1000097	0	0	0		0		4,51E+02	4,68E+03	
194	54HC4053	026	Ar	150	14,1	45	29,7	19,94	342	3,13E+03	1000694	0	0	0		0		3,19E+02	4,23E+03	
56	54HC4053	027	Xe	459	55,9	60	21,5	111,80	169	5,59E+02	501793	121	0	0		121	2,41E-04	8,98E+02	2,17E+03	
55	54HC4053	027	Xe	459	55,9	45	30,4	79,05	181	7,91E+02	1004227	258	0	0		258	2,57E-04	1,27E+03	1,27E+03	
61	54HC4053	027	Xe	459	55,9	0	43,0	55,90	395	1,12E+03	500617	138	0	0		138	2,76E-04	4,48E+02	2,62E+03	
160	54HC4053	027	Kr	316	34	45	30,4	48,08	93	1,30E+03	1006966	120	0	0		120	1,19E-04	7,75E+02	3,39E+03	
161	54HC4053	027	Kr	316	34	0	43,0	34,00	67	1,84E+03	1007578	62	0	0		62	6,15E-05	5,48E+02	3,94E+03	
196	54HC4053	027	Ar	150	14,1	60	21,0	28,20	333	2,22E+03	1002140	0	0	0		0		4,52E+02	4,39E+03	

*Error types:

1	54HC4040	at least 1 bit error	54HC4053	small
2	54HC4040	not used	54HC4053	medium
3	54HC4040	not used	54HC4053	large
4	54HC4040	not used	54HC4053	not used

Figure 10 - 54HC273 SEU Test Results

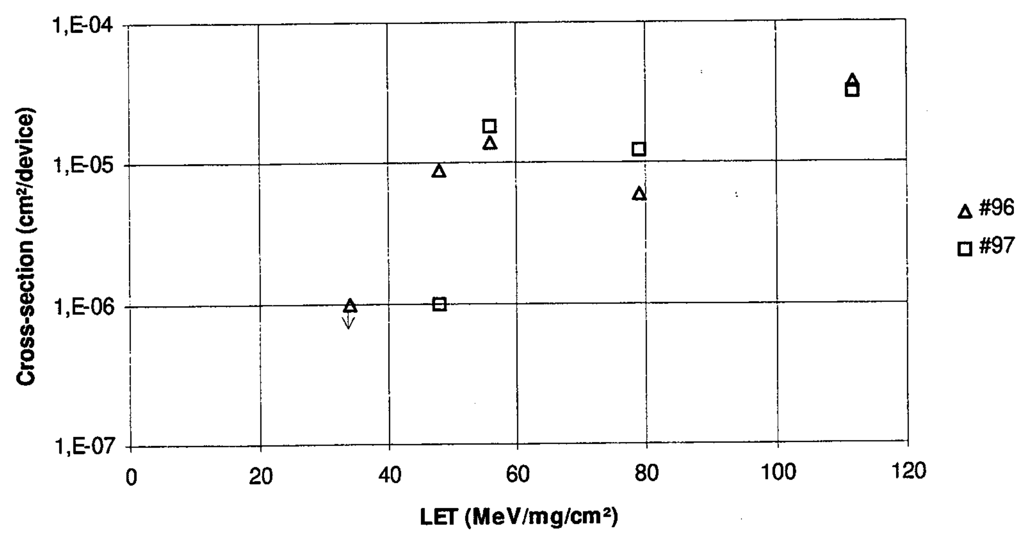


Figure 11 - 54HC4040 SEU Test Results

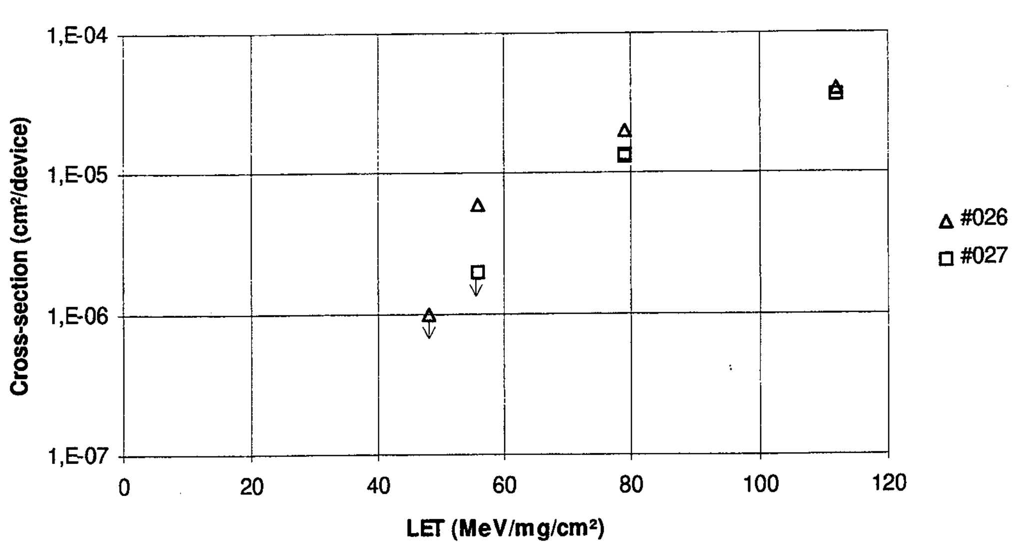
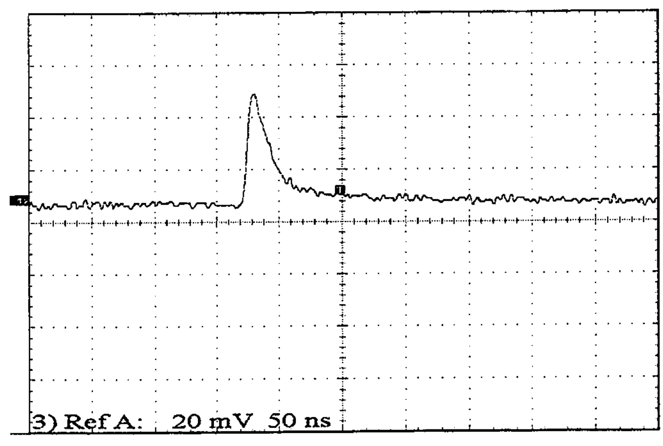


Figure 12 - 54HC4053 SEU Test Results

54HC4053 SEU Tests Results
(Only transients w ith an amplitude betw een 5 mV and 78 mV have been detected)

Cross-section (cm²/device)
1,E-03
1,E-04
1,E-05
1,E-06
1,E-07
0 20 40 60 80 100 120
LET (MeV/mg/cm²)
△ #026
□ #027

Figure 13 -54HC4053 Scope observation of SEUs



Typical event waveform

(Observed signal to be multiplied by a factor of 2 to obtain the actual amplitude)

10. CONCLUSION

SEU test have been conducted on 5 54HC functions from SGS Thomson, using the heavy ions available at the University of Louvain facility.

No SEL has been detected all the different runs performed on the five types.

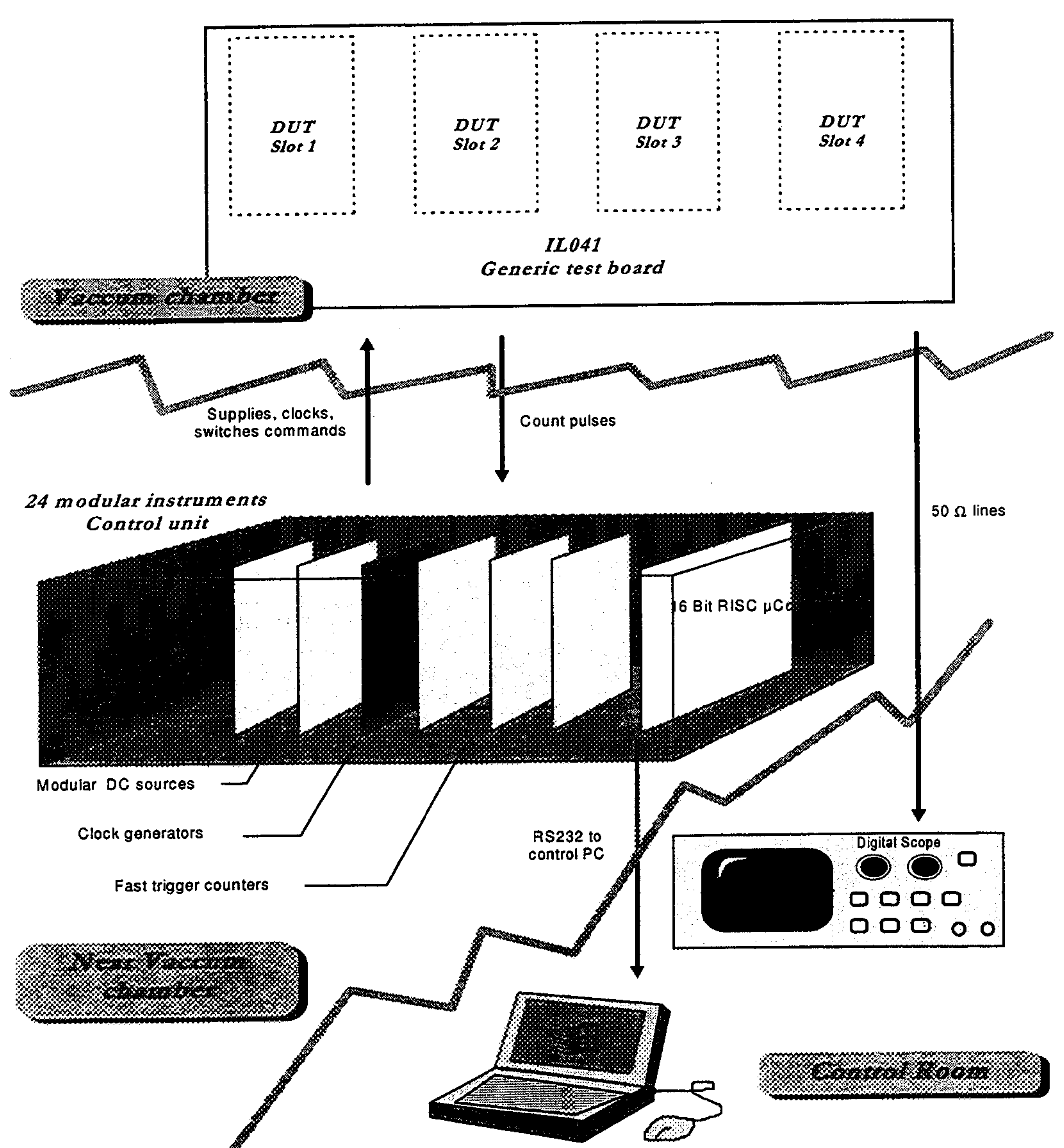
54HC08 an 54HC157 experienced no upset for LETs up to 111MeV/mg/cm².
For the three other devices (54HC4040, 54HC4053 and 54HC273) the susceptibility to SEE was obtained through the cross section versus LET curve and was found to be quite low.
With these results, upset predictions on XMM orbit, can be performed.

Appendix 1

Test set-up

The complete test equipment is constituted of:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 4 devices
- A digital oscilloscope to store analog upset waveform.

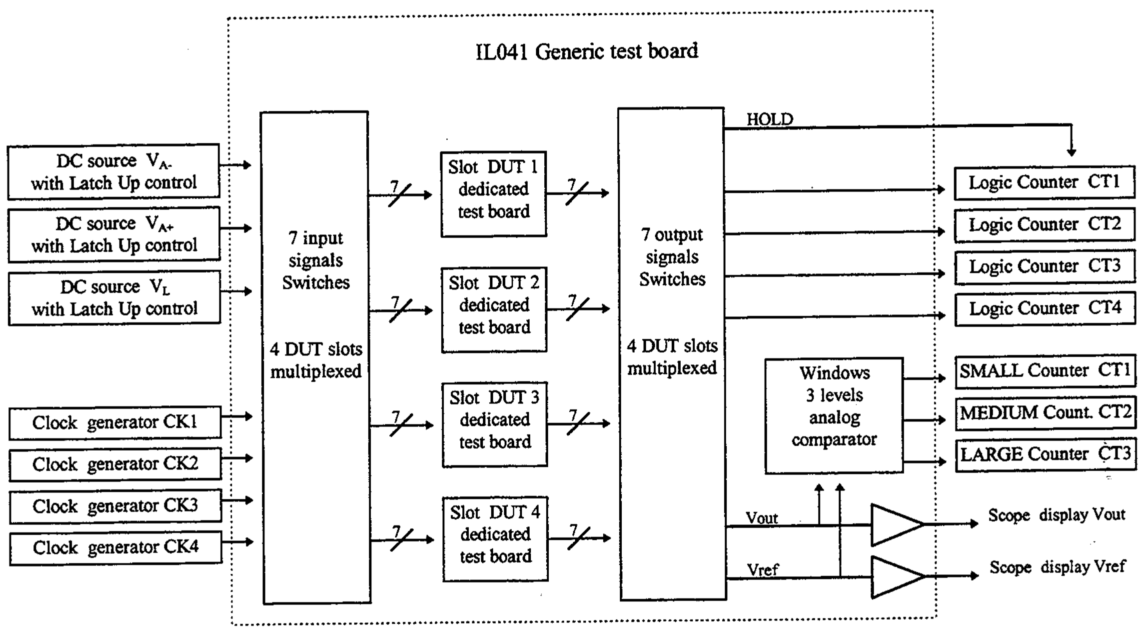


Mother board description (ref. IL041)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each DUT board slot , the following signals can be considered:

- seven inputs signals
    - 3 programmable power supplies
    - 4 programmable clocks
- seven output signals
    - 4 logic counting signals
    - 2 analog signals : DUT output and Ref . output
    - 1 HOLD signal which can inhibit temporarily the counters.

- Each device needs a dedicated plug-in test board compatible with IL041 mother board.
- IL041 board has been designed to comply with Louvain Test facilities .
- The number of slots is limited to four
  Operation is multiplexed and only one slot is powered at one time.



DUT Test board description

The device under test is mounted on a specific board support which is plugged onto the motherboard.
Mechanical outlines : 141 mm x 50 mm , wrapping or printed circuit board with two 20 pins connectors.
According to test set up and device operating conditions, the test board can accept the mounting of :

- The DUT package with beam positioning constraints (unique for Louvain facilities)
- The golden chip
- The pattern generator
- any interface circuit such as buffer, latches ...
- a standalone micro controller if necessary...

Note : beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

Three Windows analog comparator

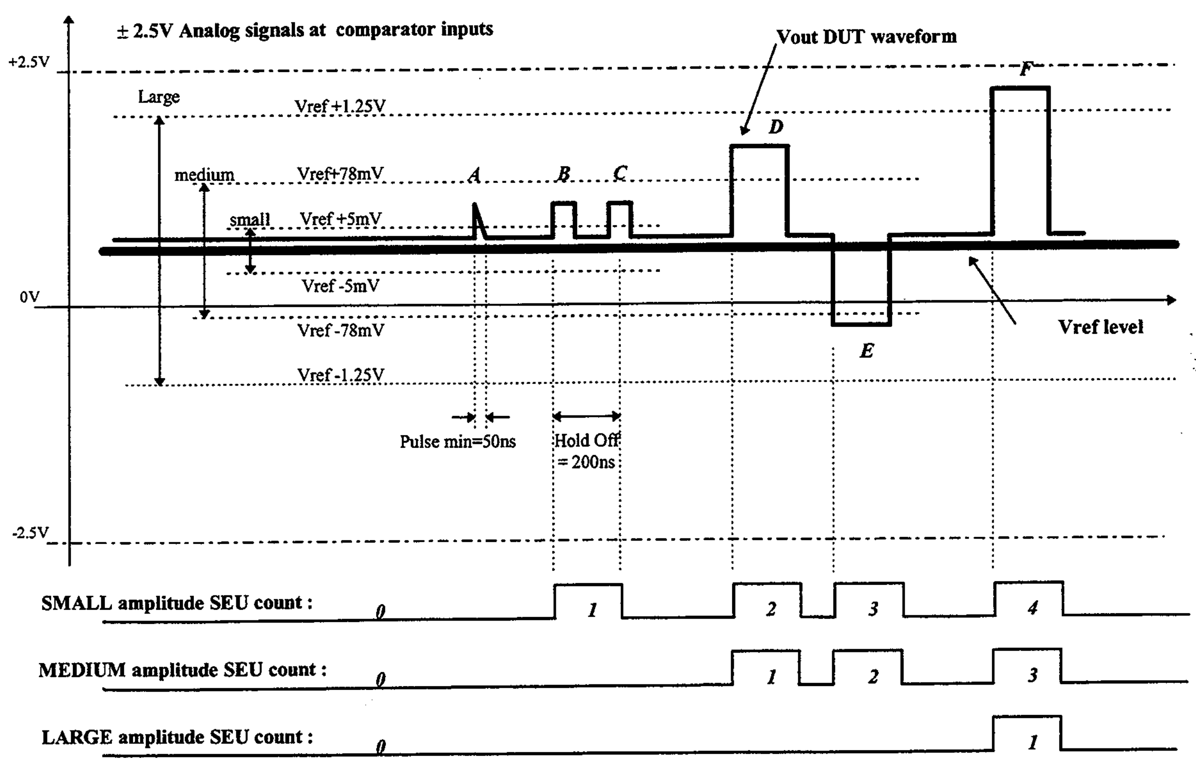
Applications :
Single analog output devices, including DAC, can be monitored with a generic 3 windows fast comparator associated to 3 counter modules .

Test principle :
Each window uses pre-defined levels centered around the awaited working point :

- The SMALL window uses the lowest levels compatible with the hardware limitation (offset, noise ...)
- The LARGE window is for counting major DUT output perturbations : Vout max /2 or DAC MSB...
- The MEDIUM window has been defined using a geometric progression between SMALL and LARGE

To illustrate how it works, the here after figure gives an example of timing diagram :
Both DUT and Ref. working point can vary within the ±2.5V allowed input range (+1V in the example).
6 transient pulses can be seen on the DUT Vout record :

- Pulse A will not be counted as its width is shorter than Pulse min parameter
- Pulse B and C : Only B will be counted as the time between B and C is less than the Hold Off parameter (this prevents of multiple counting in case of large degraded transient)
- Pulse D and E : Both pulses will be counted as the comparator works whatever polarity.
- Pulse F is an example of large event . It can be noticed that a large event is also counted as a medium and a small as well.



Interest :
The use of this principle allows for straightforward analysis of the test data, at run time. So, it is easy to react and adjust the beam conditions to obtain proper data. When preparing the report, it also shortens the subsequent run recorded data analysis exercise.
Lastly, using 3 different levels at a time, reduces the number of runs needed for the device characterization

ADC converters :
The here above method can also be transposed to the test of ADCs. In that case, the 3 windows analog comparator is replaced by a simple standalone micro controller witch execute the same windowing operation by soft.

Working point variation and HOLD function :
This window comparison is compatible with low frequency working point variation (few Hertz) . This is particularly useful with ADC and DAC devices : Saw tooth input pattern can be used to test the device with a uniform digital code distribution. In that case, the input saw tooth is rather a stair case signal. HOLD function allows to inhibit comparison and counting each time the pattern changes.

Test signals definition

Supplies

signal	module	U_{Reg}	I_{max}	I_{LU}	I_{nom}	I_{Δ}	function
V_L	8						
V_{A+}	9						
V_{A-}	10						

- **signals** V_L , V_{A+} & V_{A-} are 3 DC sources with constant voltage / current characteristic, software monitoring, Latch Up threshold detection, delayed start & stop triggering
- **module :** Slot position used by hardware & software control system
- U_{Reg} **:** DC source set up for constant voltage operation
- I_{max}**:** DC source set up for constant current operation, useful on large DUT latch up or failure
- I_{LU}**:** software Latch Up detection current threshold
- I_{nom}**:** nominal current when DUT operates properly
- I_{Δ}**:** minimum current measurement change required for event memory write
- **function:** DC source assignment (DUT or test board auxiliary device)

Latch Up timing

T_{wait}	T_{off}	$T_{set\ up}$ x 3	T_{LU}

- T_{wait} Sustaining Latch Up time (delay between detection and DC sources shut down)
- T_{off} Off state duration
- $T_{set\ up}$ **x 3** Restart triggering Delay between the different internal sequential levels
- T_{LU} Total latch Up sequence duration

clocks & commands

signal	module	period	pulse width	function
CK1	4			
CK2	4			
CK3	5			
CK4	6			
HOLD				

- **CK 1, CK2, CK3, CK 4** are 4 dedicated programmable logic signals (static or dynamic) which can be used for DUT Clock, DUT mode selection , Upset simulation ...
- **HOLD** is a dedicated signal generated by the test board circuitry ; HOLD = 1 disable all the event counters when the analog comparison is not available, during DUT level transitions ...

Event counters

signal	module	Pulse min.	Hold Off	function
CT1	16			SMALL or Logic event 1
CT2	18			MEDIUM or Logic event 2
CT3	20			LARGE or Logic event 3
CT4	22			Logic event 4

- signals CT1 ... CT4 are 4 count input channels , either for straightforward logic event acquisition or for window analog comparator acquisition
- Pulse min : minimum pulse width required , according to ove rall system bandwidth
- Hold Off: minimum delay imposed between the detection of two consecutive events

oscilloscope monitoring @50Ω

signal	Bandwidth	function	gain	nominal level
Vref				
Vout				

- **signals Vref** and **Vout** are the 2 analog input channels for both analog comparator and digital scope
- **Bandwidth:** overall channel bandwidth
- **gain:** channel gain between actual DUT level and scope displayed level

Note : The oscilloscope can be triggered by one of the event counter input signal CT1 ... CT4

Check test

nominal state check	
upset detection check	

To check that the device is operating properly, this test can be perform at any time under software control. The use of CK4 signal allows for two different modes :

- **nominal state check** : CK4 disable , absence of any event
- **upset detection check** : CK4 enable, presence of calibrated simulated event periodically introduced at a slow rate

Test board

Ref. : IL043-xx	Dim. :	slot :	

- Each set up is dedicated to a specific slot number, in order to ensure that each device is tested with the proper set up conditions.